SPP-800

Stereo Preparation Processor

[PATENT PENDING]

Circuit Research Labs, Inc.
2522 W. Geneva Drive Tempe, Arizona 85282 1-800-535-7648

TABLE OF CONTENTS

	Page
Warranty	III
Chapter I SPP-800 Stereo Preparation Processor	1-1
1.0 Introduction	1-1
1.1 Preventive Maintenance	1-2
1.2 Return for Repair Policy	1-2
Chapter II Installation	2-1
2.0 Initial Set Up	2-1
2.1 Initial Switch Positions	2-1
2.1.1 General	2-1
2.1.2 Front Panel Controls	2-1
2.1.3 Rear Panel Controls	2-1
2.2 Interconnections	2-2
2.2.1 General	2-2
2.2.2 Balanced Operation	2-3
2.2.3 Unbalanced Operation	2-4
2.3 Calibration	2-5
2.3.1 General	2-5
2.3.2 Tone Calibration Procedure	2-5
2.3.3 Dynamic Calibration Procedure	2-5
2.4 Calibration Deviations	2-6
2.4.1 General	2-6
2.4.2 Low Gain Calibration Procedure	2-7
Chapter III Operation	3-1
3.0 General	3-1
3.1 Front Panel Controls	3-1
3.1.1 Operation Switch	3-1
3.1.2 Gain Reduction Switch	3-2
3.1.3 Equalization Pot	3-3
3.1.4 Gate Switch	3-4
3.2 Rear Panel Controls	3-5
3.2.1 Input Calibrate Pots	3-5
3.2.2 Output Switch	3-5

3.2.3 Pink Noise Generator Switch 3-6
3.3 Internal Options 3-7
3.3.1 General 3-7
3.3.2 Stereo Strapping Option 3-7
3.3.3 Phase Processing Option 3-8
3.3.4 Input Attentuation 3-9
3.4 Status Indicators (External) 3-9
3.4.1 General 3-9
3.4.2 Input Level Indicators 3-10
3.4.3 Gate Status 3-11
3.5 Status Indicators (Internal) 3-12
3.5.1 General 3-12
3.5.2 High and Low Status 3-12
3.5.3 Medium/Fast Status 3-13
3.5.4 Power Supply Status 3-14
3.6 Proof Measurements 3-14
3.6.1 Defeating Gain Control 3-14
Chapter IV Theory of Operation
4.0 Simplified Theory of Operation 4-1
4.1 Simplified Block Diagram 4-2
4.2 Schematic Diagram 4-3
4.3 Parts List 4-4

LIST OF ILLUSTRATIONS

Figure	Title	Page
2-1	Front Panel Control Locations	2-1
2-2	Rear Panel Control Locations	2-2
2-3	Balanced Operation Connection Diagram	2-3
2-4	Unbalanced Operation Connection Diagram	2-4
2-5	Input Attenuator Switch Location	2-7
3-1	Operation Switch Location	3-1
3-2	Gain Reduction Switch Location	3-2
3-3	Equalization Pot Location	3-3
3-4	Gate Switch Location	3-4
3-5	Input Calibrate Pot Locations	3-5
3-6	Output Switch Location	3-5

Figure	Title	Page
3-7	Pink Noise Generator Switch Location	3-6
3-8	Stereo Strapping Location	3-7
3-9	Phase Processor Strapping Location	3-8
3-10	Input Attenuator Switch Location	3-9
3-11	Input Level Indicators	3-10
3-12	Gate Status Lamp Locations	3-11
3-13	High-Low Status Lamp Locations	3-12
3-14	Med/Fast Status Lamp Locations	3-13
3-15	Power Supply Status Lamp Locations	3-14

LIST OF TABLES

Table	Title	Page
2.1	Front Panel Control Positions	2-1
2.2	Rear Panel Control Positions	2-2
2.3	Input Attenuator Switch Positions	2-6
3.1	Operation Switch Settings Defined	3-2
3.2	Input Indicator Lamp Illumination Levels	3-10
3.3	Operation Switch Status Indicators	3-13

CHAPTER I

SPP-800

STEREO PREPARATION PROCESSOR

1.0 INTRODUCTION

Circuit Research Labs has created the SPP-800 Stereo Preparation Processor which meets the increasing demands competitive radio stations and recording studios require for their audio signal control.

The SPP-800 features unique utilization of (Patented) AGC circuits which have a highly sophisticated program control making internal alignment a thing of the past. This AGC action is normally slow and smooth, however, if there should be a sudden increase in signal level, the exclusive AGC circuits will automatically increase their response time. This will eliminate the distortion that has plagued the audio industry.

CRL's exclusive (patented) ZERO CROSS CHANNEL "IM" PROCESS produces virtually zero cross modulation of your stereo signal. Another unique feature of the SPP-800 is the internal strapping option which will produce pseudo wide band control if a true multiband processor is not required.

The versatility of the SPP-800 is increased by the front panel Equalizer Control. This control offers constant amplitude adjustment of the high and low parallel bands.

The SPP-800 will in fact, increase the loudness of the program material but not introduce any detrimental side effects.

With the audio sufficiently prepared by the SPP-800 you can be assured that the signal feeding the rest of your CRL system will be as clean as possible.

The combination of sophisticated circuit design and simplicity of operation makes your SPP-800 the ideal unit for your program processing.

CHAPTER II

INSTALLATION

2.0 INITIAL SET UP

2.1 INITIAL SWITCH POSITIONS

2.1.1 General

Before operating the SPP-800 Stereo Preparation Processor, the front and rear panel controls must be set so the starter/calibration procedure can be completed.

2.1.2 Front Panel Controls (Figure 2-1)

Table 2.1 shall define the position of the front panel controls on the SPP-800.

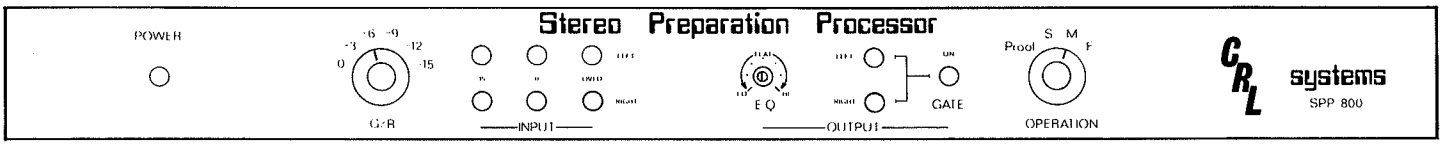


Figure 2-1 FRONT PANEL CONTROL LOCATIONS

TABLE 2.1 FRONT PANEL CONTROL POSITIONS

Control	Position
G/R Switch	Set to -6 position
EQ Pot	Set to the flat position (vertical position)
Gate Switch	Set to the ON position
Operation Switch	Set to the "M" position (Medium position)

2.1.3 Rear Panel Controls (Figure 2-2)

Table 2.2 shall define the position of the rear panel controls of the SPP-800.

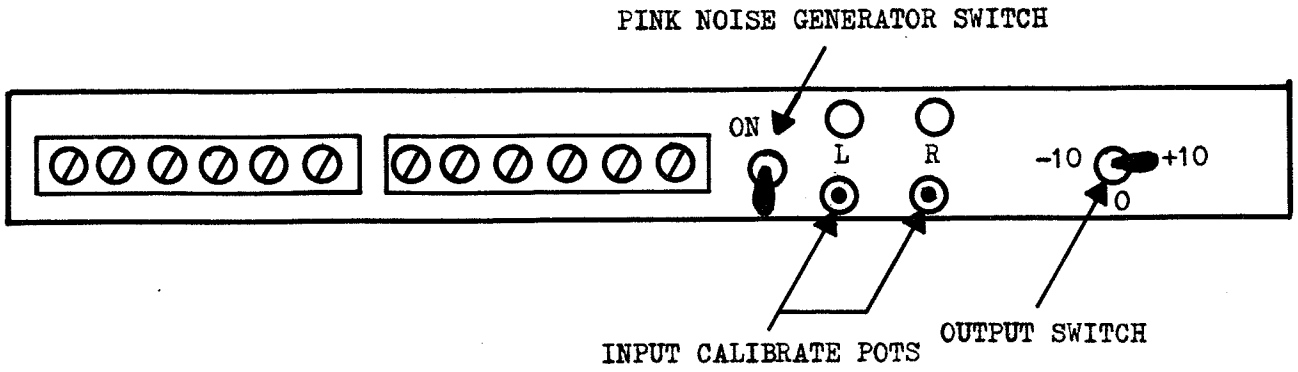


TABLE 2.2 REAR PANEL CONTROL POSITIONS

Control	Position
Pink Noise Generator Switch	Set to the STD position
Input Calibration Pot	Initially set for +4dbm input by the factory
Output Control	Set for -10 for direct AM system connections
	Set for 0 for direct FM system connections

It should be noted that most applications i.e. STL, Telco or direct hookup, require an output control setting of zero (0). However there are some stations that, due to their technical layout, may wish to use the -10 or +10 setting of the output control.

CAUTION

Check to insure that the STL or Telco equipment is not being overdriven if using the +10 output setting on your SPP-800.

2.2 INTERCONNECTIONS

2.2.1 General

The SPP-800 may be wired for either balanced or unbalanced operation. Paragraphs 2.2.2 and 2.2.3 shall define the connection procedure required for the balanced or unbalanced mode of operation respectively. The following connection procedures shall be for the left channel only but will also apply for the right channel. Determine if your system is balanced or unbalanced and proceed with the applicable

set of instructions.

2.2.2 Balanced Operation (Figure 2-3)

The following procedure shall define the interconnections that are required for the SPP-800 to operate in the balanced mode of operation.

NOTE

All interconnect cables should be shielded for best operation.

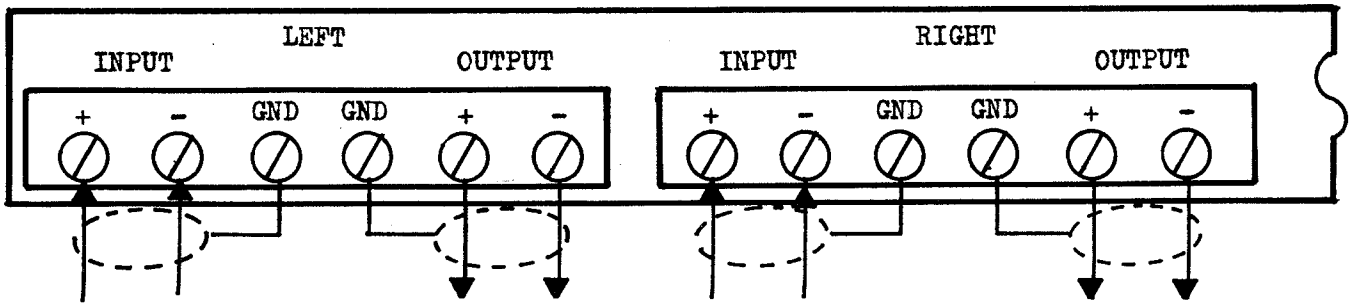


FIGURE 2-3 BALANCED OPERATION CONNECTION DIAGRAM

1. Connect the balanced audio OUTPUT cable from the console or other audio source to the terminals' labeled INPUT on the SPP-800.
2. Connect the balanced audio, INPUT cable, from the Telco, STL or recording equipment to the terminal labeled OUTPUT on the SPP-800.
3. Connect the shield of the cable connected to the SPP-800 INPUT to the Ground (GND) terminal closest to the INPUT terminals.
4. Connect the shield of the cable connected to the SPP-800 OUTPUT terminal to the Ground (GND) terminal closest to the OUTPUT terminal.

NOTE

It is imperative that both ends of the interconnect cables' shield be connected to Ground.

2.2.3 Unbalanced Operation (Figure 2-4)

The following procedure shall define the interconnections that are required for the SPP-800 to operate in the unbalanced mode of operation.

NOTE

All interconnect cables should be shielded for best operation.

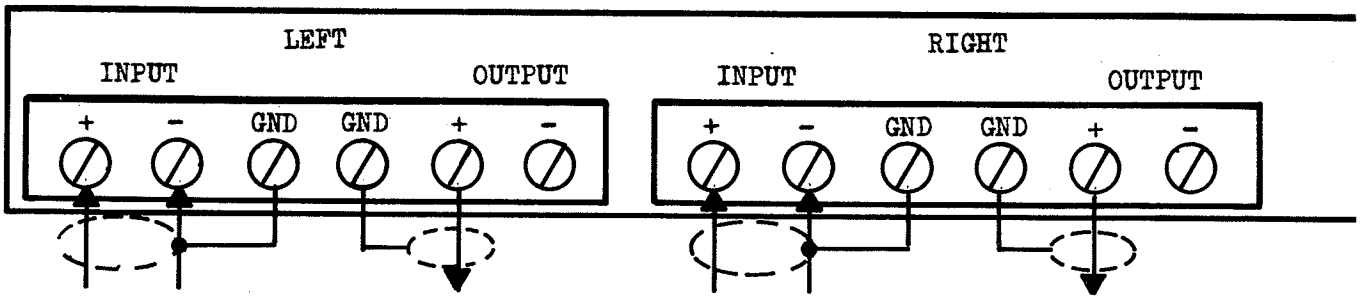


FIGURE 2-4 UNBALANCED OPERATION CONNECTION DIAGRAM

1. Connect the unbalanced audio OUTPUT cable from the console or other audio source to the plus (+) INPUT terminal on the SPP-800.
2. Connect the unbalanced audio INPUT cable from the Telco, STL or recording equipment to the plus (+) OUTPUT cable of the SPP-800.
3. Using a short section of wire, connect the minus (-) INPUT terminal of the SPP-800 to the Ground (GND) terminal closest to the INPUT terminal.
4. Connect the return of the unbalanced audio OUTPUT cable from the console or other source to the minus (-) INPUT terminal of the SPP-800.
5. Connect the shield of the cable connected to the SPP-800 INPUT to the Ground (GND) terminal closest to the INPUT terminals.
6. Connect the shield of the cable connected to the SPP-800 OUTPUT to the Ground (GND) terminal closest to the OUTPUT terminals.

NOTE

For unbalanced operation the minus (-) OUTPUT terminal must not be grounded. This output is directly coupled to the output of an amplifier and is not transformer coupled.

2.3 CALIBRATION

2.3.1 General

Once the front and rear panel controls are set and the rear panel interconnections are made the SPP-800 may be calibrated. Paragraph 2.3.2 shall define the tone calibration procedure and Paragraph 2.3.3 shall define the dynamic calibration procedure. Both procedures are just as accurate but by using the tone calibration procedure better balance will be produced than when using the dynamic calibration procedure. Determine which procedure fits your requirements and proceed with the applicable paragraph.

2.3.2 Tone Calibration Procedure

1. Apply a +3VU 1KHz sine wave to the SPP-800.
2. Apply power (115VAC) to the SPP-800.
3. Locate the left and right calibration pots and Light Emitting Diodes (LED's) on the rear panel of the SPP-800.
4. Rotate the left channel control pot, clockwise, until the left channel calibration LED just lights.
5. Repeat Step 4 for the right channel calibration.

NOTE

If the calibration LED's do not light until after 15 complete clockwise rotations, the input amplifiers may have to be set to a more sensitive setting. If this condition occurs proceed to Paragraph 2.4.

2.3.3 Dynamic Calibration Procedure

1. Adjust the input source for a OVU reference level.

NOTE

The signal used to calibrate the SPP-800 should be your typical program format.

2. Apply power (115VAC) to the SPP-800.

3. Locate the left and right channel calibration pots and Light Emitting Diodes (LED's) on the rear panel of the SPP-800. (Refer to Figure 2-2)
4. Rotate the left channel control pots, clockwise, until the left channel calibration LED flashes on program peaks approximately 10-20% of the time.
5. Repeat Step 4 for the right channel calibration.

NOTE

If the calibration LED's do not begin to flash until after 15 complete clockwise rotations, the input amplifiers may have to be set to a more sensitive setting. If this condition occurs proceed to Paragraph 2.4.

2.4 CALIBRATION DEVIATIONS

2.4.1 General

The SPP-800 is shipped from the factory with the input attenuators set at an input gain range of -5dbm to +20dbm. If during the calibration procedure described in Paragraph 2.3.2 or 2.3.3 it is determined that the input control attenuators do not have enough gain you will need to adjust the settings of the internal mini dip switches. (Refer to Figure 2-5 for switch location) If the input level entering the SPP-800 is between 0dbm and -20dbm the mini dip switches must be set in the medium sensitivity setting. If the input level is between -10dbm and -30dbm the mini dip switches must be set in the high sensitivity setting. Table 2.3 will define the proper switch settings for setting the gain of the SPP-800 in the medium or high sensitivity setting.

NOTE

In the following table and procedures the term "ON" will mean the switch is in the closed position and the term "OFF" will mean the switch is in the open position.

TABLE 2.3 ATTENUATOR SWITCH POSITIONS

Gain Range	Switch Setting			
	S1	S2	S3	S4
High Sensitive Setting (-10 to -30dbm)	On	On	On	On
Medium Setting (0 to -20dbm)	On	On	Off	Off
Standard Setting (-5 to +20dbm)	Off	Off	Off	Off

NOTE

The left and right channels mini dip switches are identical. The sensitivity switch settings will be the same for both channels.

2.4.2 If the calibration LED's do not begin to flash until after 15 complete clockwise rotations proceed as follows:

1. Remove power from the SPP-800.
2. Place the operation switch to the OVU position. (Refer to Figure 2-2 for switch location)
3. Rotate both calibration pots counterclockwise at least 20 complete rotations.
4. Remove the top cover of the SPP-800.
5. Locate the internal mini dip switches. (Refer to Figure 2-5 for switch location)
6. Place switches S1, S2, S3 and S4 on both the left and right channels in the pattern defined in Table 2.3 for the sensitivity setting required.
7. Replace the top cover of the SPP-800.
8. Apply power to the SPP-800.
9. Check the audio console or other programming source to insure the OVU setting, if using dynamic calibration, or +3VU if using tone calibration, has not drifted off its initial setting.
10. Rotate the left channel control pots, clockwise, until the calibration LED's flash on program peaks approximately 10 - 20% of the time for dynamic calibration or just light when using tone calibration.
11. Repeat Step 10 for the right channel calibration.

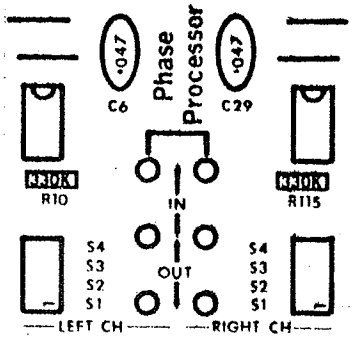


FIGURE 2-5 ATTENUATOR SWITCH LOCATION

CHAPTER III

OPERATION

3.0 GENERAL

The SPP-800 is now ready for operation. The output control, located on the rear panel has been set to either -10, 0 or +10 depending upon the requirements of the load being driven. We can now describe the function of the front and rear panel controls.

3.1 FRONT PANEL CONTROLS

3.1.1 Operation Switch (Figure 3-1)

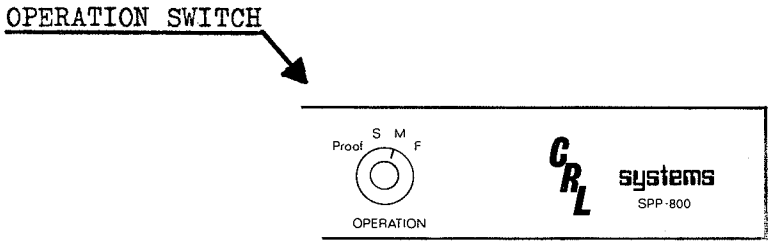


FIGURE 3-1 OPERATION SWITCH

The operation switch controls the operational speed of the Automatic Gain Control (AGC) circuits of the SPP-800 processor. As the operational speed of the AGC circuit is increased, the RMS energy and the loudness of the signal is increased without increasing its peak amplitude. The increase in RMS energy and loudness results in a decrease in the original musical dynamics being presented. The SPP-800's technology has minimized this drawback by making it very difficult to detect anything but an increase in the loudness when the signal's RMS energy is increased. The four settings, PROOF, S, M and F on the operation switch will be defined in Table 3.1.

TABLE 3.1 OPERATION SWITCH SETTING DEFINITION

Switch Setting	Definition
PROOF	This setting will connect the input amplifier to the output amplifier. With the switch in this position the AGC circuits will function as a normal linear amplifier.
S	When the switch is in this position the SPP-800 will behave like a slow AGC or "GAIN RIDER" processor.
M	When the switch is in this position the SPP-800 processor's AGC will have a medium release time. This setting will be optimum for most applications.
F	When the switch is in this position the SPP-800 processor's AGC will have a fast release time.

3.1.2 Gain Reduction Switch (Figure 3-2)

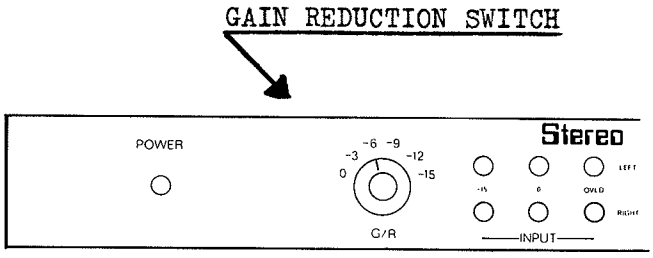


FIGURE 3-2 GAIN REDUCTION SWITCH

The gain reduction switch controls the range over which gain reduction will take place in the SPP-800. When the G/R switch is set in the -9 position, the medium-slow AGC circuit will hold the SPP-800 output constant if the input source material drops 9db below OVU as referenced from the audio source. If the input source material drops 10db or more, the output will drop no more than the difference between the G/R switch setting and the input source level. For example, the G/R switch is set at -9, and the input level drops 11db below OVU. The total drop in signal level at the output will be 2db below the OVU

setting. Signals may rise as much as 25db above OVU and not be affected by the G/R switch setting.

NOTE

AGC action is automatic above OVU.

In effect, this circuit gain rides the aberage signal level and tends to make up for "Jock Errors". Since the average and peak signal levels are being controlled by the SPP-800 you will detect a loudness increase when turning the G/R switch clockwise (towards -15). The greatest increase in loudness will be realized when the G/R switch is switched from 0 to -3 and from -3 to -6. By continuing to turn the switch towards the -15 position, there will be no additional increase in loudness.

Since there is a loss of long term dynamic integrity with higher switch settings, the position of this switch is of a subjective nature. CRL recommends that the G/R switch setting be set in as low a position to achieve your goal.

NOTE

A large amount of control is possible in the SPP-800 without the ear detecting any unpleasant side effects.

3.1.3 Equalization Pot (Figure 3-3)

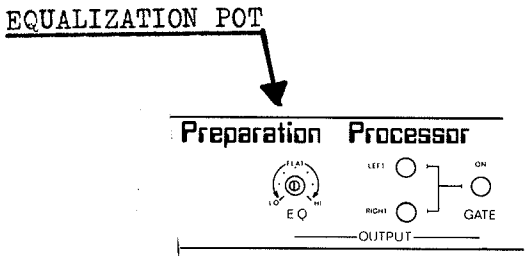


FIGURE 3-3 EQUALIZATION POT

The equalization pot controls the recombination of the high and low frequency bands in the SPP-800. After the audio signal passes through the

harmonic phase rotation network, producing a symmetrical waveform, it is split into high and low frequency bands. The high and low frequency bands, which are AGC controlled, are then recombined by the EQ pot. By rotating the pot in a clockwise direction (towards high) the gain of the high frequency band is increased and the low frequency band is reduced. By turning the pot counterclockwise (towards low) the gain of the low frequency band is increased and the high frequency band is reduced. The EQ pot will allow a gain adjustment of plus or minus 6db and is adjusted by using a small flat bladed screwdriver.

3.1.4 Gate Switch (Figure 3-4)

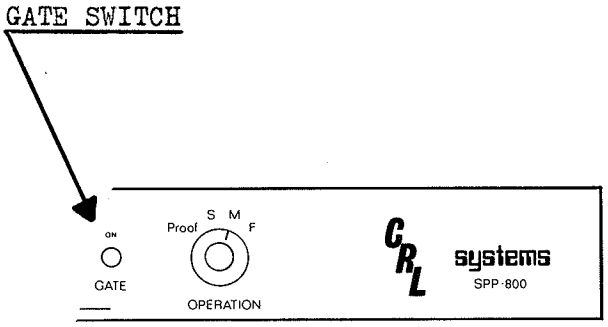


FIGURE 3-4 GATE SWITCH

The gate switch will prevent low level signals, such as noise, from being treated as intelligence by the AGC circuits. With the gate switch in the ON position (normal operating position), the gain control circuits will operate in the normal manner until the input drops to between -20db and -22db. When the input level drops below -20db all gain control circuits freeze. As the -20 to -22db threshold is crossed, the gain of the input will remain constant until the incoming signal level increases above the threshold. The gate lamp, located on the front panel will illuminate whenever there is a program pause.

3.2 REAR PANEL CONTROLS

3.2.1 Input Calibrate Pots (Figure 3-5)

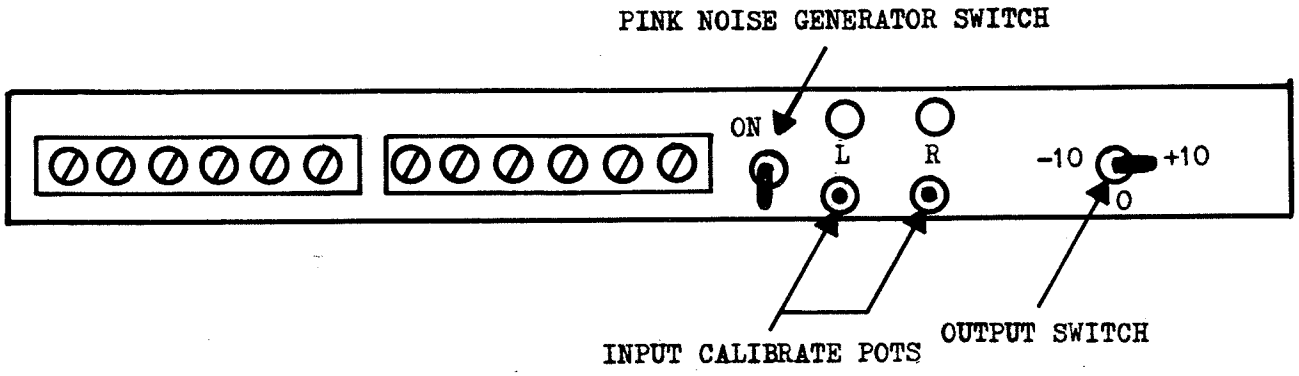


FIGURE 3-5 INPUT CALIBRATE POTS

The left and right channel input calibration pots are used to control the amount of input signal that will reach the input amplifiers of the SPP-800. The optimum amount of input signal that should reach the input amplifiers is OVU as indicated on your control console or automation system.

3.2.2 Output Switch (Figure 3-6)

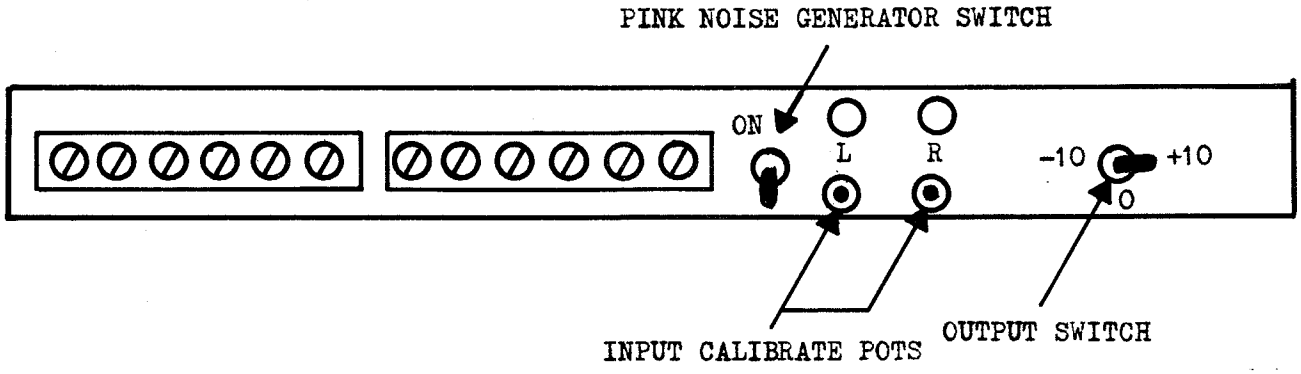


FIGURE 3-6 OUTPUT SWITCH

The output switch is used to control the output level of the SPP-800. Circuit Research Labs has designed the SPP-800 with the option of selecting either a 0, -10 or +10dbm output level. Although some STL or Telco links may require a +10dbm setting, care should be taken not to overdrive equipment by using the +10dbm output.

3.2.3 Pink Noise Generator Switch (Figure 3-7)

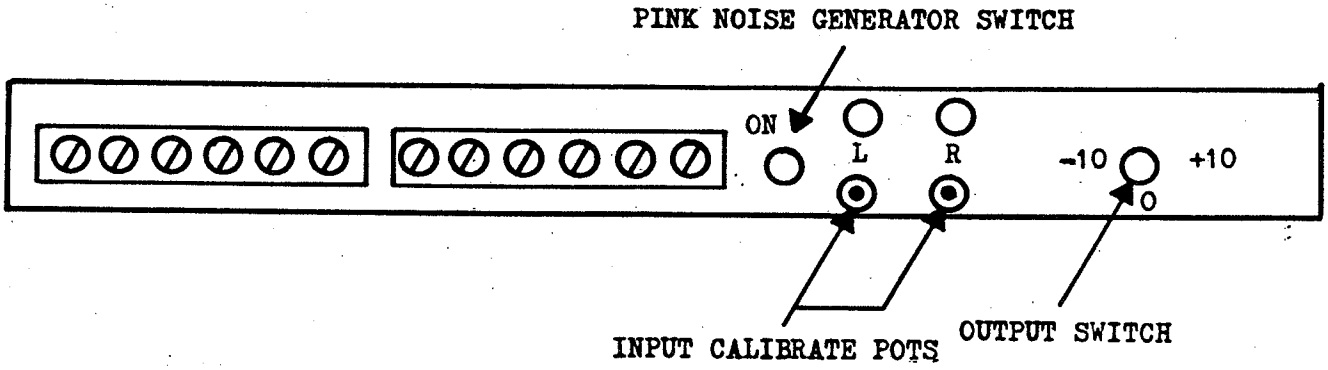


FIGURE 3-7 PINK NOISE GENERATOR SWITCH

The pink noise generator switch controls the white noise generator that has been built into the SPP-800 for support equipment calibration. This generator, although not a highly precision generator, is de-emphasized -3db per octive as the frequency increases. During normal operation of the SPP-800 Stereo Preparation Processor this switch must be in the OFF position.

When using the pink noise generator to calibrate other CRL equipment a few minor adjustments must be made to the SPP-800. These adjustments are:

1. Set the EQ pot to the vertical (flat) position.
2. Set the pink noise generator switch to the ON position.

NOTE

The EQ pot has a ±6db gain range that will affect the pink noise generator's -3db de-emphasis feature and frequency spectrum if not placed in the vertical position.

By placing the SPP-800 in the auxilary equipment calibration mode other CRL equipment can be calibrated. The other CRL equipment, SEP-400, SEP-400A, SMC-600A or the SMP-800, can be calibrated by setting their calibration pots so that the calibration or peak lamps just begin to flicker. It is recommended that you refer to each unit's calibration procedure to insure that the equipment's controls are set in the proper position for calibration. After all the CRL equipment has been calibrated,

the pink noise generator signal is ready to enter your transmitter or stereo generator. To do this set the peak limiter on the PMC-300, PMC-400, SMC-600 or SMP-800 to their maximum process/clipping setting and then set the input levels entering your transmitter or stereo generator.

NOTE

When setting up an older AM transmitter you may wish to use less than full process to avoid damage to your transmitter or antenna system.

The signal from the pink noise generator contains low frequency pulse information that is suitable for setting frequency tilt corrections. The pink noise generator, by being a mono signal, is suitable for setting the left and right null, and for balancing the controls of your stereo processing system.

3.3 INTERNAL OPTIONS

3.3.1 General

The SPP-800 offers two operational options which are built into the printed circuit board layout. These options, phase processing and stereo strapping will be described in the following paragraphs.

3.3.2 Stereo Strapping (Figure 3-8)

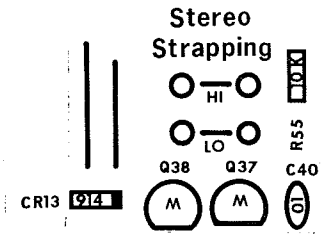


FIGURE 3-8 STEREO STRAP LOCATION

The left and right channel AGC circuitry is strapped together when the SPP-800 is shipped from the factory. This strapping allows the right channel to be controlled by the overall gain of the left channel

program material and the gain of the left channel to be controlled by the right channel program material. This insures that the center image of the stereo program will not shift due to processing. Both the low and high bands of the left and right channels are strapped together to track. If you wish to unstrap the gain control, remove the jumper straps shown in Figure 3-8.

3.3.3 Phase Processing (Figure 3-9)

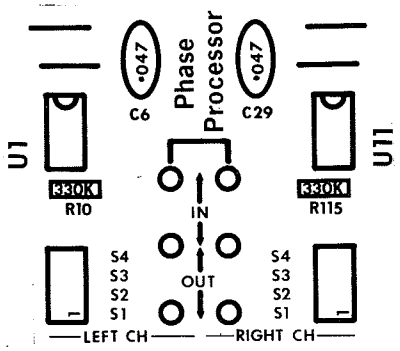


FIGURE 3-9 PHASE STRAP LOCATION

A two stage all pass filter, located on the input side of the AGC processing path, intentially shifts the phase response of the system based on the frequency content. This filter, which will not affect amplitude response, will produce symmetrical waveforms for entrance to the AGC circuitry. These symmetrical waveforms will allow cleaner processing of the voices in the audio signal. This phase processing can be eliminated by removing the straps from the IN position and placing them in the OUT position. (Refer to Figure 3-9 for strap location)

NOTE

The phase processor will not degrade the mono signal content.

3.3.4 Input Attentuation (Figure 3-10)

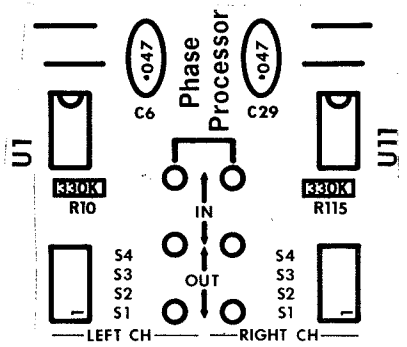


FIGURE 3-10 INPUT ATTENTUATOR LOCATION

The SPP-800 has an identical gain attenuator on each channel. Each attenuator is controlled by a four position mini dip switch. These mini dip switches will select three overlapping gain ranges. These gain ranges are -30dbm to -10dbm, -20dbm to 0dbm and -5dbm to 20dbm. It is possible to select different gain ranges for the left and right channel but is not recommended. For detailed information concerning the setting of the three gain ranges, refer to Paragraph 2.4, Calibration Deviation Procedure.

3.4 STATUS INDICATORS (EXTERNAL)

3.4.1 General

Two sets of status indicators have been included on the front panel of the SPP-800 to give the operator a constant update on system operation. These indicators are the input level indicators and gating status, both indications will be defined in Paragraphs 3.4.2 and 3.4.3 respectively.

3.4.2 Input Level Indicators (Figure 3-11)

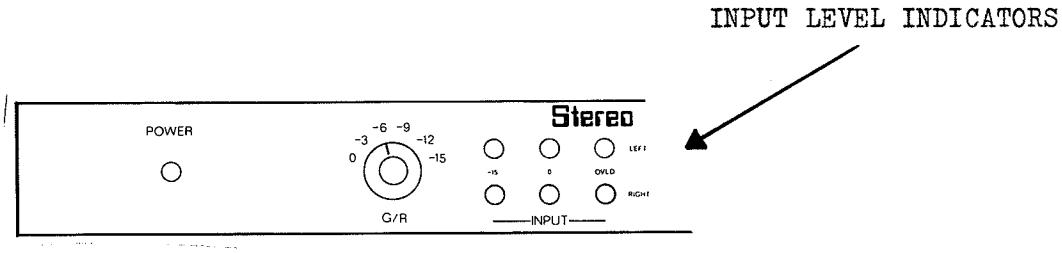


FIGURE 3-11 INPUT LEVEL INDICATORS

The input level indicators will light and remain lit when the pre-determined input levels of the program material are reached. Table 3.2 will define the levels at which each lamp will light when the input signal is calibrated to the OVU reference level as indicated on your audio console or automation system.

TABLE 3.2 INDICATOR LAMPS' ILLUMINATION LEVELS

Lamp	Illumination Level
-15	-15db below the OVU calibration reference level
0	Signals that exceed the OVU calibration reference level
OVLD	Signals that are 12db above the OVU calibration reference level

NOTE

The top row of lamps indicate the left channel and the bottom row of lamps indicate the right channel on the SPP-800.

3.4.3 Gate Status (Figure 3-12)

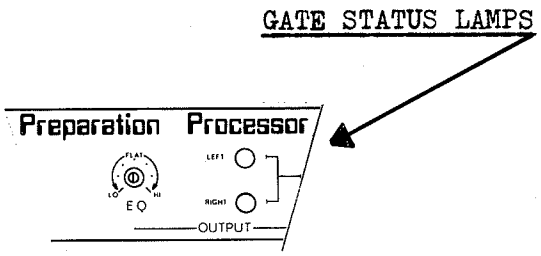


FIGURE 3-12 GATE STATUS LAMPS

The gate status lamps indicate the amount of gating activity occurring in the AGC circuits of the SPP-800. When the gate switch is on these lamps will light everytime the SPP-800 goes into the linear amplifier mode of operation. When the AGC circuits are automatically reactivated the lamps will go out.

3.5 STATUS INDICATORS (INTERNAL)

3.5.1 General

The SPP-800 has three separate sets of status indicators located within the unit. These status indicators will be defined in Paragraphs 3.5.2 through 3.5.4.

3.5.2 High and Low Status (Figure 3-13)

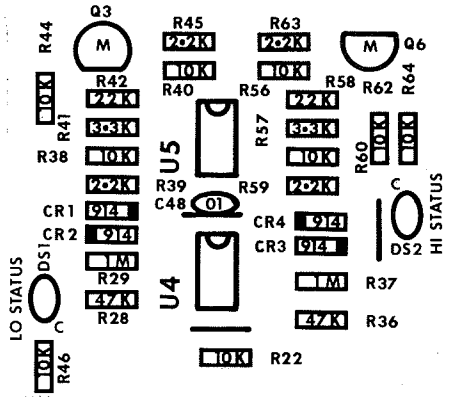


FIGURE 3-13 HIGH LOW STATUS LAMPS

The high and low status LED's indicate the status of the control current feeding the OTA circuits. Each lamp indicates the status of their respective band, i.e. high lamp for the high band and low lamp for the low band. During normal operation the lamps will be fully lit but should the control circuitry fail, the lamps will either dim or go completely out.

NOTE

During normal programming these lamps may dim SLIGHTLY in some units. This condition is normal and will not affect system operation.

3.5.3 MED/FAST Status (Figure 3-14)

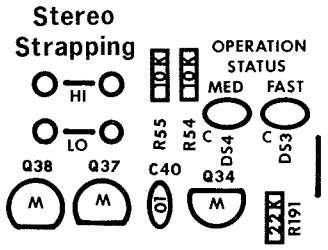


FIGURE 3-14 MED/FAST STATUS LAMPS

The MED/FAST indicators indicate the condition of the control voltage on the operation switch. Table 3.3 shall define the lamp indications when the operation switch is in each of its possible positions.

TABLE 3.3 OPERATION SWITCH STATUS INDICATIONS

Operation Switch Position	Lamp Indications MED	FAST
PROOF	OFF	OFF
S (Slow)	OFF	OFF
M (Medium)	ON	OFF
F (Fast)	OFF	ON

If the lamps do not follow the sequence defined in Table 3.2 there may be a problem with either the operation switch, wiring harness or solid state switches.

3.5.4 Power Supply Status (Figure 3-15)

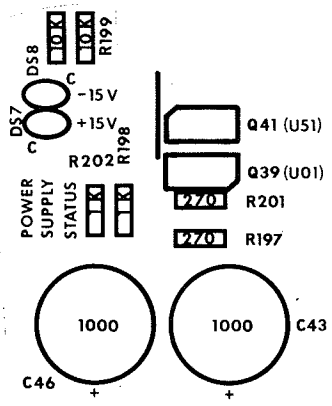


FIGURE 3-15 POWER SUPPLY STATUS LAMPS

Two LED's DS-7 and DS-8, monitor the output voltage of the SPP-800's internal power supply. Should the -15VDC supply fail LED DS-8 will dim or go out, and if the +15VDC supply fails LED DS-7 will dim or go out.

3.6 PROOF MEASUREMENTS

3.6.1 Defeating Gain Control

Frequency response and distortion measurements may have to be made in some applications (mainly broadcast). To obtain the correct data the automatic gain control circuits must be defeated. To do this place the operation switch into the PROOF position, this will place the AGC circuits in the linear amplifier mode.

CHAPTER IV

THEORY OF OPERATION

4.0 SIMPLIFIED THEORY OF OPERATION (Refer to Block Diagram Figure 4.1)

The following Simplified Theory of Operation is for one channel of the SPP-800. However both channels are identical.

The external audio signal enters the SPP-800 through the balanced audio input terminals located on the rear panel. The audio input is adjusted by the INPUT CAL POT, also located on the rear panel, which is used to set the unit's pre-determined input reference level before entering the INTERNAL INPUT ATTENUATION SWITCHES.

The INTERNAL INPUT ATTENUATION SWITCHES are used to adjust the overall input sensitivity to one of three ranges. These ranges are High (-10 to -30dbm), Med (0 to -20dbm) and Low (-5 to +20dbm).

After the appropriate input sensitivity has been selected it enters an active balanced input amplifier. This circuit eliminates the need for a passive balanced input transformer and the audio degradation or distortion it produces.

The balanced input signal then enters the phase scrambler circuit. This circuit is an all pass constant amplitude filter which is used to eliminate most of the asymmetry in the program content. Asymmetry is removed at this point to prevent audio loudness from being lossed in the following gain reduction. This feature may be removed, if desired, by placing the jumper located on the printed circuit board in the "Out" position. Once the asymmetry is removed, the Gain Reduction (G/R) switch, will allow the user to select the desired pre-programmed amount of gain reduction to maintain constant level at the unit output for audio signals which fall below the input gain reduction threshold. This precision gain reduction network will accurately repeat six different reduction levels ranging from 0 to -15db.

Following the G/R switch a two position pink noise/standard switch can be used to select the internal pink noise generator. This generator when activated by the switch can be used to align

later processing equipment or amplifiers. Placing the switch in the standard position allows the SPP-800 to operate in its normal mode of operation from the preceeding stages.

The High and Low Band AGC circuits provide the means in which to initiate the optimum attack and release times chosen by the PROGRAM CONTROL MEMORY. The attack and release times chosen for frequencies below 400Hz are initiated in the low frequency AGC circuitry while the frequencies above 400Hz are initiated in the High frequency AGC circuitry.

The high and low frequencies are recombined by the unique EQ pot circuit configuration. This circuit will automatically subtract high frequency energy when low frequency energy is added. It will also add high frequency energy when low frequency energy is subtracted. This addition or subtraction of high and low frequency energy results in a constant amplitude output when frequency content is varied, thereby creating constant amplitude equalizing.

The High and Low Band signal's attack and release times are selected by the front panel operation switch. This four position switch can be set to three positions of operation, Slow, Medium and Fast, and the Proof position. The Slow position is equivalent to a slow and gentle gain riding element while the Medium position is a more radical or faster gain riding element. In the Fast position the multiband device becomes a multiband AGC compressor which will remove both long term and medium term dynamic ranges. The fourth position, Proof, is used when the SPP-800 must be placed in the by-pass condition. This position is used when static measurements or proof of performance measurements must be made.

The output control switch selects one of three output signal levels available in the SPP-800. The active balanced output, -10, 0 or +10db referenced into 600 ohms, is then conditioned for driving long low impedance balanced program lines in the active balanced output configuration referenced to chassis ground.

ADDITIONAL FEATURES:

Input LED indicators:

CRL has designed a unique visual input signal indicator system

into the SPP-800. The three front panel LED indicators simulate a simple VU meter monitor of the input signal. The LED labeled "-15" will illuminate when the input signal becomes greater than -15db below the signal threshold of Odb. The "O" LED will light when the signal reaches the gain reduction input threshold reference level of Odb. If the signal exceeds the desired range and begins reaching possible distortion levels the "OVLD" LED will light. When this LED lights the input of the SPP-800 is usually being overdriven by the equipment preceeding the unit. This LED indicator network has been placed at the output of the phase scrambler circuit, thereby allowing the SPP-800 to condition the signal as much as possible before measuring the audio level. This method and location of signal measurement gives the user a true indication of the quality of signal that is about to be processed in the SPP-800.

Gate Switch:

The gate switch and LED indicator, located on the front panel are tied to the high and low band AGC circuits. This switch, which activates a circuit unique to the SPP-800, will freeze or lock the G/R stages at constant gain for input signals at -22db below the input reference level, if it drops lower than -22db. When the input signal reaches -22db below reference the gate LED will light and remain lit until the signal level increases back toward O reference level. After the signal increases past -22db the LED will go off and the normal attack and release times of the AGC circuitry will resume.

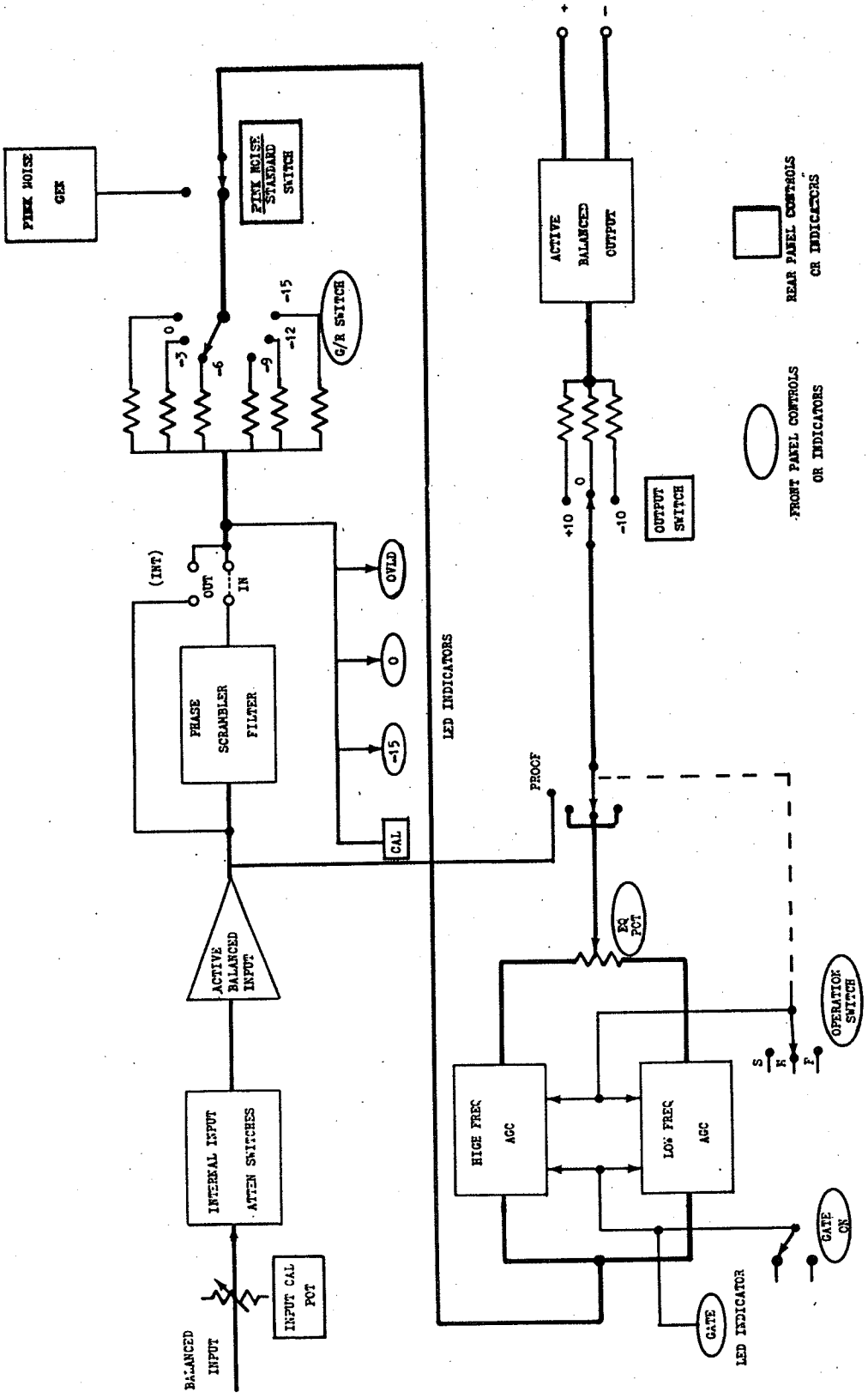


FIGURE 4.1 SIMPLIFIED BLOCK DIAGRAM

CAPACITORS
ALL VALUES ARE IN MICROFARADS UNLESS OTHERWISE NOTED

C 1	10 ELECTROLYTIC 16V	C 2	10 ELECTROLYTIC 16V
C 3	10 ELECTROLYTIC 16V	C 4	10 ELECTROLYTIC 16V
C 5	.047 POLYESTER 2% 100V	C 6	.047 POLYESTER 2% 100V
C 7	2.2 TANTALUM 20% 16V	C 8	.047 POLYESTER 2% 100V
C 9	.1 POLYESTER 10% 100V	C 10	.22 POLYESTER 10% 100V
C 11	.047 POLYESTER 2% 100V	C 12	.1 POLYESTER 10% 100V
C 13	.22 POLYESTER 10% 100V	C 14	10 PF CERAMIC 10% 50V
C 15	10 PF CERAMIC 10% 50V	C 16	2.2 TANTALUM 20% 16V
C 17	.01 POLYESTER 10% 100V	C 18	.01 POLYESTER 10% 100V
C 19	2.2 TANTALUM 20% 16V	C 20	.22 POLYESTER 10% 100V
C 21	.047 POLYESTER 5% 100V	C 22	.047 POLYESTER 5% 100V
C 23	10 ELECTROLYTIC 16V	C 24	10 ELECTROLYTIC 16V
C 25	10 ELECTROLYTIC 16V	C 26	10 ELECTROLYTIC 16V
C 27	10 ELECTROLYTIC 16V	C 28	.047 POLYESTER 2% 100V
C 29	.047 POLYESTER 2% 100V	C 30	2.2 TANTALUM 20% 16V
C 31	.047 POLYESTER 2% 100V	C 32	.1 POLYESTER 10% 100V
C 33	.22 POLYESTER 10% 100V	C 34	.047 POLYESTER 2% 100V
C 35	.1 POLYESTER 10% 100V	C 36	.22 POLYESTER 10% 100V
C 37	10 PF CERAMIC 10% 50V	C 38	10 PF CERAMIC 10% 50V
C 39	2.2 TANTALUM 20% 16V	C 40	.01 POLYESTER 10% 100V
C 41	.01 POLYESTER 10% 100V	C 42	470 ELECTROLYTIC 50V
C 43	1000 ELECTROLYTIC 16V	C 44	.22 POLYESTER 10% 100V
C 45	470 ELECTROLYTIC 50V	C 46	1000 ELECTROLYTIC 16V
C 47	.22 POLYESTER 10% 100V	C 48	.01 POLYESTER 10% 100V
C 49	.01 POLYESTER 10% 100V	C 50	.01 POLYESTER 10% 100V
C 51	.01 POLYESTER 10% 100V	C 52	.01 POLYESTER 10% 100V
C 53	.001 FEEDTHRU (TO BRIDGE)	C 54	.001 FEEDTHRU (TO BRIDGE)
C 55	.001 FEEDTHRU (R-OUT)	C 56	.001 FEEDTHRU (R+OUT)
C 57	.001 FEEDTHRU (R-IN)	C 58	.001 FEEDTHRU (R+IN)
C 59	.001 FEEDTHRU (L-OUT)	C 60	.001 FEEDTHRU (L+OUT)
C 61	.001 FEEDTHRU (L-IN)	C 62	.001 FEEDTHRU (L+IN)
C 63	.047 POLYESTER 5% 100V	C 64	.047 POLYESTER 5% 100V
C 65	22 TANTALUM 20% 16V	C 66	.01 POLYESTER 10% 100V

DIODES

CR 1	1N914	CR 2	1N914
CR 3	1N914	CR 4	1N914
CR 5	1N914	CR 6	1N914
CR 7	1N914	CR 8	1N914
CR 9	1N914	CR 10	1N914
CR 11	1N914	CR 12	1N914
CR 13	1N914	CR 14	1N914
CR 15	1N914	CR 16	1N914
CR 17	1N914	CR 18	1N914
CR 19	1N914	CR 20	1N914
CR 21	1N914	CR 22	1N914
CR 23	1N914	CR 24	1N914
CR 25	1N4001	CR 26	1N4001
CR 27	1N4001	CR 28	1N4001
CR 29	1N4001	CR 30	1N4001

LEDS

DS 1	MV55A (LOW STATUS<L>)	DS 2	MV55A (HIGH STATUS<L>)
DS 3	MV55A (OP STATUS<FAST>)	DS 4	MV55A (OP STATUS<MED>)
DS 5	MV55A (LOW STATUS<R>)	DS 6	MV55A (HIGH STATUS<R>)
DS 7	MV55A (+15V)	DS 8	MV55A (-15V)
DS 9	2190M94 (POWER)	DS 10	2190M95 (-15 L)
DS 11	2190M95 (-15 R)	DS 12	2190M96 ("0" CAL L FNT)
DS 13	2190M96 ("0" CAL R FNT)	DS 14	2190M94 (OVLD L)
DS 15	2190M94 (OVLD R)	DS 16	2190M94 (GATE OUT L)
DS 17	2190M94 (GATE OUT R)	DS 18	2190M96 ("0" CAL L REAR)
DS 19	2190M96 ("0" CAL R REAR)		

FUSES

F 1	3/10 AMP SLO-BLOW

COILS

L 1	1.2 UH (R-OUT)	L 2	1.2 UH (R+OUT)
L 3	1.2 UH (R-IN)	L 4	1.2 UH (R+IN)
L 5	1.2 UH (L-OUT)	L 6	1.2 UH (L+OUT)
L 7	1.2 UH (L-IN)	L 8	1.2 UH (L+IN)

TRANSISTORS

Q 1	MPS404A	Q 2	2N4123
Q 3	MPS404A	Q 4	MPS404A
Q 5	MPS404A	Q 6	MPS404A
Q 7	MPS404A	Q 8	MPS404A
Q 9	MPF102	Q 10	MPF102
Q 11	MPF102	Q 12	MPF102
Q 13	2N4125	Q 14	2N4123
Q 15	2N4125	Q 16	MPS404A
Q 17	2N4123	Q 18	MPS404A
Q 19	2N4125	Q 20	MPS404A
Q 21	2N4123	Q 22	MPS404A
Q 23	MPS404A	Q 24	MPF102
Q 25	MPF102	Q 26	MPF102
Q 27	MPF102	Q 28	MPS404A
Q 29	MPS404A	Q 30	MPS404A
Q 31	MPS404A	Q 32	2N4125
Q 33	2N4123	Q 34	2N4125
Q 35	MPS404A	Q 36	2N4123
Q 37	MPS404A	Q 38	2N4125
Q 39	NSDU01	Q 40	MJE720
Q 41	NSDU51	Q 42	MJE710

RESISTORS
ALL RESISTORS ARE 5% 1/4 WATT UNLESS OTHERWISE NOTED

R 1	620	R 2	4.7K
R 3	4.7K	R 4	68K
R 5	68K	R 6	10K
R 7	10K	R 8	1.5K
R 9	1.5K	R 10	330K
R 11	330K	R 12	10.0K 1%
R 13	22.1K 1%	R 14	10.0K 1%
R 15	10.0K 1%	R 16	22.1K 1%
R 17	10.0K 1%	R 18	1K
R 19	10K	R 20	1.5K
R 21	22K	R 22	10K
R 23	68K	R 24	10K
R 25	1K	R 26	2.2M
R 27	2.2K	R 28	47K
R 29	1M	R 30	10K
R 31	68K	R 32	10K
R 33	1K	R 34	2.2M
R 35	2.2K	R 36	47K
R 37	1M	R 38	10K
R 39	2.2K	R 40	10K
R 41	3.3K	R 42	22K
R 43	2.2K	R 44	10K
R 45	2.2K	R 46	10K
R 47	22K	R 48	10K
R 49	470K	R 50	470K
R 51	10K	R 52	220K
R 53	10K	R 54	10K
R 55	10K	R 56	10K
R 57	3.3K	R 58	22K
R 59	2.2K	R 60	10K
R 61	1K	R 62	10K
R 63	2.2K	R 64	10K
R 65	22K	R 66	10K
R 67	470K	R 68	470K
R 69	10K	R 70	220K
R 71	10K	R 72	3.3K
R 73	4.7K	R 74	68K
R 75	6.8K	R 76	100K
R 77	10K	R 78	100K
R 79	10K	R 80	10K
R 81	100K	R 82	100K
R 83	10K	R 84	10K
R 85	39K	R 86	22
R 87	22K	R 88	100K
R 89	22	R 90	6.8K
R 91	100K	R 92	100
R 93	22K	R 94	39K
R 95	100K	R 96	22K
R 97	27K	R 98	68K
R 99	39K	R 100	68K
R 101	*	R 102	6.8K

R 103 1.2K
R 104 1.2K
R 105 270
R 106 620
R 107 4.7K
R 108 4.7K
R 109 68K
R 110 68K
R 111 10K
R 112 10K
R 113 1.5K
R 114 1.5K
R 115 330K
R 116 330K
R 117 10.0K 1%
R 118 22.0K 1%
R 119 10.0K 1%
R 120 10.0K 1%
R 121 22.1K 1%
R 122 10.0K 1%
R 123 1K
R 124 10K
R 125 1.5K
R 126 22K
R 127 10K
R 128 68K
R 129 10K
R 130 1K
R 131 2.2M
R 132 2.2K
R 133 47K
R 134 1M
R 135 10K
R 136 68K
R 137 10K
R 138 1K
R 139 2.2M
R 140 2.2K
R 141 47K
R 142 1M
R 143 10K
R 144 2.2K
R 145 10K
R 146 3.3K
R 147 22K
R 148 2.2K
R 149 10K
R 150 2.2K
R 151 10K
R 152 22K
R 153 10K
R 154 470K
R 155 470K
R 156 10K
R 157 220K
R 158 10K
R 159 10K
R 160 3.3K
R 161 22K
R 162 2.2K
R 163 10K
R 164 1K
R 165 10K
R 166 2.2K
R 167 10K
R 168 22K
R 169 10K
R 170 470K
R 171 470K
R 172 10K
R 173 220K
R 174 10K
R 175 3.3K
R 176 4.7K
R 177 68K
R 178 6.8K
R 179 10K
R 180 39K
R 181 22
R 182 22K
R 183 100K
R 184 22
R 185 6.8K
R 186 100K
R 187 100
R 188 22K
R 189 39K
R 190 100K
R 191 22K
R 192 27K
R 193 68K
R 194 39K
R 195 68K
R 196 100K/PWR SUPPLY 1K
R 197 270
R 198 1K
R 199 10K
R 200 1K
R 201 270
R 202 1K
R 203 10K
R 204 100K
R 205 100K
R 206 100K
R 207 100K
R 208 100K
R 209 5K MULTITURN POT
R 210 4.7K
R 211 2.7K
R 212 1.8K
R 213 1K
R 214 390

R 215 1K	R 216 390
R 217 10K	R 218 10K POT
R 219 10K	R 220 1K
R 221 5K MULTITURN POT	R 222 4.7K
R 223 2.7K	R 224 1.8K
R 225 1K	R 226 390
R 227 1K	R 228 10K
R 229 10K POT	R 230 10K

SWITCHES

S 1 1/4 MINI DIPSWITCH <L&R>	S 2 1/4 MINI DIPSWITCH <L&R>
S 3 1/4 MINI DIPSWITCH <L&R>	S 4 1/4 MINI DIPSWIYCH <L&R>
S 5 ROTARY (G/R)	S 6 105D TOGGLE (GATE)
S 7 ROTARY (OPERATION)	S 8 105E TOGGLE (OUTPUT CNTRL)
S 9 3P 2T TOGGLE (PINK N/OPER)	

TRANSFORMERS

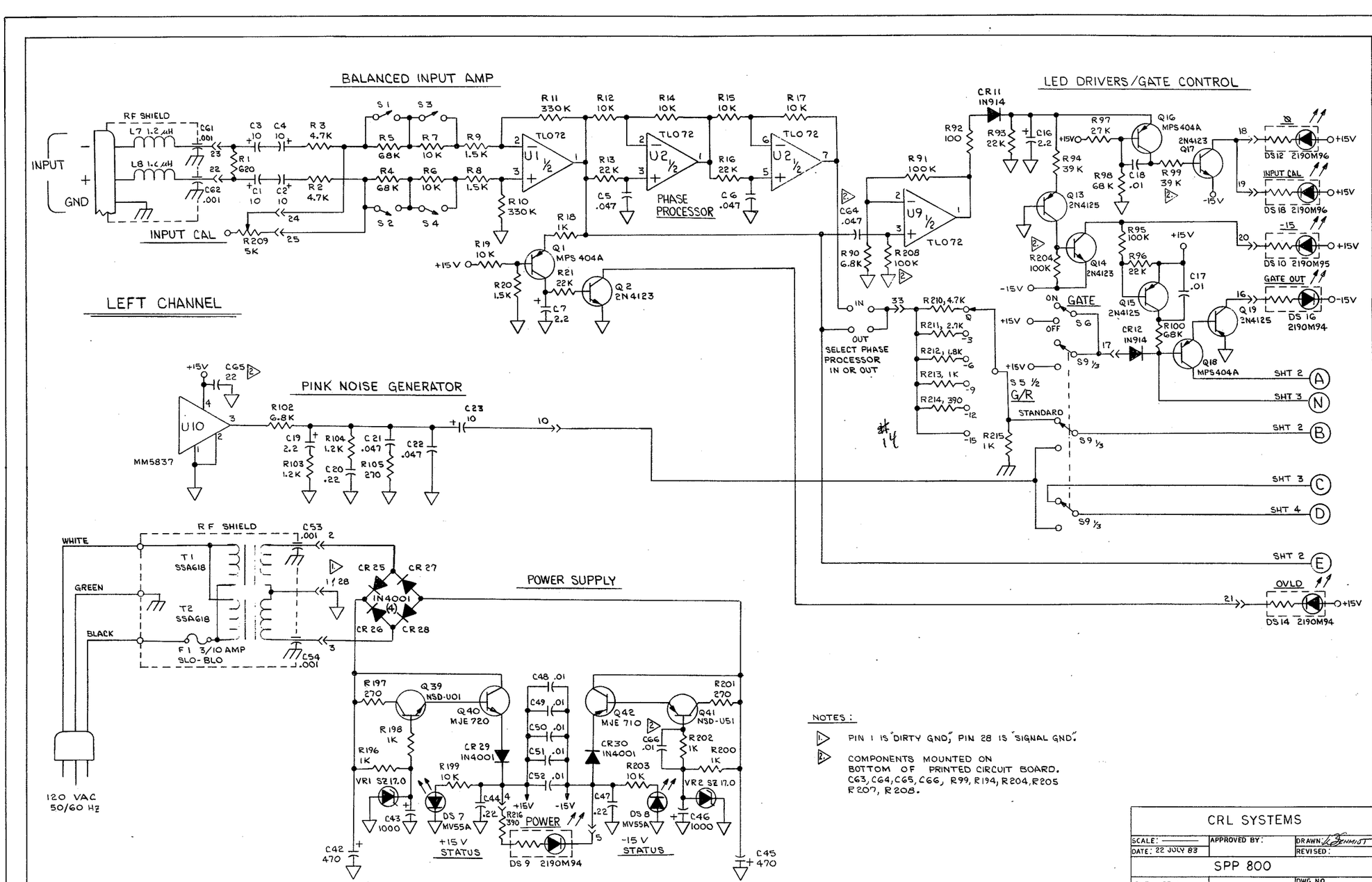
T 1 SSA618	T 2 SSA618

ICS

U 1 TL072	U 2 TL072
U 3 LM13600N	U 4 TL072
U 5 TL072	U 6 502 MODULE
U 7 TL072	U 8 TL072
U 9 TL072	U 10 MM5837
U 11 TL072	U 12 TL072
U 13 LM13600N	U 14 TL072
U 15 TL072	U 16 502 MODULE
U 17 TL072	U 18 TL072

ZENERS

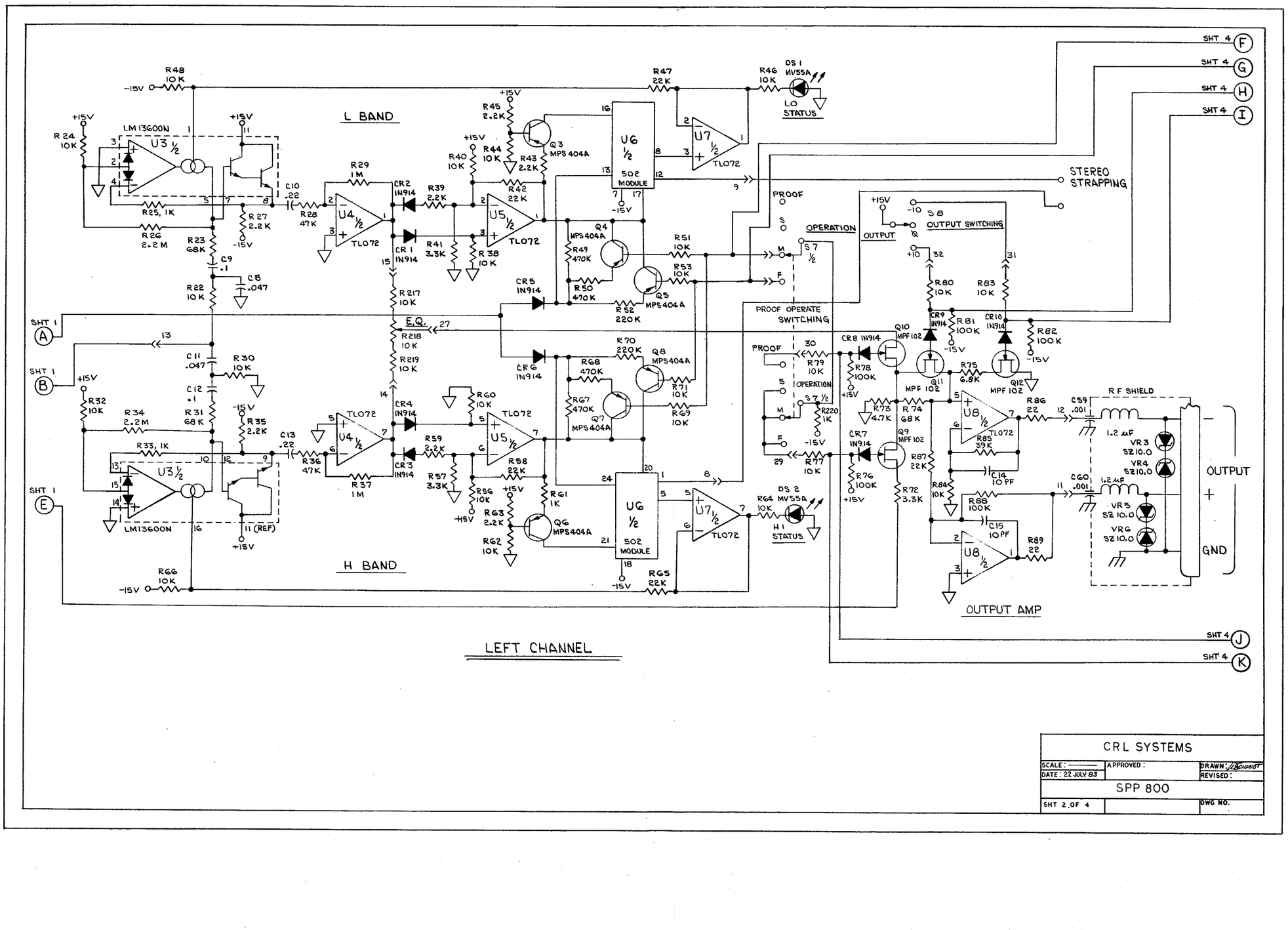
VR 1 SZ17.0	VR 2 SZ17.0
VR 3 SZ10.0	VR 4 SZ10.0
VR 5 SZ10.0	VR 6 SZ10.0
VR 7 SZ10.0	VR 8 SZ10.0
VR 9 SZ10.0	VR 10 SZ10.0



NOTES :

1. PIN 1 IS "DIRTY GND," PIN 28 IS "SIGNAL GND."
2. COMPONENTS MOUNTED ON BOTTOM OF PRINTED CIRCUIT BOARD. C63, C64, C65, C66, R99, R194, R204, R205 R207, R208.

CRL SYSTEMS		
SCALE:	APPROVED BY:	DRAWN: L. SCHMIDT
DATE: 22 JULY 83		REVISED:
SPP 800		
SHT 1 OF 4		DWG NO.


L BAND
H BAND
LEFT CHANNEL
LM13600N
TL072
MPS404A
502 MODULE
MV55A
MPF 102
IN914
E.Q.
PROOF OPERATE SWITCHING
OUTPUT SWITCHING
STEREO STRAPPING
RF SHIELD
OUTPUT AMP
LO STATUS
HI STATUS
OUTPUT
GND
SHT 1
SHT 4
CRL SYSTEMS
SCALE: ——
DATE: 22 JULY 83
APPROVED:
DRAWN: J. SCHMIDT
REVISED:
SPP 800
SHT 2 OF 4
DWG NO.

BALANCED INPUT AMP

INPUT +
INPUT −
GND
RF SHIELD
L3 1.2 μH
L4 1.2 μH
C57 .001
C58 .001
R106 620
C26 10
C27 10
C24 10
C25 10
R108 4.7K
R107 4.7K
39
40
38
37
INPUT CAL
R221 5K
S1
S2
S3
S4
R110 68K
R112 10K
R109 68K
R111 10K
R114 1.5K
R113 1.5K
R116 330K
R117 10K
R119 10K
R120 10K
R122 10K
U11 ½ TL072
U12 ½ TL072
U12 ½ TL072
R118 22K
R121 22K
C28 .047
C29 .047
PHASE PROCESSOR
R115 330K
R123 1K
+15V
R124 10K
R125 1.5K
Q20 MPS404A
R126 22K
Q21 2N4123
C30 2.2

RIGHT CHANNEL

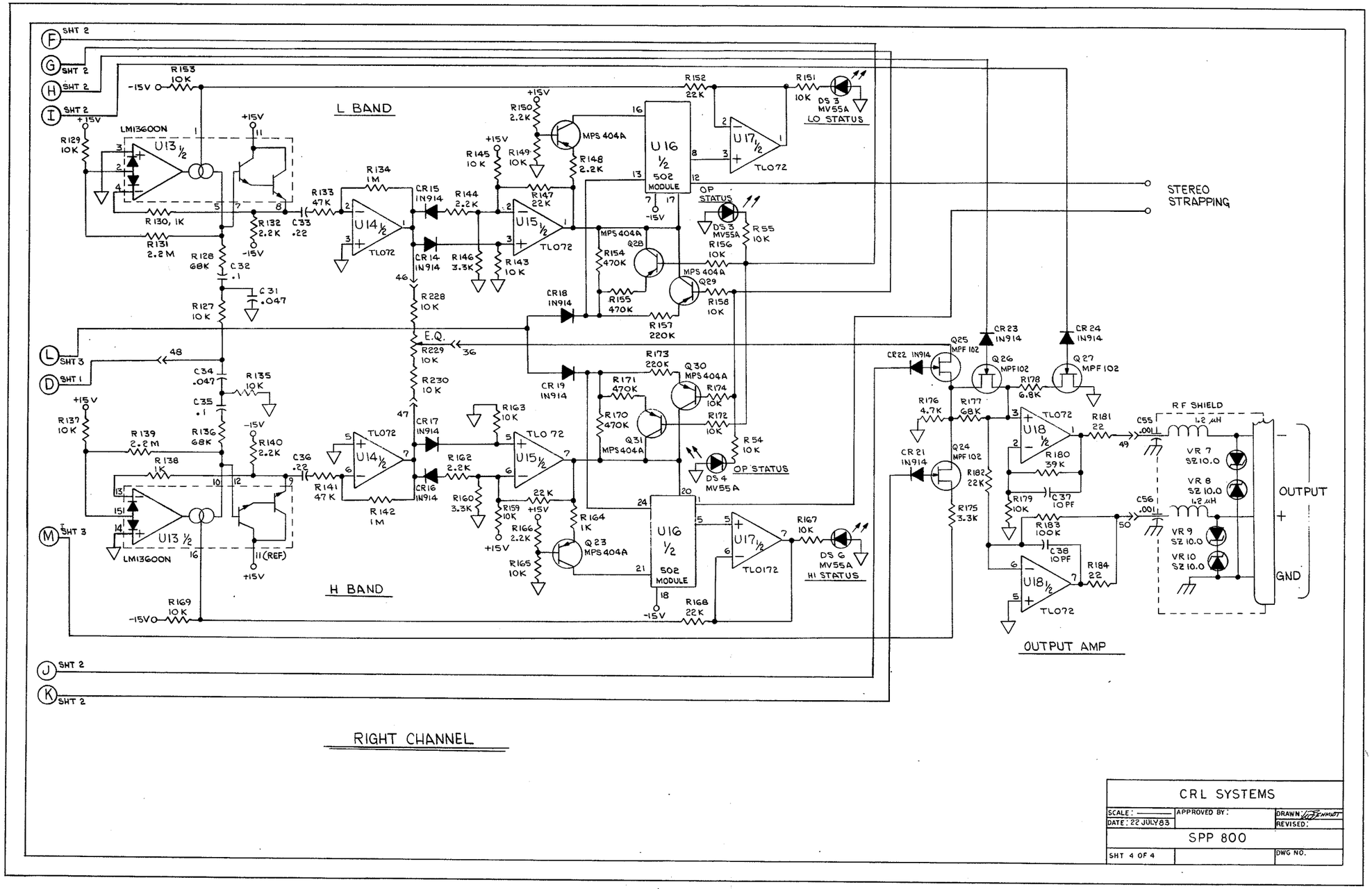
C63 .047
R185 6.8K
R207 100K
U8 ½ TL072
R186 100K
IN
OUT
SELECT PHASE PROCESSOR IN OR OUT
R222, 4.7K
R223, 2.7K
R224, 1.8K
R225, 1K
R226, 390
-3
-6
-9
-12
-15
S5 ½
G/R
R227 1K

LED DRIVERS/GATE CONTROL

CR20 IN914
R187 100
R188 22K
C39 2.2
+15V
R189 39K
R192 27K
Q35 MPS404A
R193 68K
C41 .01
R194 39K
Q36 2N4123
-15V
Q32 2N4125
R205 100K
Q33 2N4123
R190 100K
R191 22K
C40 .01
Q34 2N4125
R195 68K
R196 100K
Q37 MPS404A
Q38 2N4125
43
44
42
45
DS13 2190M96
INPUT CAL
DS19 2190M96
-15
DS11 2190M95
GATE OUT
DS17 2190M94
SHT 4 (L)

SHT 1 (C)
SHT 1 (N)
SHT 4 (M)
OVLD
41
DS15 2190M94

CRL SYSTEMS		
SCALE:	APPROVED BY:	DRAWN: BENNET
DATE: 22 JULY 83		REVISED:
SPP 800		
SHT 3 OF 4		DWG NO.


L BAND
H BAND
RIGHT CHANNEL
OUTPUT AMP
LM1360ON
TL072
MPS 404A
MPF 102
MV55A
STEREO STRAPPING
OP STATUS
LO STATUS
HI STATUS
E.Q.
RF SHIELD
OUTPUT
GND
SHT 2
SHT 3
SHT 1
-15V
+15V
U13 ½
U14 ½
U15 ½
U16 ½ 502 MODULE
U17 ½
U18 ½
R153 10K
R129 10K
R130, 1K
R131 2.2M
R132 2.2K
R133 47K
R134 1M
R135 10K
R137 10K
R138 1K
R139 2.2M
R140 2.2K
R141 47K
R142 1M
R143 10K
R144 2.2K
R145 10K
R146 3.3K
R147 22K
R148 2.2K
R149 10K
R150 2.2K
R151 10K
R152 22K
R154 470K
R155 470K
R156 10K
R157 220K
R158 10K
R159 10K
R160 3.3K
R162 2.2K
R163 10K
R164 1K
R165 10K
R166 2.2K
R167 10K
R168 22K
R169 10K
R170 470K
R171 470K
R172 10K
R173 220K
R174 10K
R176 4.7K
R177 68K
R178 6.8K
R179 10K
R180 39K
R181 22
R182 22K
R183 100K
R184 22
R228 10K
R229 10K
R230 10K
C31 .047
C32 .1
C33 .22
C34 .047
C35 .1
C36 .22
C37 10PF
C38 10PF
C55 .001
C56 .001
1.2 µH
CR14 IN914
CR15 IN914
CR16 IN914
CR17 IN914
CR18 IN914
CR19 IN914
CR21 IN914
CR22 IN914
CR23 IN914
CR24 IN914
Q23 MPS404A
Q24 MPF 102
Q25 MPF 102
Q26 MPF102
Q27 MPF 102
Q28 MPS 404A
Q29 MPS 404A
Q30 MPS 404A
Q31 MPS404A
DS 3 MV55A
DS 4 MV55A
DS 5 MV55A
DS 6 MV55A
VR 7 SZ 10.0
VR 8 SZ 10.0
VR 9 SZ 10.0
VR 10 SZ 10.0
R 54 10K
R55 10K
46
47
48
49
50
36
22K
CRL SYSTEMS
SCALE:
DATE: 22 JULY 83
APPROVED BY:
DRAWN
REVISED:
SPP 800
SHT 4 OF 4
DWG NO.