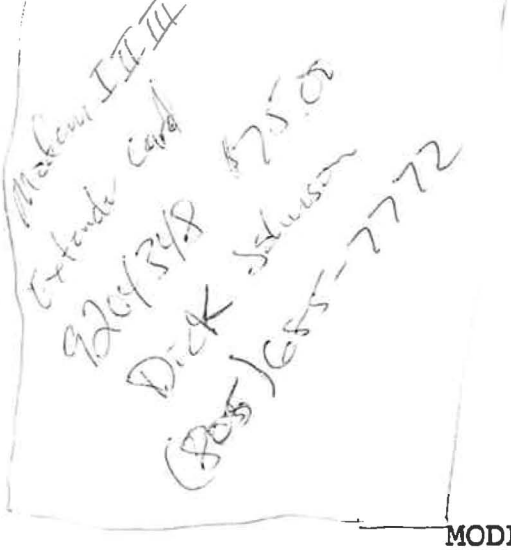

INSTRUCTION MANUAL

MODEL MRC-1 MICROPROCESSOR
REMOTE CONTROL SYSTEM

REMOTE TERMINAL

MOSELEY ASSOCIATES, INC.
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Rev. 9 June 1980

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WARNING

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instruction manual, may cause interference to radio communications. As temporarily permitted by regulation it has not been tested for compliance with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user, at his own expense will be required to take whatever measures may be required to correct the interference.

1 January 1981

1.0 SYSTEM INTRODUCTION

1.1 INTRODUCTION

The MRC-1 Microprocessor Remote Control System is a modular solid-state microprocessor-based system designed to meet the needs of the broadcaster to obtain remote indications of analog and status information, and to provide remote control of his equipment.

The MRC-1 consolidates, into one convenient package, all the features of existing moderately-priced remote control systems that require numerous auxiliary devices to function as a system in addition to many features normally found in large-scale remote control systems. The many features incorporated into the MRC-1 are made possible through the use of a microprocessor as the main control and logic element of each Remote and Control Terminal.

The flexibility of the microprocessor has also led to some changes in the terminology that is used to describe the functions performed by the MRC-1 and the way it is connected as a system. It is highly recommended that personnel installing an MRC-1 for the first time completely read and understand the manual before attempting to connect the MRC-1 to the user's equipment. There are two separate manuals for a complete MRC-1 system. One manual is for the Control Terminal; the second manual for the Remote Terminal.

1.1.1 Manual Organization

This manual has been designed to guide the user through the many features of the MRC-1 in a logical manner. Following the system specifications and unpacking instructions, Section 4 defines the operation of the Remote and Control Terminals. Once the operation of the system is mastered, Section 5 describes how to connect the MRC-1 to equipment being monitored and controlled. Section 6 defines the adjustment and calibration of the unit. Section 7 is a guide to maintenance of equipment should any difficulties be encountered. Section 8 contains circuit card descriptions, schematics and illustrations organized by type of circuit card. The last section will contain data for any options that were ordered as a part of the system. Should options be ordered at some future time, the option data may be appended to this manual by the user.

1.1.2 Technician Safety

The compact and modular design of the MRC-1, with convenient access to all modules and wiring, dictates that, from a safety standpoint, no lethal voltages be accidentally accessible to the technician. With the exception of the AC mains, which are made difficult to access, all internal voltages are less than 15 volts in magnitude. The user-applied voltages are limited to a maximum of 48 volts at any terminal (generally less) so that, when performing normal maintenance on the equipment, no lethal voltages are present inside the chassis. All high-voltage power switching and control must be performed indirectly by equipment external to the MRC-1.

1.2 SYSTEM OVERVIEW

An MRC-1 system consists of a Control Terminal and from one to nine Remote Terminals. Each Remote Terminal may access up to

32 status inputs (ON/OFF), 32 telemetry inputs (analog), and up to 64 command outputs (ON/OFF).

The Control Terminal communicates with each of the Remote Terminals over a single communications circuit that connects all locations. The communication circuit may be either 2-wire or 4-wire (or equivalent) telephone lines, STL subcarrier, aural SCA or private radio/ microwave links. Figure 1-1 is a typical illustration of the Control Terminal connected to several Remote Terminals.

In operation, one of the remote sites is selected for display at the Control Terminal. The value of each of the 32 status inputs is displayed on a set of 32 LED's. Calibrated analog values are digitally displayed one at a time. A CHANNEL SELECT key is used to display the desired channel.

The Remote Terminals perform seven (7) basic functions:

1. The remote keyboards are used to set up the system. When the system is installed, calibration data, alarm criteria, and so forth, are entered at each Remote Terminal keyboard. These may be changed from the remote keyboards during operation.
2. Once the system has been set up, the Remote Terminals process the incoming data according to the details of how the system was set up. The necessary computations for calibration, alarm checking, etc., are performed at the Remote Terminals.
3. The Remote Terminals process and transmit data, and turn ON and OFF the command output lines as instructed by the operator activating the Control Terminal.

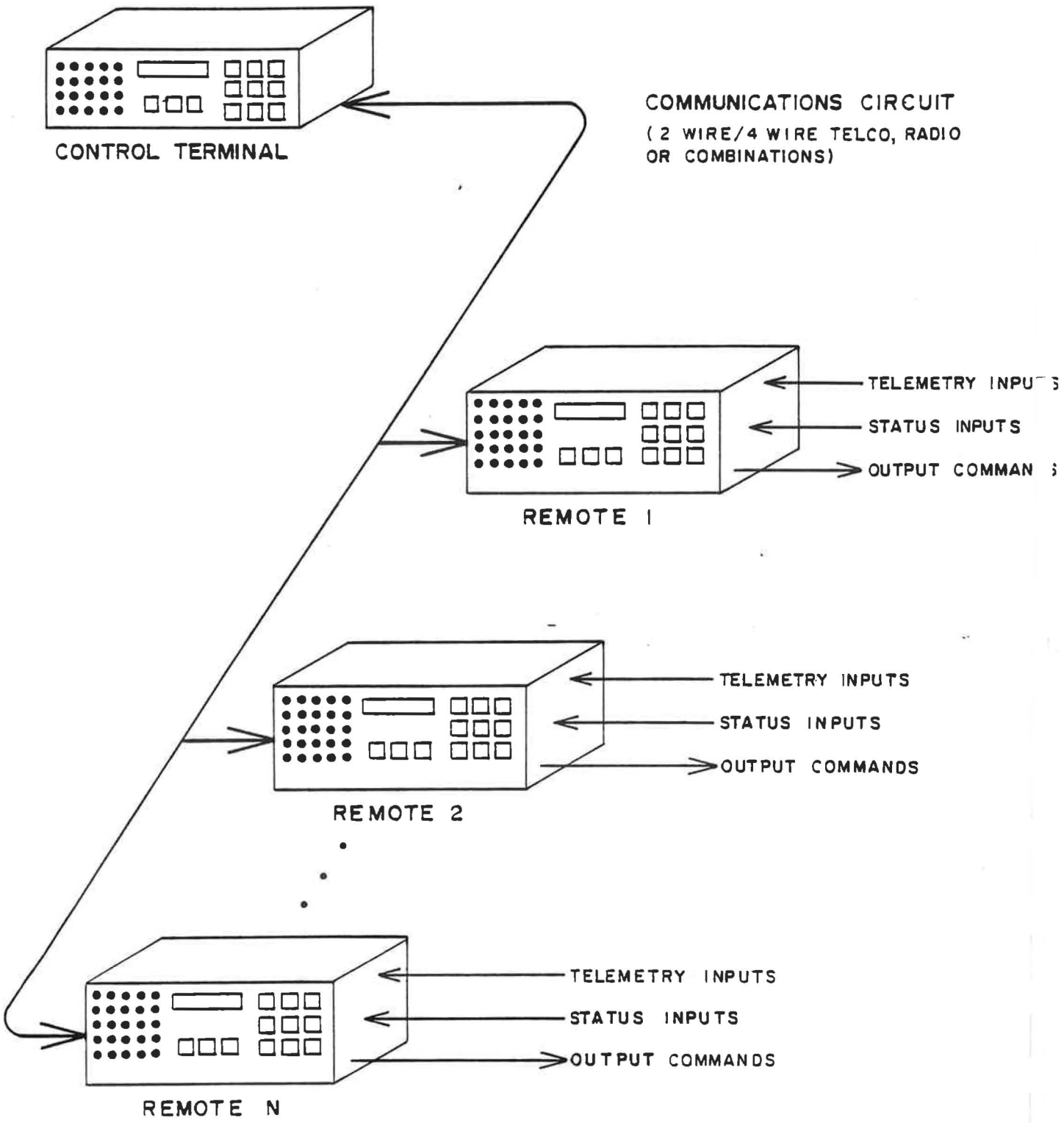


FIGURE 1-1

TYPICAL MRC-1 SYSTEM INTERCONNECT

4. The Remote Terminals check for alarms and notify the Control Terminal should an alarm condition be found.

5. If desired, a remote site may be operated directly from its own front panel, if it is placed in MAINTENANCE OVERRIDE mode.

6. The Remote Terminals provide a fail-safe output as required in broadcast applications.

7. The Remote Terminals continually monitor changes in their individual conditions (e.g., with temperature) and make slight adjustments in calibration calculations as required.

The Control Terminal is specialized to communicate with the various Remote Terminals, requesting display information and processing alarm reports as required. The Control Terminal prepares messages to the various Remote Terminals according to the actions of the user.

Much of the power of the MRC-1 is due to the flexibility available to the user in setting up the system. Specifically:

1. Telemetry (analog) channels may be calibrated in three ways:
   a. Directly proportional to input level (linear calibration)
   b. Proportional to the square of the input level (power calibration)
   c. Proportional to the product of two telemetry (analog) inputs (indirect calibration)

2. Each of these calibrated telemetry (analog) channels may have an upper and lower limit. If these limits have been established, the input is sampled, adjusted

according to calibration, and compared against the limits. Any violation causes an alarm.

3. Each of the individual status inputs may be given attributes causing them to "latch" or be inverted before display. Each status input may be set up to trigger an alarm, either on rising edge or falling edge (or both).

4. Any command output may be assigned to either the RAISE or LOWER key for any specified channel. "Latching" command lines also may be specified, in which case, pushing RAISE turns the command output ON, and pushing LOWER turns it OFF.

5. Telemetry inputs may be assigned "Mute" status inputs. If the "Mute" status input is ON, the telemetry data is displayed and limit-checked normally. If the "Mute" status input is OFF, limit checking is suppressed.

2.0 SYSTEM SPECIFICATIONS

2.1 INTRODUCTION

The MRC-1, as a system, can accommodate a wide variety of options with regard to interfacing the system to the user's equipment. The specifications for each interface, in addition to system specifications, are detailed in this section.

2.2 SYSTEM SPECIFICATIONS

The following are general system specifications for the MRC-1:

Type of System	Microprocessor-based Control and Remote Terminals.
Number of Control Terminals Per System	One (1) Control Terminal active in a system at a time
Number of Remote Terminals	One (1) to nine (9) Remote Terminals in a system
Failsafe:	
Control	Complies with current FCC requirements for AM, FM and TV service. Responds 45 seconds after failure of interconnecting circuit.
Telemetry	Internal timers and monitors for FCC TV compliance
Output	N.C. transistor closure at 48V, 100 mA
Alarm Indications	Visual and aural. Aural alarm defeatable and remoteable.
Maintenance Override	Remote Terminal front-panel control provides Remote Terminal "GO HOME" transistor closure and Control Terminal indication. N.O. transistor at 48V, 100mA, isolated.

Interconnect

Interconnect Classes	2-wire, 4- wire, FM subcarrier, or combinations
2-Wire/4-Wire	Nominal 600Ω balanced line. Series 3002 (unconditioned) data channel per Bell System Technical Reference PUB-41004. Two-way non-simultaneous. Nominal send level 0 dBm; receive level -30 dBm minimum
FM Subcarrier (Optimal)	Nominal levels 1.5V p-p at 2kΩ. Frequency range 26 kHz to 185 kHz
Modulation	Two-tone FSK; 1200 Hz idle, 2200 Hz mark frequencies
Data Rate	1200 bits per second
Data Format	10 bits, 7-bit ASCII plus parity, start, stop bits
Data Checking	Parity by character, longitudinal redundancy check and fixed formats

Command Functions

Number of Command Lines	16, 32, 48 or 64 lines per Remote Terminal
Command Line Modes	Each line programmable by user for momentary or latching operation
Command Line Association	Each momentary programmed line is user-assignable to one or more telemetry channels. Each latching line is assignable to one telemetry channel.
Tally-Back	Front-panel LED indicators at Remote and Control Terminals
Response Time	250 ms, nominal

Status Functions

Number of Channels	16 or 32 channels per Remote Terminal

States	User-programmable for N.O./N.C. activating front-panel LED's
Attributes	Latching or Following Alarm on rising, falling, or both conditions (or no alarm)
Response Time	250 ms, nominal, per site, from status change at Remote Terminal to Control Terminal indication.

Telemetry Functions

Number of Channels	16 or 32 channels per Remote Terminal
Calibration	Via keyboard at Remote Terminal in user-selected units of measure
Calibration Modes	Linear, power-to-linear, and indirect power calculation
Display	4 digits with decimal point and polarity sign for value and limits display
Alarms	Fully tolerance-alarmed for high and/or low limits
Muting	User-assignable status channel to cause alarm muting
Input Filtering	Digital two-pole filter
Display Response Time	500 ms, nominal, from request at Control Terminal
Self Check	A self-calibration cycle performed at approximately 4-second intervals

Physical Specifications

Power:	
Standard Control	120/240 VAC 50/60 Hz, 50 watts, nominal
Remote & Expanded Control	120/240 VAC 50/60 Hz, 100 watts, nominal

Size:	
Standard Control	13.3 cm H x 48.3 cm W x 38.1 cm D (5.25" H x 19" W x 15" D) Depth less connectors
Remote & Expanded Control	17.8 cm H x 48.3 cm W x 39.4 cm D (7" H x 19" W x 15.5" D) Depth less battery or connectors
Operating Temperature	0° - 50°C

2.3 ANALOG-TO-DIGITAL CONVERTER MODULE

The following specifications apply to the analog-to-digital (A/D) converter assembly supplied as a part of the system:

Channels	16 channels per module, 2 modules (maximum) per Remote Terminal
Resolution	One part in 1024
Inputs	Double-ended ±3.5 volts nominal, 100k DC bridging
Maximum Input	±5.0 volts. Application of voltage above this level causes erratic operation of one or more channels. Damage level is ±40 volts.
Sample Interval	A channel is sampled more than twice a second, regardless of the number of channels in the Remote Terminal.
Overall Measurement Accuracy	Better than 0.5%

2.4 TTL STATUS INPUT MODULE

The following specifications apply to the TTL Status Input Module supplied in the MRC-1 system:

Number of Channels	16 per module, 2 modules (maximum) per Remote Terminal

Input Configuration	Low-power TTL with 10k pull-up to +5 volts DC	
Voltage Reference	Chassis signal ground	
Maximum Input Voltage	+5.5 volts DC	Contact closure to ground will operate circuit
Minimum Input Voltage	0.0 volts	
Logic High Level Input Voltage	Greater than 2.0 volts	
Logic Low Level Input Voltage	Less than 0.8 volts	
Short Circuit Output Current	Less than 1.0 ma	

2.5 OPTICALLY-ISOLATED STATUS INPUT MODULE

The following specifications apply to the Optically-Isolated Status Input Module that can be interchanged with the TTL Status Module. Both module types may be mixed within a single Remote Terminal:

Number of Channels	16 per module, 2 modules (maximum) per Remote Terminal
Input Configuration	LED optical isolator
Voltage Reference	Two-terminal isolated from reference
Maximum Input Current	30 ma maximum through optical isolator, user-supplied current. User-changeable current limiting resistors
Maximum Voltage	±50 volts above chassis ground

2.6 OPEN COLLECTOR COMMAND OUTPUT MODULE

The Open Collector Command Output Module is supplied in an MRC-1 system for activating external devices:

Number of Outputs	16 command outputs per module, 4 modules (maximum) per Remote Terminal
Output Configuration	High current peripheral driver integrated circuit
Voltage Reference	Chassis signal ground
Maximum Voltage	48 volts DC, user-supplied
Maximum Current	250 ma, user-supplied
Voltage Drop (250 ma)	1.5 volts

2.7 OPTICALLY-ISOLATED COMMAND OUTPUT MODULE

The Optically-Isolated Command Output Module can be interchanged with the Open Collector Output Module for activating external devices:

Number of Outputs	16 command output per module; 4 modules (maximum) per Remote Terminal
Output Configuration	Optical isolator driving high-current Darlington
Voltage Reference	Two-terminal
Maximum Voltage	48 volts DC between terminals, user-supplied
Maximum Current	250 ma, user-supplied
Voltage Drop (250 ma)	1.5 volts

3.0 UNPACKING AND PRE-INSTALLATION CHECKOUT

3.1 UNPACKING

Upon removing the units from the shipping cartons, please inspect them carefully for internal and external damage that may have occurred during transit. Verify that all printed circuit cards are seated firmly in the mother boards. All cards are the same length and all should appear to be seated in the card cage to the same depth.

An instruction manual - Control Terminal or Remote Terminal - is shipped with each unit. There is some terminology that is used to describe the location of components on the PC boards within the card cages. The cards in a Standard Control Terminal are mounted horizontally (component side up) while those in a Remote Terminal or expanded Control Terminal are mounted vertically (component side to the right). The location of the components, i.e., LED's, test points, and switches are always given as if the cards were mounted vertically. The top edge of a card in a Standard Control Terminal is the left-hand edge; the bottom the right side.

Initial checkout of certain options, such as the LOGGER and POWER FAIL/MEMORY are covered in the documentation supplied with the option and presumes that the basic unit pre-installation checks have been performed. All units are checked out as a total system, as ordered.

The main purpose of pre-installation checkout is for the user to gain familiarity with the system while both the Control and

Remote Terminals are easily accessible and together on a bench at the same location. It is recommended that the user read the entire manual to understand the MRC-1 prior to attempting a hookup to his equipment. While the installation is relatively simple and straightforward, certain details of installation and operation, if overlooked, may cause what appear to be equipment failures.

3.2 POWER SUPPLY SHIPPING HOLDDOWN

A shipping screw is provided to hold down the power supply during transit. The screw is located on the left-hand side of the bottom chassis plate near the rear. Removal of the shipping screw prior to installation of the equipment into the rack will allow removal of the power supply assembly for servicing without removing the entire chassis from the rack.

> **CAUTION**
>
> WHENEVER THE UNIT IS SHIPPED, THE SHIPPING SCREW MUST BE INSTALLED AND SECURELY FASTENED. FAILURE TO OBSERVE THIS PRECAUTION CAN RESULT IN PHYSICAL DAMAGE TO THE UNIT AND VOIDS ALL WARRANTIES IF SHIPPED WITHOUT THE SCREW.

The shipping screw should be saved and taping the screw to the chassis for any possible shipment is encouraged.

3.3 PRE-INSTALLATION CHECKOUT

The following procedures apply to checking the Control and Remote Terminals on a stand-alone basis upon receipt of the units.

1. Verify that the power line voltage selector and fuse are set for the line voltage to be applied to the unit. The voltage selector is located

at the left rear of the chassis. The units are shipped for 120 VAC operation, unless otherwise specified. The voltage selected can be observed on the PC card through the window in the AC power connector. To change the voltage, remove the power cord, slide the access window to the left, and with small needle-nose pliers, grasp and remove the PC card. Orient the card for proper operation - either 120 VAC or 220 VAC only - and firmly replace the PC card. Install the proper fuse for the applied voltage as indicated by the placard on the AC mains connector. Slide the window to the right and install the AC mains connector.

2. Install the backup battery, provided only with the Remote Terminal. Connect the plus terminal of the battery to the red terminal of the CPU I/O connector and the negative to the black terminal of the CPU I/O connector. Batteries are shipped disconnected to prevent complete discharging.

3. Open the front panel by turning the knurled screw on the right side of the panel counterclockwise until the fastener disconnects and the panel can be swung open.

4. Connect the AC power connector to the AC mains. Depress the "ACK" key on the Remote Terminal front panel in order to clear the "cold start" condition which occurs whenever the Remote Terminal is powered up after the contents of memory have been lost.

5. Observe that the three upper LEDs on the CPU board - the bottom slot of the card cage - are ON.

These three LED's monitor the +15, +5 and -15 volt power supplies and are illuminated when there is voltage present.

6. Depress the "Reset" switch on the CPU board. Observe that the single LED near the switch illuminates while the switch is depressed and, for a short period, after the switch is released.

7. Observe the top LED on the modem PC board. It should turn ON and OFF at a periodic rate indicating that the Control Terminal is attempting to communicate with Remote Terminals.

8. Depress the LAMP TEST key. All LED's and displays on the Terminal should illuminate. A second depression of the LAMP TEST key will restore all LED's and displays.

9. This concludes initial checkout. Note that after six seconds an alarm condition will be indicated at the Control Terminal by a flashing "DATA ERROR" LED because of the failure to communicate with a Remote Terminal."

3.4 PRE-INSTALLATION SYSTEM CHECKOUT

Follow the individual checkout procedures for the Control Terminal and each Remote Terminal supplied as part of a system.

The Remote and Control Terminals should be connected back-to-back to verify communications according to the type of communications board supplied.

A. Modem Telco Interface

When telephone lines are used for communication in both directions, this board will be supplied for the Remote and Control Terminals. Two modes of operation are possible; two-wire or four-wire. In the two-wire mode, one telephone pair carries both Remote and Control message transmissions. In the four-wire mode, the Remote and Control Terminal messages are transmitted on separate telephone pairs, giving slightly better noise immunity. Figure 3-1A shows two-wire interconnection techniques. Figure 3-1B shows four-wire interconnection.

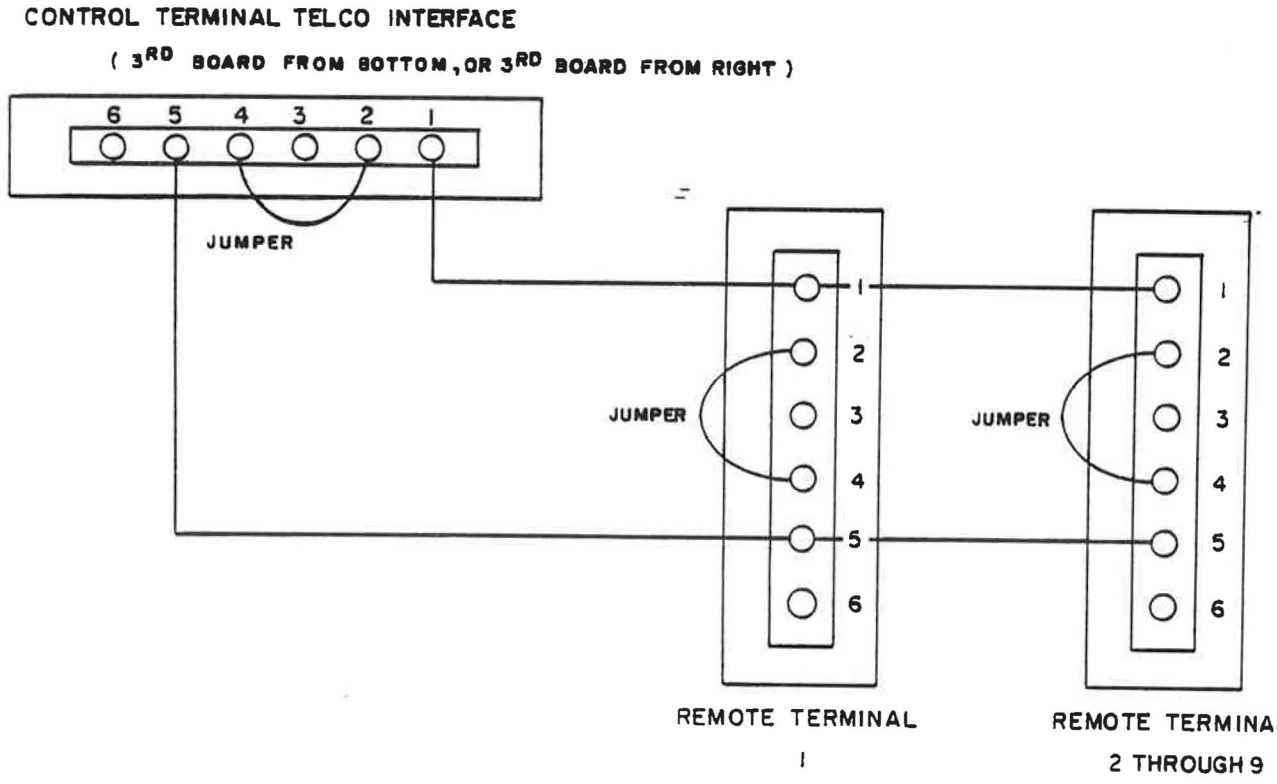


FIG. 3-1A

TWO-WIRE TELEPHONE LINE INTERCONNECTIONS

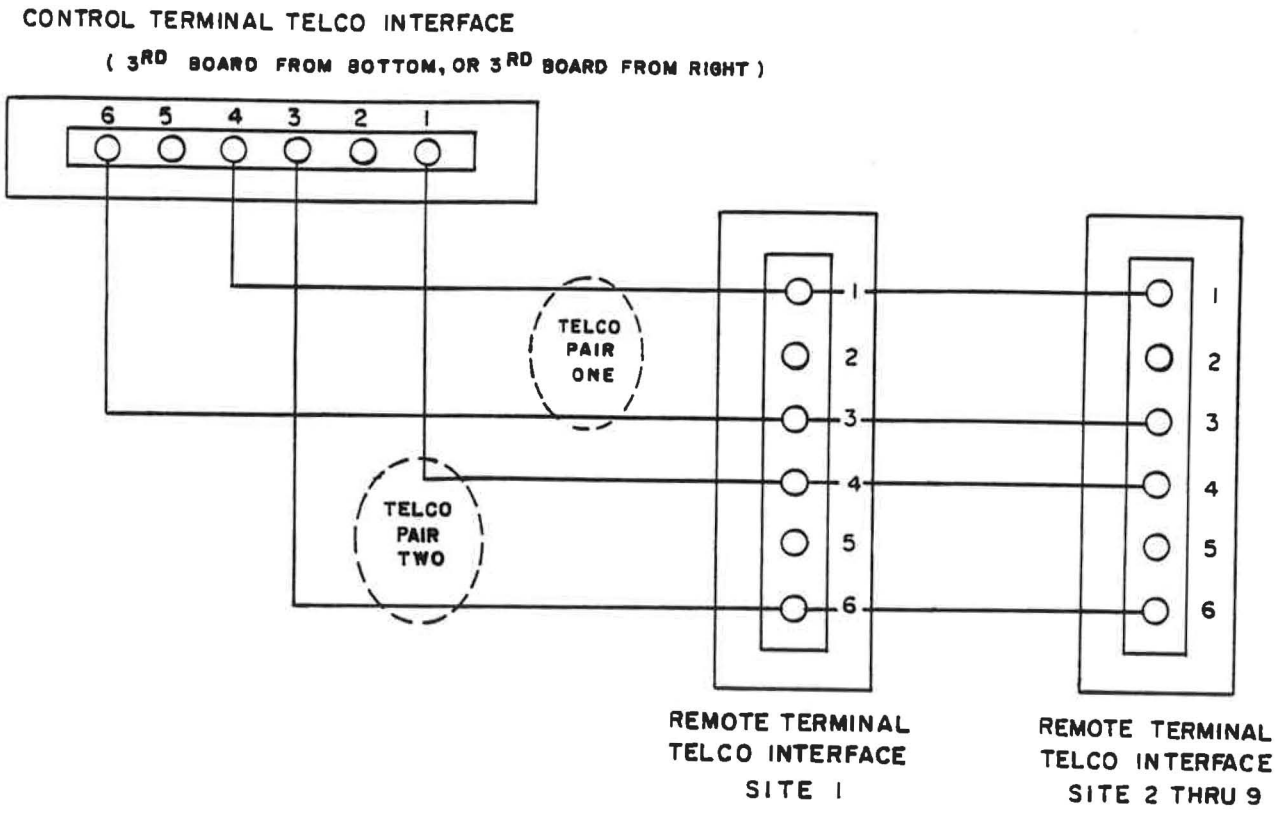


FIG 3-1B

FOUR-WIRE TELCO INTERFACE

After the units are interconnected, measure the output levels and modem input level and adjust, if necessary, as described in Section 6 of this manual. These levels should be checked again when the unit is installed at the final location. Adjusting these controls, taking into consideration actual telco line loss, will greatly improve communications reliability.

B. Subcarrier Interface

When FM subcarriers are used for data in both directions, this board will be supplied. Interconnection is quite simple. Using two BNC-to-BNC connector cables, interconnect units as shown in Fig. 3-2.

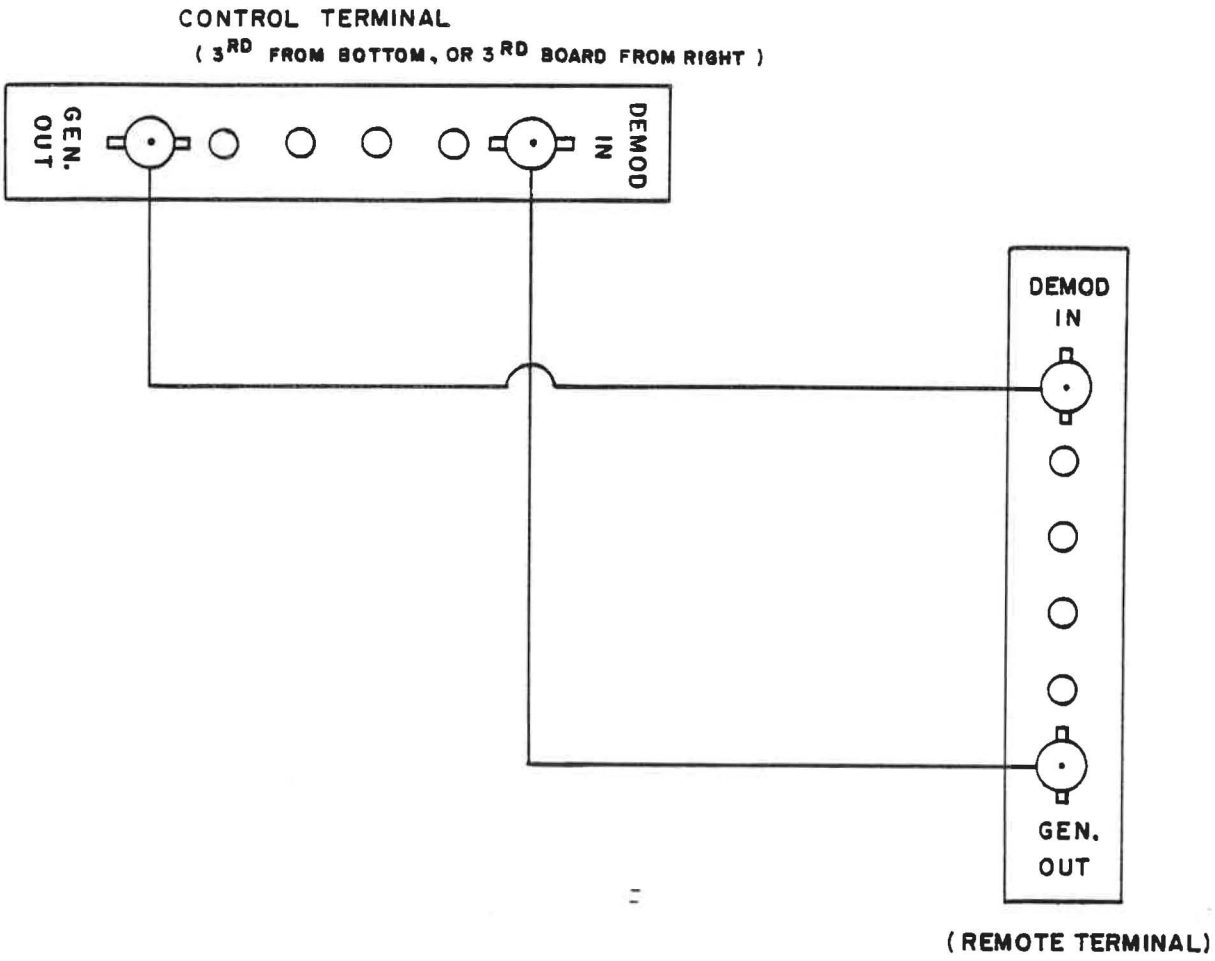


FIG. 3-2

DUAL SUBCARRIER COMMUNICATIONS

C. Subcarrier/Telco Interfaces

When one communication direction is on telephone lines and the other direction is on an FM subcarrier, a combination telephone/ subcarrier board is used at each end. Interconnection is shown in Fig. 3-3.

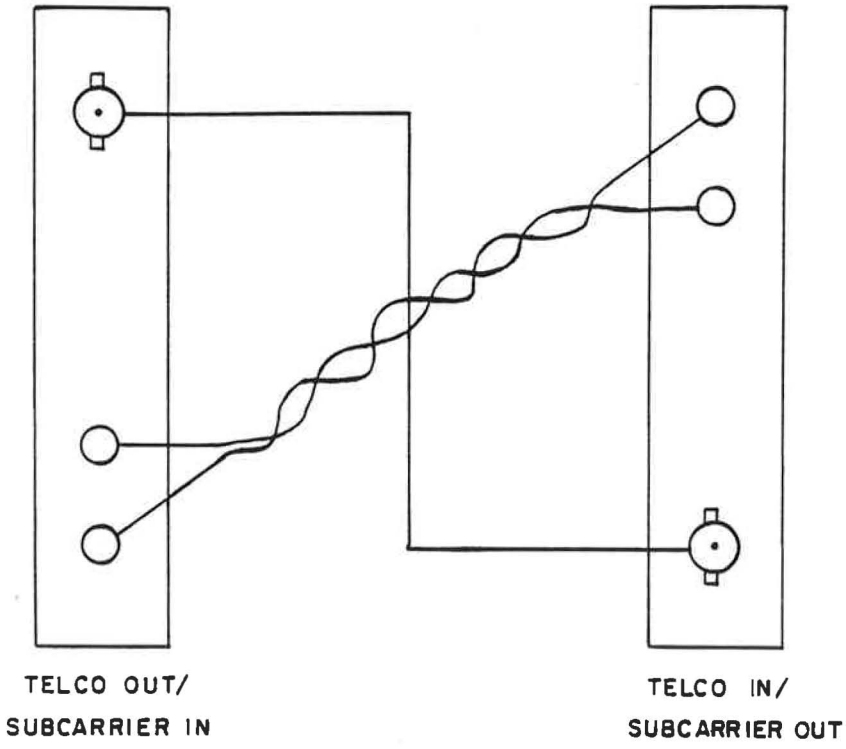


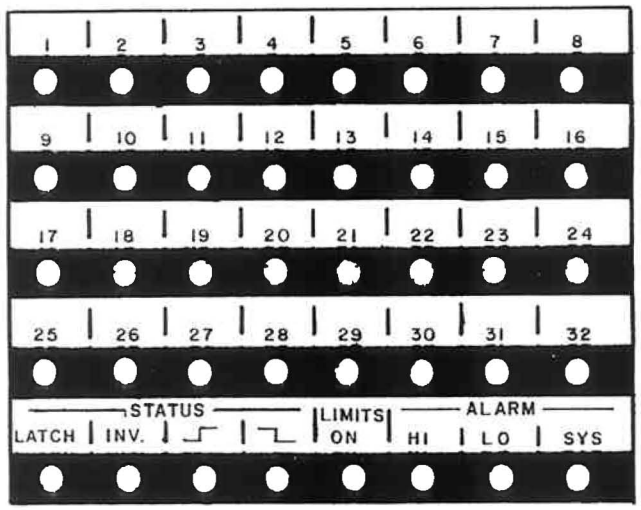
FIG. 3-3

TELCO / SUBCARRIER COMMUNICATIONS

The user may now connect test inputs to status and telemetry I/O interface and loads to control outputs as desired.

Referring to Section 4 of the Remote Terminal manual, telemetry channels that have inputs may be calibrated. Status channels (with or without input connections) may be programmed. Exercising the MAP function, the effect of commands to RAISE and LOWER may be observed.

In the event that any difficulty is encountered, review thoroughly Sections 4 through 7 to determine the cause of the difficulty. Refer especially to Section 8 for wireline modem or subcarrier modem adjustments.



MICROPROCESSOR REMOTE CONTROL MODEL MRC-I

SITE CHANNEL VALUE / EDIT

MOSELEY ASSOCIATES INC.

MAINT O'RIDE LAMP TEST ACK RAISE/ON LOWER/OFF

REMOTE TERMINAL

7	8	9	MAP ·	STAT CLR —
4	5	6	POWER LIM	LATCH INV
1	2	3	UPPER LIM LOW LIN	
SITE	0	CH	MUTE LIMS	SHFT

CHANNEL INDEX							
1	5	9	13	17	21	25	29
2	6	10	14	18	22	26	30
3	7	11	15	19	23	27	31
4	8	12	16	20	24	29	32

FIGURE 4-1

4.0 REMOTE TERMINAL OPERATION

4.1 INTRODUCTION

This section defines the operation of the Remote Terminal from the operator's view point. A detailed description of each key and its effect on the operation of the MRC-1 Remote Terminal is presented. Once familiarity is gained with the system, reference can be made to the last part of this section where a brief summary of the key operation is given.

4.1.1 Front-Panel Controls and Indications

Referring to an actual Remote Terminal or Figure 4.1, the front panel of the Remote Terminal contains the following.

A. Numeric Displays

   1. Site (1 digit)
   2. Channel (2 digits)
   3. Value/Edit (4 digits + sign)

B. LED Displays

   1. Status Indicators (32 LED's)
   2. Status Attribute Indicators (4 LED's)
   3. Alarm Indicators (3 LED's)
   4. System Indicators (4 LED's)

C. Audible Alarm

D. Keyboard

   1. Value Entry Keys
   2. Shift Key
   3. Function Keys
      A. "CH"
      B. "SITE"

C. "LATCH", "INVERT", "⎍⎺", "⎺⎍", and "STAT CLR"

D. "LIN" and "POWER"

E. "HI LIM" and "LO LIM"

F. "LIMS"

G. "MAP", "RAISE", and "LOWER"

H. "MUTE"

I. "ACK" (ACKNOWLEDGE)

J. "LAMP TEST"

K. "MAINT O'RIDE"

L. FAILSAFE FUNCTIONS

Each of these will be described in turn.

4.1.2 Numeric Displays

The numeric (7-segment) displays at the Remote Terminal provide the following indications under the condition described:

A. SITE: The SITE display is a single-digit display indicating which site number has been assigned to a Remote Terminal. In an MRC-1 System which consists of a Control Terminal and one to nine Remote Terminals, each remote must be given a unique site number. If two remote terminals have the same site number, both will respond at once when the Control Terminal attempts to communicate with the duplicated site number, and neither will be able to send back data successfully. The site number is automatically assigned according to strapping on the front-panel printed circuit board, and may be changed by using the site key (described in Section 4.5.2).

B. CHANNEL: The CHANNEL display is a two-digit display indicating which channel is selected. For example, if "01" appears in the channel display, Telemetry Channel 1 may be calibrated, assigned limits, assigned command outputs, raised, lowered, etc. If

Telemetry Channel 1 has already been calibrated, its current value will appear in the value-edit display.

C. VALUE-EDIT: The VALUE-EDIT display consists of four digits plus sign. It serves two functions: To display values currently being entered in command key sequences, or if no command sequence is being entered the current value of the selected telemetry channel.

While a key sequence is being entered the numeric keys activated are displayed, with each new digit entered pushing previously entered digits to the left. If more than four digits are entered only the last four digits entered are significant, the remaining being lost. A decimal point in the left-most digit indicates that the shift key was activated. Entering a "-" sign as a part of the key sequence affects the sign portion of the display. At the end of a properly executed key sequence the user will see the results as described later in this section for each key sequence. Any error in the key sequence results in an "E" appearing in the display for two seconds whereupon the display returns to whatever was being displayed just prior to the key sequence.

When not displaying key sequences the value appearing in the display for the channel selected can have the following meanings:

1. If the channel is uncalibrated, the VALUE-EDIT display remains blank.
2. If the channel is in an overflow condition, a flashing "EEEE" will appear in the display. An overflow condition occurs when the telemetry (analog) value for the selected channel is too large to display as calibrated.

For example, if Telemetry Channel 1 is calibrated to display a value of "9000" for 2.0 volts applied, and 5.0 volts is then applied, the resulting value ("22500") will overflow

the four digits available, and "EEEE" will be displayed.

3. If more than about 6 volts is applied, the selected telemetry channel may be in a saturated condition, i.e., the analog-to-digital converter is operating beyond the range where it is accurate. In this case, a flashing "----" will appear in the display.
4. Otherwise, the current value of the telemetry channel as calibrated will be displayed.

4.1.3 LED Indications

There are four major groups of LED indications on the front panel to:

A. Indicate the user's status conditions;
B. Indicate how a selected status bit has been programmed;
C. Indicate system details, and;
D. To indicate system and tolerance alarms.

The functions of each group of LED indicators is as follows:

A. Status Indications

There are 32 red LED's displaying the current value of status channels 1-32. LED's are assigned to channels starting from upper left and proceeding across from left to right. Thus, the first row displays status channels 1-8; the second row displays 9-16; the third row 17-24; and the fourth row 25-32. An "ON" condition is displayed by a steadily lit LED, and an "OFF" condition by an unilluminated LED. If an alarm condition has occurred on a status channel and has not yet been acknowledged, the appropriate LED will flash at a 2 Hz rate. (Alarm conditions may be defined by the user; this and the procedure for acknowledgement will be described later.)

B. Status Programming

There are four green LED's indicating which attributes, if any, have been assigned to the selected status channel. The LED's are labeled "LATCH", "INVERT", "_|‾" (Rising edge alarm), and "‾|_" (Falling edge alarm). These attributes are selected and removed via key commands described in later paragraphs of this manual. The specific status bit selected and programming displayed in these LED's is indicated by the channel display.

C. System Details

There are four yellow LED's which indicates various details of the status of the system:

A. The "RAISE/ON" and "LOWER/OFF" LED's show the status of the user-assigned command outputs. If the command channels have been established as momentary in operation, each LED is lit if the assigned command output is "ON" and not lit if the command output is "OFF". For example, suppose channel 12 has been selected for display, with command output 3 established as the raise output, and command output 8 established as the lower output. Then the "RAISE/ON" LED will reflect the status of command output 3 and the "LOWER/OFF" LED that of command output 8.

   If a command output of latching type has been established instead, then the "RAISE/ON" light indicates that the command output is "ON" and the "LOWER/OFF" LED indicates that the channel is "OFF".

B. The LED labeled "LIMITS ON/OFF" is lit if limit checking is enabled.

C. The yellow LED positioned over the key labeled "MAINT O'RIDE" indicates whether the terminal is in maintenance

override status; the LED is illuminated if so. If the system is in Maintenance Override status, RAISE or LOWER commands issued from the Control Terminal will be ignored, and any failsafe condition will be terminated. If the system is not in Maintenance Override status, RAISE or LOWER command issued from the Remote Terminal keyboard will be ignored.

D. Tolerance Alarms

There are three red LED's which are used to indicate alarm conditions. Two of these, labeled "HI" and "LOW", are used to describe the current condition of the selected telemetry channel with respect to its limits. For example, if Channel 7 is being displayed and the current value of that channel, as calibrated, exceeds its upper limit, the "HI" LED will be lit (and flashing at 2 Hz if the alarm has not been acknowledged by pushing the "ACK" key). This, of course, is only if limit checking has been enabled.

Additionally, the LED labeled "SYS" describes the condition of the analog-to-digital conversion hardware. Each Remote Terminal, at approximately 4-second intervals, makes internal tests of various conditions, including the gain-reference and offset voltages. If any of these violate factory-set tolerances, the "SYS" LED is illuminated until the violation of tolerance ends.

4.1.4 Audible Alarm

Each front panel in an MRC-1 system is equipped with an audible alarm. The alarm will sound only if it is enabled via the rear-panel socket. At Remote Terminals, the alarm is used for two functions:

1. In case of a power failure where memory has not been preserved (or when starting the system for the first time), the alarm sounds to indicate the necessity to recalibrate

telemetry channels, re-assign attributes, re-enter limits, etc. (I.E., the user must reinitialize the terminal.) Pushing the Acknowledge key turns off the alarm and begins normal operation. Note that, even if the alarm is not enabled via the rear-panel socket, "ACK" must be pushed to begin normal operation.

2. If an unacknowledged alarm condition is found, the audible alarm indicates the presence of the alarm.

4.2 KEYBOARD INTRODUCTION

The MRC-1 Remote Terminal front panel has 20 keys, each with a function. A shift key is used to enable 11 additional functions. Operations on the front panel keyboard are quite similar to operations on a calculator.

The following abbreviations appear on the Remote Terminal keyboard:

Abbreviation	Meaning
STAT CLR	Status Clear
LIN	Calibrate - Linear
INV	Invert
HI LIM	Upper Limit
LO LIM	Lower Limit
_┘‾	Rising Edge Alarm
‾└_	Falling Edge Alarm
LIMS	Limits On/Off
SHFT	Shift
ACK	Acknowledge
MAINT O'RIDE	Maintenance Override

The MRC-1 is controlled by means of key sequences. If an erroneous or meaningless key sequence is entered, an "E" appears in the value/edit display for 2 seconds.

Examples of this:

1. "SHFT 9"

   Undefined - Causes "E"

2. "LIN"

   Attempt to calibrate telemetry channel without entering a value.

3. "1 Ø Ø Ø LIN"

   This is normally valid, but results in an "E" if an insufficient level is applied to the telemetry input at calibration time.

4.3 VALUE ENTRY KEYS

The value entry keys are the numeric keys Ø-9, the decimal point key ("."), and the minus sign key ("-"). Some MRC-1 functions, for example, calibrating telemetry channels, demand a value. Entry of values is made possible by the numeric, sign, and point keys. If a function requires a value, the value is entered before the function key is pushed. For example, to calibrate a telemetry channel at 1ØØØ in linear mode, push:

1 Ø Ø Ø LIN"

As the value is entered, it appears in the value/edit display. If a mistake is made, the value entered may be cleared by pushing the acknowledge ("ACK") Key. When "ACK" is pushed, or the sequence is

complete, the value/edit display returns to indicating the value or status of the selected telemetry channel as calibrated.

The sign key may be pushed at any time up to the final function key; for instance:

"- 1 Ø Ø Ø LIN" and "1 Ø Ø Ø - LIN"

have the same effect, both calibrating the selected telemetry channel in linear mode at -1ØØØ.

Decimal points are entered by pushing "." at the proper point in the key sequence, for instance:

"1 Ø . Ø Ø - LIN"

calibrates the selected telemetry channel in linear mode at -1Ø.ØØ.

If more than four number keys are pushed, only the last four will be used. The excess number keys are shifted off the left end of the value/edit display and are lost as new keys are pushed.

For example:

"- 1 2 3 . 4 1 Ø . Ø Ø LIN"

has the same effect as the example immediately preceding. Note that the sign is preserved during the entry.

4.4 SHIFT KEY

The shift key (at the lower right of the keypad) chooses the set of functions engraved on the metal part of the front panel rather than those inscribed on the keytops. The shift action is "Push-On/Push-Off" in nature, each push of the shift key reversing the set of functions selected.

The value/edit display visually indicates the presence or absence of a shift in a command line by a dot (similar in appearance to a

decimal point) at the far left end, to the left of the sign position.

Example to illustrate use of shift key:

"1 Ø Ø Ø SHFT LIN"

calibrates the selected telemetry channel at 1ØØØ in power mode, since "POWER" is engraved on the front panel above the "LIN" key. (This will henceforth be shown in the manual as:

"1 Ø Ø Ø SHFT POWER"

using the name of the actual function selected to avoid confusion.)

As further example:

"1 Ø Ø Ø SHFT SHFT LIN"

calibrates in linear mode since the first push of the shift key selects the "UPPER CASE" power function and the second push reselects the "LOWER CASE" linear calibrate function.

4.5 FUNCTION KEYS

Function keys are always the last keystroke in a key sequence - the effect of the key sequence takes place immediately when a function key is pushed. The various remote terminal functions that are performed by each function key is defined below.

4.5.1 "CH" Channel Key

The "CH" (Channel) key is used to change the selected channel. For example, entering:

"1 7 CH"

Makes 17 the selected channel. "17" will appear in the channel display, and if analog input 17 has been calibrated its current value

will appear in the value/edit window. Status Channel 17 may have its latch, invert, or alarm attributes changed. Where applicable, all key sequences will apply to Channel 17.

Pushing the "CH" key with no preceding value will advance the channel by one. Continuing the above example, if we then enter:

"CH"

we will advance to Channel 18. If the selected channel is 32 entering:

"CH"

will make 1 the selected channel.

4.5.2 SITE Key

The "SITE" key is used to assign a different site number to the remote terminal than the one set at the factory or programmed at the rear of the front panel. For example, entering:

"8 SITE"

will make the remote terminal respond as Site 8 rather than its factory-assigned site number. The control terminal will then select this terminal when Site 8 is selected for display. It should be stressed that each remote terminal should have a different site number. If there are two terminals set to the same site number, the system cannot operate.

In the event of a power failure where memory has not been preserved, the remote terminal will, of course, be re-initialized to its factory-assigned site number, regardless of previous use of the site key.

4.5.3 Latch, Invert, ¬_, _¬ Keys

The "LATCH", "INVERT", "¬_" (Falling Edge Alarm), and "_¬" (Rising Edge Alarm) functions are used to assign and remove attributes for selected status channels. Each of these functions is Push-On/Push-Off in nature. The first time the function is invoked the attribute is added, the second time it is removed, etc. The current status of each of these attributes for the selected channel is displayed on the corresponding green status LED's. For each of these functions, the status channel affected is the channel selected for display (as shown in the channel window).

The invert attribute reverses the external value applied to a status channel before it is displayed. If the external state of status Channel 1 is "OFF" and Channel 1 is assigned an invert attribute, the LED corresponding to status Channel 1 will be lit.

The latch attribute causes a status channel to remain in the "ON" condition after a rising edge (after inversion if applicable) is detected. Subsequent edges are disregarded. The status-clear function returns all latched channels to the "OFF" state until the next rising edge. Alarms and muting are invoked on the basis of status value as modified by latch and inversion.

The "¬_" (Falling Edge Alarm) attribute causes an alarm to occur if a falling edge is detected. Alarms are more fully described in the section describing the "ACKNOWLEDGE" function.

The "_¬" (Rising Edge Alarm) attribute causes an alarm to occur if a rising edge is detected. Note that if a channel has both "_¬" and "¬_" attributes, any edge at all will trigger an alarm.

Examples:

"INV"

reverses the current status of the invert attribute for the selected channel.

"SHFT LATCH"

reverses the latch attribute.

"⌐¬"

reverses the "⌐¬" attribute.

"SHFT ¬⌐"

reverses the "¬⌐" attribute.

"SHFT STAT CLR"

releases all latched status channel to the "OFF" state.

Numerical values preceding the function keys in these cases are meaningless, and such key sequences are rejected with an "E". For example:

"1 INV"

does not invert status Channel 1, but rather results in "E" being displayed for two seconds. If Channel 1 is to be inverted, Channel 1 should first be selected using the "CH"key.

4.5.4 "LIN", "POWER" Keys

The "LIN" (linear-calibration) and "POWER" functions are used to calibrate the selected telemetry channel. Linear calibration implies that a change in the external value results in a directly proportional change in the display. For example, if 3 volts are applied to telemetry input 1, and 1 is the selected channel, and

"1 Ø Ø LIN"

is entered, whenever 3 volts is again applied, "1ØØ" will be displayed. If 1.5 volt is applied, "5Ø" will be displayed, etc.

Power calibration is similar to linear calibration, but the change in displayed value changes as the square of the change in applied value. If 3 volts are applied as before, and

"1 Ø Ø SHFT POWER"

is entered, whenever 3 volts are applied, "1ØØ" will be displayed, just as above. But if 1.5 volt is applied, since the applied value has been halved (multiplied X .5), "25" is displayed (since the square of .5 is .25). Similarly, if 6 volts are applied, "4ØØ" is displayed.

"INDIRECT METHOD" calibration is also possible, by the convention of entering a negative initial value and choosing power calibration. (A negative number cannot be displayed in a power calibrated channel since no real number may be squared with the result a negative number.) "INDIRECT METHOD" calibration displays a result proportional to the values of the two preceding telemetry channels. For example, if we apply 3 volts to telemetry input 1 and 2 volts to telemetry input 2 and then select Channel 3 for display, and then enter:

"- 1 Ø Ø . Ø SHFT POWER"

Channel 3 will then be calibrated in "INDIRECT METHOD" mode. Whenever the product of levels applied to Channels 1 and 2 equals 6, 1ØØ.Ø" will be displayed. If we then apply 1 volt to each channel, the product is one sixth of what it was at calibration time, and so one sixth of 1ØØ.Ø, or 16.7 is displayed.

It is good practice to calibrate telemetry inputs with as large as possible a value applied to the input. It is better to apply 5 volts and calibrate than to apply 1 volt and calibrate. This is because analog-to-digital converters return an integer number, proportional to the level applied. So lower levels cause numbers with fewer significant digits to be returned. The calculations for calibration of necessity have a larger percentage error at low values.

For this reason, the MRC-1 will not permit calibration to be made with less than about 256 millivolts applied to the telemetry input. This insures an acceptable level of accuracy. (Better, normally much better, than Ø.5%.) An attempt to calibrate with an insufficiently large level results in "E" being displayed for 2 seconds.

4.5.5 LOW LIM, HI LIM Keys

Each telemetry channel may be assigned an upper lmit and a lower limit. If limit checking has been enabled and the telemetry channel as calibrated is found to violate one of the limits, an alarm is initiated.

Examples:

"1 Ø Ø Ø LOW LIM"

establishes 1ØØØ as the lower limit for the selected channel.

"1 Ø 5 Ø HI LIM"

establishes 1Ø5Ø as the upper limit for the selected channel. The limits may be displayed by omitting to enter the value. Continuing the preceding example, pushing:

"LOW LIM"

will display "1ØØØ for two seconds, and pushing

"SHFT HI LIM"

will display "1Ø5Ø for two seconds.

Once established, limits may be removed by entering Ø as the limit. Entering:

"Ø LOW LIM"

will remove any lower limit established for the selected channel. Similarly,

"Ø SHFT HI LIM"

will remove any upper limit.

If no limit has been established, "Ø" will be displayed as the limit when a display is requested.

This means, of course, that it is impossible to enter a limit of exactly zero, because the system interprets a limit of zero as no limit at all. This can be circumvented by entering a limit very close to zero. For example, entering:

". Ø Ø Ø 1 SHFT HI LIM"

makes a number very close to zero the upper limit, whereas entering:

"Ø SHFT HI LIM"

will make a "HIGH LIMIT ALARM" on the selected channel impossible, and is equivalent to no limit at all.

4.5.6 LIMS Key

Limit checking is enabled and disabled via the "LIMS" key. This key operates in a push-on/push-off manner, the first push enabling

limit checking, and the next push disabling limit checking. The current status is indicated by the "LIMITS ON" LED.

4.5.7 MAP Key

The MRC-1 Remote Terminal may administer up to 64 command outputs. To use these, each command output must first be associated with a channel. This process is called "MAPPING", and is normally done when the system is set up. Once "MAPPED", command outputs are activated by pushing the "RAISE" or "LOWER" keys while the appropriate channel is selected.

For example, suppose we select Channel 1Ø and enter:

"1 SHFT MAP RAISE"

("MAP" is the upper case of the "." key.) Then henceforth, whenever we select Channel 10 and push "RAISE", command output line "1" will be activated for as long as the key is pushed.

Now suppose we enter:

"2 SHFT MAP LOWER"

Similarly, whenever we select Channel 10 and push lower, command output "2" will be activated. Each channel may have two command outputs "MAPPED" to it in this manner. The mapping is removed by entering "Ø" as the command output number. Entering:

"Ø SHFT MAP RAISE"

will cause the "RAISE" key to have no effect. Likewise:

"Ø SHFT MAP LOWER"

will cause the "LOWER" key to become undefined.

Mapping may be displayed as follows: Entering:

"SHFT MAP RAISE"

will display the number of the command output that is assigned to the raise key, and:

"SHFT MAP LOWER"

will display the number of the command output that is assigned to the lower key. In cases where no mapping has been established, "Ø" will be displayed.

Above, we described momentary operation where pushing the "RAISE" or "LOWER" key causes a command output to be activated but only for as long as the key is pushed. Another mode is possible: "LATCHING" operation. In latching operation, one command output is assigned to a channel; pushing the "RAISE" key activates the command output to the on condition, and pushing the "LOWER" key turns the command output off.

Latching channels are established by specifying the same command output as both "RAISE" and "LOWER" outputs. For example, if we select Channel 11 and enter:

"3 SHFT MAP RAISE"

followed immediately by

"3 SHFT MAP LOWER"

then the command output 3 will be established as a latching command output for Channel 11.

As the final keystroke ("LOWER") is entered, the LED over the lower key is lit to indicating the latching channel is off. Pushing "RAISE" will turn the channel on and light the LED over the "RAISE" key.

Latching command channels are removed by entering Ø, exactly as is done for momentary channels. So:

"Ø SHFT MAP RAISE"

followed immediately by:

"Ø SHFT MAP LOWER"

will turn off the latching command output and will cause the "RAISE" and "LOWER" keys for the selected channel to again be undefined.

The above text has described the procedure to assign a command output channel. Command outputs that are used in the momentary mode may be assigned to more than one channel. This is particularly advantageous when a single control function - say a final amplifier controller - affects several measured parameters - plate voltage, plate current, and measured power output. If these parameters were assigned to Channels 6, 7, and 8 respectively, and command output 4 connected to cause the power controller to increase, with command output 5 causing a decrease, then you can assign the command output 4 and 5 to each of the Channels 6, 7, and 8. To complete key sequence to accomplish this assignment is:

```
6     CH
4     SHIFT MAP RAISE
5     SHIFT MAP LOWER
CH
4     SHIFT MAP RAISE
5     SHIFT MAP LOWER
CH
4     SHIFT MAP RAISE
5     SHIFT MAP LOWER
```

Then, regardless of which of the three channels is selected for display of the telemetry value, activating the RAISE or LOWER keys will cause the power controller to function appropriately.

4.5.8 MUTE Key

The "MUTE" function is used to enable and disable limit checking on the individual telemetry channels, under the control of a status input. Suppose we select Channel 9 and enter:

"3 Ø SHFT MUTE"

then, Status Channel 3Ø will control limit checking on telemetry Channel 9. Whenever Status Channel 3Ø (after latching and inversion, if specified) is OFF, limit checking on telemetry Channel 9 will cease.

When Status Channel 3Ø LED goes ON again (after latching and inversion, if specified), limit checking resumes after a four-second delay.

In this manner, any telemetry channel may have any status input assigned to it as a mute channel.

A mute channel may be removed by entering Ø instead of a valid status channel number; i.e., entering:

"Ø SHFT MUTE"

will cause the selected channel to have its mute assignment removed.

Mute assignments may be displayed by entering:

"SHFT MUTE"

If no mute assignment has been made for the selected channel, "Ø" will be displayed.

Note that it is possible to assign more than one telemetry channel to a single status input for muting purposes. All of the telemetry

channels for the main transmitter can be assigned to one status input that indicates the main transmitter is operational, and all telemetry channels for a backup transmitter assigned to a second status channel that indicates the backup transmitter is operational. Telemetry channel alarms will then only occur when the corresponding transmitter is operational. Depending upon how the status inputs are derived from the transmitter, you may want to have an alarm indicated by the change of state of the status channels themselves. I.E., it is possible through the use of the mute function and the manner in which the status used to operate the mute function to have a transmitter fail and no alarm indication. Because of the wide varity of transmitters in use, it is not possible to give specific details. The user must select his best method of incorporating this function.

4.5.9 ACK Key

The "ACK" (acknowledge) key is used to clear alarms. At the remote terminal, the following conditions cause alarms:

- A status channel with "falling edge" attribute experiences a falling edge.
- A status channel with "rising edge" attribute experiences a rising edge.
- An analog channel violates its lower limit.
- An analog channel violates its upper limit.
- The fail-safe time-out period has been intiated.
- The fail-safe time-out period has expired.

When an alarm occurs, the audible alarm sounds (if it has been enabled via the rear-panel socket) and the channel display flashes to indicate

the alarm. This will continue until "ACK" (acknowledge) is pushed.

Once "ACK" has been pushed, the system automatically selects the channel where the alarm condition was detected. (If several alarms have occurred, the channel where the first alarm occurred is selected.) The alarm-causing condition may now be observed on the indicator LED's as follows"

- o If a status alarm has occurred, the appropriate status LED will be flashing at 2 Hz.
- o If a telemetry input has gone below its upper limit, the "LOW" LED will be flashing at 2 Hz.
- o If a telemetry input has risen above its upper limit, the "HI" LED will be flashing at 2 Hz.

The second push of the "ACK" key clears the alarm, causing the flashing to end.

For example, suppose Channel 1Ø is selected when telemetry Channel 3 falls below its lower limit. First the audible alarm sounds if it has been enabled, and the channel display starts flashing to indicate the presence of the alarm. To examine the alarm, push "ACK". Then the sonalert is switched off and the system selects Channel 3. We see the "LOW ALARM" LED flashing at 2 Hz, indicating that the alarm arose because Channel 3 fell below its lower limit. Pushing "ACK" again causes "LOW ALARM" to cease flashing. If the low limit is still being violated, the LED will remain steadily on; if it has risen back within limits, the LED will go off.

Suppose a little later, status Channel 6, which has been given a falling edge alarm attribute, changes from "ON" to "OFF". Then the sonalert will again come on, and the channel display will again flash. After pushing "ACK", the audible alarm is switched off, the

system selects Channel 6, and the LED displaying Status Channel 6 may be observed flashing at 2 Hz. When "ACK" is pushed the second time, the flashing ceases.

To summarize, each alarm is cleared by pushing "ACK" twice. The first push turns off the audible alarm, changes channels, and displays the alarm condition via flashing lights. Acknowledged limit violations continue to be displayed via steadily-ON (not flashing) LED's, until the telemetry value has returned within limits (or limit checking is disabled, or mute status begins).

4.5.10 Lamp Test

The Lamp Test function tests the LED's and the seven-segment displays on the front panel. "LAMP TEST" is a push-on/push-off function - the first push begins the test; the second push ends it.

4.5.11 Maintenance Override

The Maintenance Override function is used to establish local control of the Remote Terminal. If the system is not in Maintenance Override mode, raise and lower commands from the Remote Terminal are disabled.

Conversely, if the system is in Maintenance Override mode, raise and lower commands from the Control Terminal are inhibited and any failsafe condition is discontinued.

Maintenance Override status is invoked and ended by the "MAINT O'RIDE" key. Current Maintenance Override status is indicated by the LED over the function key. If the system is in a Maintenance Override status, the LED will be lit.

4.6 FAILSAFE FUNCTIONS

MRC-1 Remote Terminals provide a "FAILSAFE" output as required in broadcast applications. The failsafe output is activated 45 seconds after signals from the Control Terminal cease ("CONTROL FAILSAFE"). The failsafe output is ended immediately on receipt of a valid message from the Control Terminal, or when maintenance override mode is entered.

In FCC television broadcasting applications, a second type of "FAILSAFE" output is required: If aural plate voltage, aural plate current, aural power output, or visual power output metering vanish for an one hour period, a failsafe output is required ("TELEMETRY FAILSAFE").

A telemetry failsafe is also required if the Remote Terminal is unable to communicate with the Control Terminal for an one hour period.

At the MRC-1 Remote Terminal, there is a single failsafe output which is activated for either or both types of failsafe.

"TELEMETRY" failsafe will occur only if certain key sequences activating it have been entered. These will be demonstrated by example:

Suppose Telemetry Input 13 is aural plate voltage, input 15 is aural plate current; input 17 is aural power output, and input 25 is visual power output. We may initiate failsafe monitoring of these four channels by the following four key sequences:

"1 3 SHFT 1"

This specifies that Telemetry Channel 13 shall be monitored as the first telemetry failsafe channel.

"1 5 SHFT 2"

This specifies that Telemetry Channel 15 shall be monitored as the second telemetry failsafe channel.

"1 7 SHFT 3"

This specifies that Telemetry Channel 17 shall be monitored as the third telemetry failsafe channel.

"2 5 SHFT 4"

This specifies that Telemetry Channel 25 shall be monitored as the fourth telemetry failsafe channel.

All four telemetry failsafe channels having been established, monitoring commences, and should less than about 256 mV be observed at any of the four specified telemetry inputs, the one-hour countdown will begin.

Telemetry failsafe channels may be removed and displayed in a manner exactly analogous to muting, limits or mapped commmand channels; therefore:

"Ø SHFT 1"

removes the first telemetry failsafe channel and ends failsafe monitoring. Similarly:

"Ø SHFT 2"
"Ø SHFT 3"
"Ø SHFT 4"

remove the other channels.

Entering "SHFT 1", "SHFT 2", "SHFT 3", "SHFT 4" will display those telemetry failsafe channels which have been established previously, or "Ø" if none has been established. If any or all of

the four telemetry failsafe channels have not been established, then telemetry failsafe is inhibited, and only control failsafe is possible.

Selecting "CHANNEL ZERO" will result in a display of the remaining time until failsafe in the VALUE-EDIT window, i.e., entering

"Ø CH"

will cause the remaining time to be displayed. This will, of course, normally be "6Ø", indicating that all is well. Should telemetry failsafe be inhibited, "CHANNEL ZERO" may not be selected; "E" will be displayed if this is attempted.

In the event of any kind of failsafe, all command outputs are inhibited. As described above, putting the terminal into Maintenance Override status ends all failsafe conditions and re-enables command outputs.

When Maintenance Override mode is ended, all timers are reset, so there is once again a 45-second wait until control failsafe and an one-hour wait until telemetry failsafe, regardless of past conditions at the Remote Terminal. In addition, should all four telemetry failsafe channels vanish, then telemetry failsafe is ended.

4.7 MRC-1 REMOTE REFERENCE DATA

The following is a condensed description of MRC-1 Remote Terminal key sequences and functions for quick reference purposes.

SELECT NEW CHANNEL:	X X CH
ADVANCE ONE CHANNEL:	CH
SELECT NEW SITE:	X SITE
INVERT/DEINVERT STATUS CHANNEL:	INV

LATCH/UNLATCH STATUS CHANNEL	SHFT LATCH
ADD/REMOVE FALLING EDGE ALARM	⌐¬
ADD/REMOVE RISING EDGE ALARM	SHFT ¬⌐
RELEASE ALL LATCHED CHANNELS	SHFT STAT CLR
CALIBRATE, LINEAR MODE	X X X X LIN
CALIBRATE, POWER MODE (Sign of X X X X must be positive)	X X X X SHFT POWER
CALIBRATE, INDIRECT MODE: (Sign of X X X X must be negative) Display will be proportional to product of two preceding channels. Channels 1 and 2 may not be calibrated in this mode.	- X X X X SHFT POWER
ESTABLISH LOWER LIMIT: (Point position of limit need not match point position of calibration)	X X X X LOW LIM
DISPLAY LOWER LIMIT	LOW LIM
REMOVE LOWER LIMIT	Ø LOW LIM
ESTABLISH UPPER LIMIT: (Point position of limit need not match point position of calibration)	X X X X SHFT UPPER LIM
DISPLAY UPPER LIMIT:	SHFT UPPER LIM
REMOVE UPPER LIMIT:	Ø SHFT UPPER LIM
ENABLE/DISABLE LIMIT CHECKING:	LIMS
ESTABLISH RAISE CHANNEL:	X X SHFT MAP RAISE
DISPLAY RAISE CHANNEL:	SHFT MAP RAISE
REMOVE RAISE CHANNEL:	Ø SHFT MAP RAISE
ESTABLISH LOWER CHANNEL:	X X SHFT MAP LOWER
DISPLAY LOWER CHANNEL:	SHFT MAP LOWER
REMOVE LOWER CHANNEL:	Ø SHFT MAP LOWER

ESTABLISH LATCHING COMMAND CHANNEL: (Where X X in both lines is the channel to be made latching)	X X SHFT MAP RAISE X X SHFT MAP LOWER
RAISE:	RAISE
LOWER:	LOWER
TURN ON LATCHING COMMAND CHANNEL:	RAISE
TURN OFF LATCHING COMMAND CHANNEL:	LOWER
ESTABLISH MUTE CHANNEL: A. Mute condition occurs when mute channel is "OFF" (after latch and invert, if applicable.) B. No limit checking during mute condition or for 4 seconds thereafter.	X X SHFT MUTE
DISPLAY MUTE CHANNEL	SHFT MUTE
REMOVE MUTE CHANNEL:	Ø SHFT MUTE
ACKNOWLEDGE ALARM: A. First push displays channel number and condition, silences audible alarm. B. Second push ends flashing alarm indication. C. In the case of limit violations, steadily-on alarm indication will persist until: analog value is back in bounds; or, mute status begins; or, limit checking is disabled.	ACK ACK
BEGIN LAMP TEST:	LAMP TEST
END LAMP TEST:	LAMP TEST
BEGIN MAINTENANCE OVERRIDE: A. Ends any failsafe condition. B. Inhibits any RAISE/LOWER commands from control end.	MAINT O'RIDE
END MAINTENANCE OVERRIDE A. Resets failsafe timers. B. Inhibits commands from remote end.	MAINT O'RIDE
ESTABLISH TM FAILSAFE CHANNEL N: (N=1 to 4)	X X SHFT N

Telemetry failsafe takes place if the analog value on any established telemetry failsafe channel remains below about 0.3 volts for 1 hour, or the Control Terminal fails to receive transmissions from the Remote Terminal for 1 hour. Telemetry failsafe ends if all four telemetry failsafe channels fall to zero.

DISPLAY TM FAILSAFE CHANNEL N: SHFT N

REMOVE TM FAILSAFE CHANNEL N: Ø SHFT N

MISCELLANEOUS:

Control failsafe takes place if a Remote Terminal receives no successful communications directed to it for 45 seconds.

Alarms are disabled for 1Ø seconds after reset.

CALIBRATION OVERFLOW DISPLAY: EEEE

A/D SATURATION DISPLAY (6144 COUNTS) ----

5.0 INSTALLATION

5.1 INTRODUCTION

The purpose of this section is to provide installation details for the MRC-1 Remote Terminal. It also provides other data should the user expand or otherwise modify the system in the future.

> CAUTION
>
> ALWAYS REMOVE POWER FROM THE TERMINAL AND DISCONNECT THE BATTERY WHENEVER PRINTED CIRCUIT MODULES ARE REMOVED OR REPLACED IN THE UNIT. FAILURE TO OBSERVE THIS CAUTION MAY CAUSE DAMAGE TO ONE OR MORE MODULES.

5.2 PHYSICAL INSTALLATION

The MRC-1 is designed for industry standard RTMA rack mounting. It is suggested that the Remote Terminal be mounted in the rack at approximately 65 inches height for best operation accessibility. With the power supply shipping screw removed, insert the terminal in the rack or cabinet and install 10/32 x 1" screws with fiber washers through the oval holes in the chassis flanges. Torque screws firmly to provide a secure mounting. Once installed in the rack, all assemblies that normally require service can be removed without removing the chassis from the rack. The extender board is stowed to the left of the power supply. The flat ribbon cable between the front panel and CPU card may have to be disconnected to remove the extender board. At this time, remove the extender board and store in another location at the Remote Terminal site in order to provide maximum ventilation to the Terminal.

5.3 PHONE LINE CONNECTION - 4-WIRE

If you are using a 4-wire interconnect service, the pair of wires

to the Control Terminal is connected to terminals 4 and 6 of the Modem Telco Interface card (third from right assembly at rear of unit). The pair from the Control Terminal is connected to terminals 1 and 3. Note that the Modem Telco Interface contains fuses mounted internal to the card. Should you suspect that, as a result of lightning strike, the phone lines have been hit, remove the two screws securing the Modem Telco Interface card and check and/or replace fuses, as required.

5.4 PHONE LINE CONNECTION - 2-WIRE

If you are using a two-wire interconnect arrangement, place a short jumper between terminals 2 and 4. Then, connect the telephone line to terminals 1 and 5 of the Modem Telco Interface card. See the preceding paragraph for lightning protection fuses.

5.5 FM SUBCARRIER INTERCONNECT

BNC connector J3 is the output of the Remote Terminal and is connected to the equipment over which the subcarrier signal will be transmitted. A BNC connector J2 is used for the subcarrier data being received from the Control Terminal. Note that the components of the subcarrier interface module are frequency dependent. Should your requirements for subcarrier frequencies change in the future, some changes in component values may be required. The component values for various bands of subcarrier frequencies are detailed in Section 8 for the subcarrier interface card, if ordered as part of the system.

5.6 MIXED COMMUNICATIONS

If the system is ordered with mixed communications functions; i.e., telco in/subcarrier out, or telco out/subcarrier in, the connection procedure is similar to that outlined for the previous methods

of communications link interconnection. The subcarrier function (either in or out, as appropriate) is a BNC connector while the telephone circuit is a terminal block connection.

5.7 AUDIBLE ALARM

The control of the audible alarm of the Remote Terminal is accessed through pins 5 and 6 of J1 on the CPU interface card (right module viewed from rear of chassis).

Several alternatives are available to the user. The simplest is to jumper pins 5 and 6 on the connector. In this case, the audible alarm will always be activated when an alarm condition is detected. In the event that the Remote Terminal is located in a studio booth, it is possible to have external control of the audible alarm so that it will be muted when a mike is active if those facilities are available in the studio. Figure 5.1 indicates a typical arrangement of muting the alarm when mikes are active.

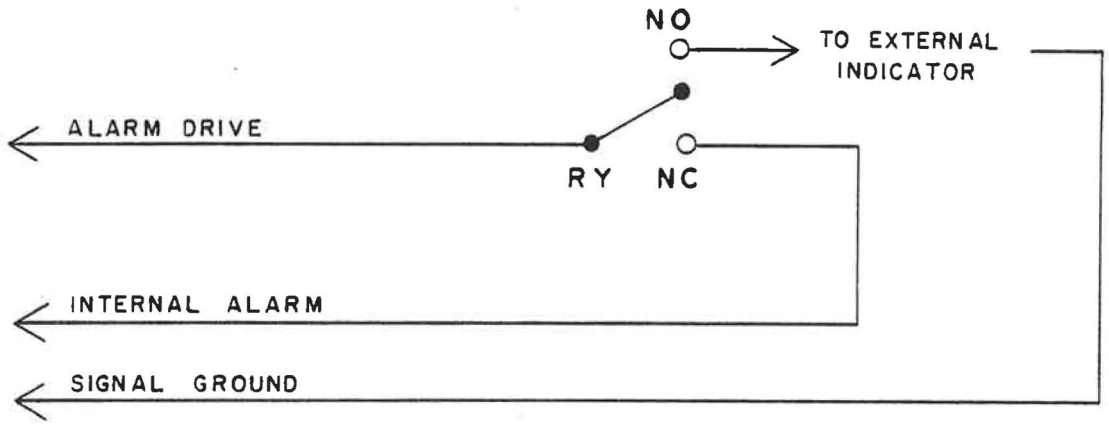


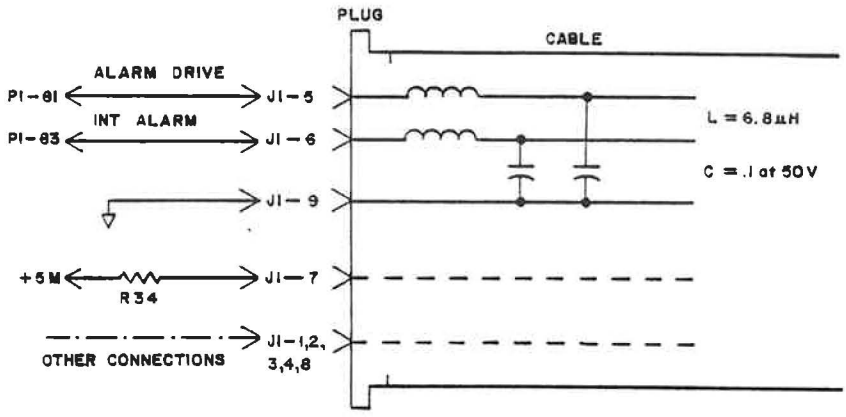
FIGURE 5-1 AUDIBLE ALARM CONNECTIONS

The relay contact (supplied by user) is assumed to be N.O. when any mike is active and N.C. when no mikes are active. The signal labeled to EXTERNAL INDICATOR may be used to operate a user-supplied indicator for an alarm indication.

NOTE: The "ALARM DRIVE" and "INT ALARM" connections are each associated with a trace which runs across the C.P.U. Interface Board, through the Mother Board, across the C.P.U. Board and eventually terminates at the Alarm Driver on the front panel.

Because these connections are generally used at a studio location, and seldom in an R.F. environment, no filtering was included for them.

Considering the susceptibility of any digital logic system to R.F. spikes, it is our suggestion that all MRC-1 customers who use these connections for remote alarms or remote alarm enable switches in an R.F. environment should incorporate a small LC filter in order to isolate the MRC-1 from R.F. interference. It will be easiest to do this by locating the inductors and capacitors near the female plug on the cable when the cable for this jack is made up. Below is a diagram of the procedure to follow.



MAI Part Numbers: 14-287.25, 4020343, Inductor
R.F. 6.80 µH
05-397.25, 4310207, Capacitor
.1 µF/50 V 20%

5.8 EXTERNAL BATTERY

The Remote Terminal normally requires the use of an external battery to maintain the contents of memory in the event of a power failure. The battery is supplied to maintain memory contents for a period of time during a power failure (not complete terminal operation, however). To connect the battery, first attach the battery holder to the chassis, insert battery and connect the terminals in accordance with Figure 5.2. Batteries are always shipped disconnected to prevent discharge during transit. The positive (+) battery terminal is connected to the red binding post terminal and the negative (-) is connected to the black binding post.

The user may use other batteries in place of the one supplied. In this case, the maximum voltage that may be applied to the terminal posts is 7.0 volts. The nominal design voltage is 6.0 volts, with a float charge of 6.7 volts and a maximum float charge current of 75 ma. If you use an external battery and charger, the charger voltage must never exceed 7.0 volts and must be filtered with no more than 10 mV ripple.

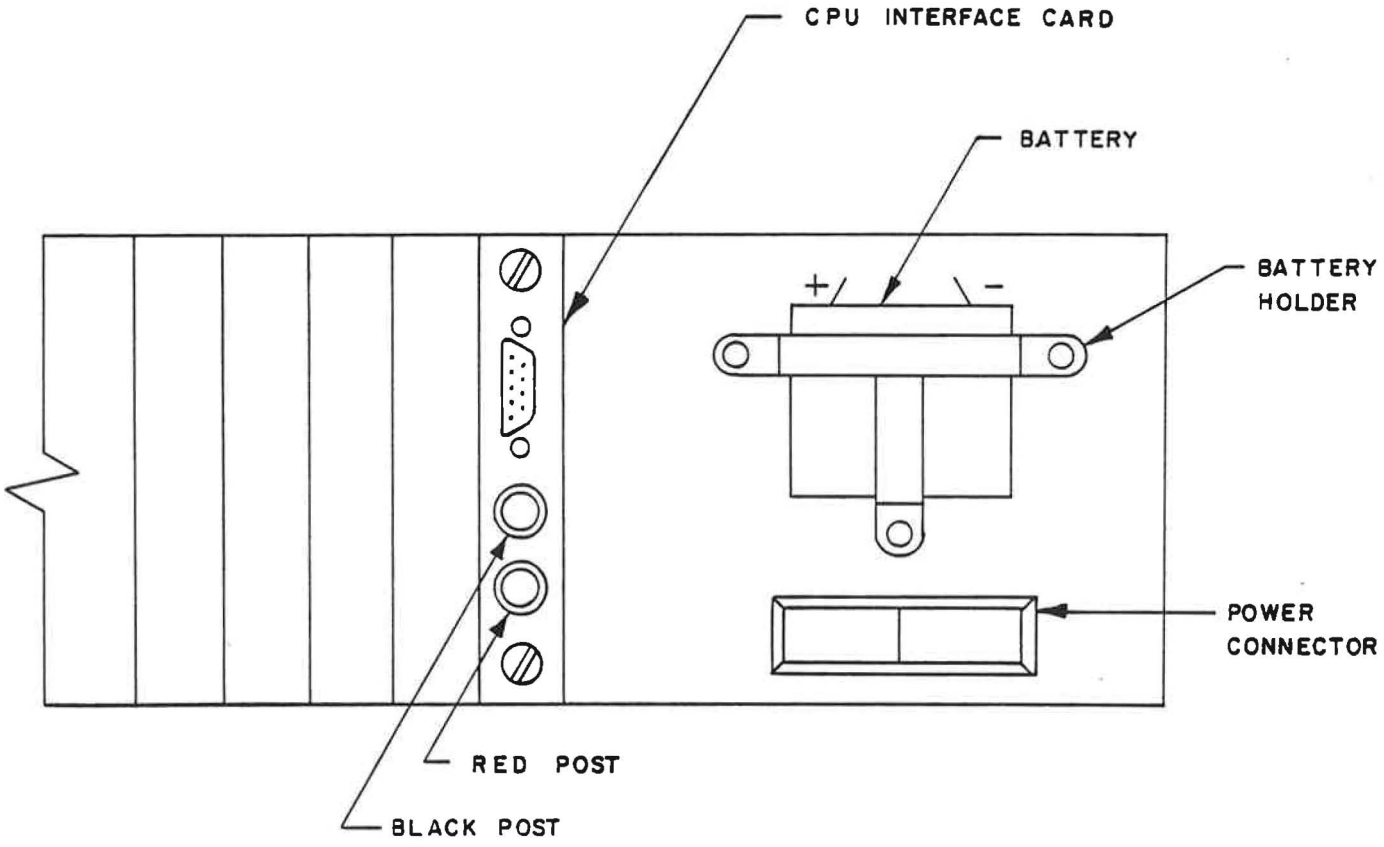


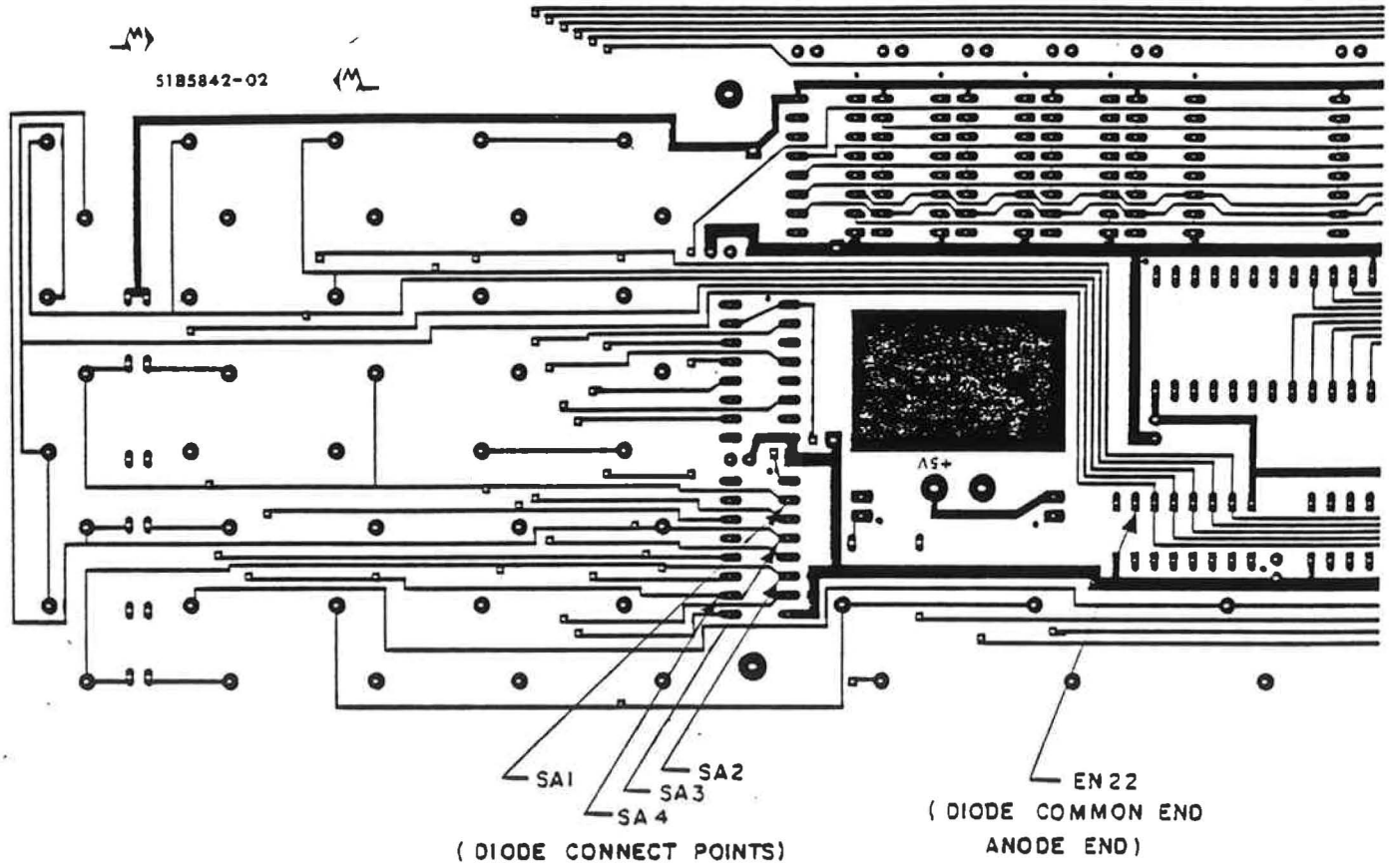
FIGURE 5-2 BATTERY INSTALLATION
REMOTE TERMINAL

5.9 SITE SELECTION

It is necessary to program the Remote Terminal with the number of the site for the terminal. It is assumed that sites are numbered sequentially from 1 to N where N is the last site number with no numbers skipped. Note that early production units use a soldered diode matrix instead of the switches. Refer to Figure 5.3 for location and connection chart.

The switches are set as shown in the table below for the number of sites in the system:

SITE	SWITCH POSITIONS			
	1	2	3	4
1	OFF	OFF	OFF	OFF
2	ON	OFF	OFF	OFF
3	OFF	ON	OFF	OFF
4	ON	ON	OFF	OFF
5	OFF	OFF	ON	OFF
6	ON	OFF	ON	OFF
7	OFF	ON	ON	OFF
8	ON	ON	ON	OFF
9	OFF	OFF	OFF	ON



Foil Side of Front Panel PCB Shown

DIODES INSTALLED
(Diodes are 1N270 or equivalent)

SITE	SA1	SA2	SA3	SA4
1	None	None	None	None
2	Diode	None	None	None
3	None	Diode	None	None
4	Diode	Diode	None	None
5	None	None	Diode	None
6	Diode	None	Diode	None
7	None	Diode	Diode	None
8	Diode	Diode	Diode	None
9	None	None	None	Diode

FIGURE 5.3

SITE IDENTIFICATION DIODES
(Early Production Units Only)

5.10 FAIL SAFE

The fail-safe output is controlled by a relay capable of switching a load of up to 24 VDC at currents of up to 1 ampere. During normal operation the relay will close a connection between pins 3 and 4 of the rear connector on the CPU Interface Board. When MRC-1 power is removed or a fail-safe condition occurs, the relay will open. Figure 5-4 illustrates a typical application of the fail-safe output.

Inductive loads (relay coils, etc.) should have a "clamping" diode wired across them to inhibit negative voltage spikes. External relays should be used when it is desired to switch to greater loads (or AC loads which must have a Series R (100Ω)/C (1μf) network across them).

These relays may also be interfaced with transistor-transistor logic (TTL) digital circuits. The relay contacts should be wired so that one side is referenced to the digital common (ground), and the other relay contact to the digital input. A pull-up resistor may be necessary, and it is advisable to wire a 1 μf capacitor and 100 ohm resistor (in series) across the relay output to suppress contact bounce. For further details, refer to Section 8, CPU Interface.

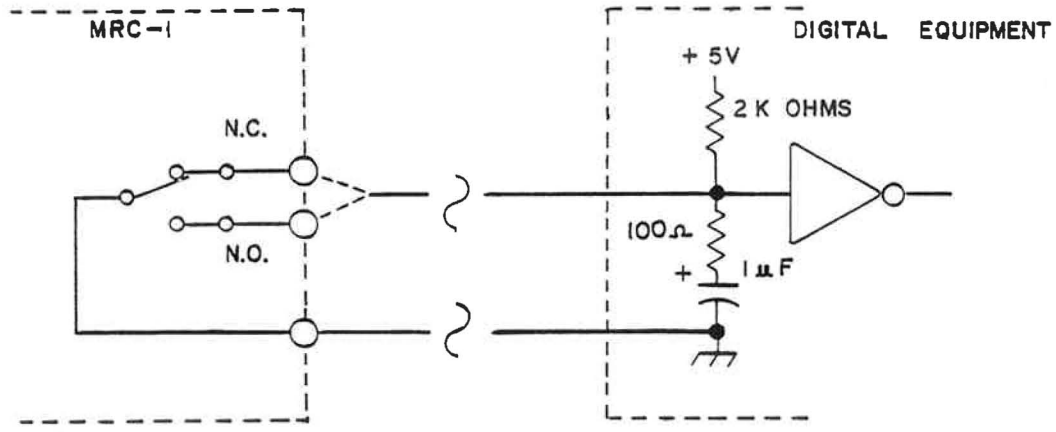


FIGURE 5-4 TYPICAL FAIL SAFE OUTPUT

5.11 MAINTENANCE OVERRIDE

An external indicator is provided in the form of a relay to provide remote indication that the Remote Terminal has been placed in the Maintenace Override mode of operation. This indication is normally used to illuminate a light near the exit of the transmitter room to warn the operator the Remote Terminal has been left in the Maintenance Override Mode. When in the Maintenance Override mode, no commands are accepted by the Remote Terminal from the Control Terminal; hence, you may save yourself a trip to the transmitter site by getting into the habit of removing the Remote Terminal from the Maintenance Override mode before you leave. There is no way to exercise this function from the Control Terminal. You may use a relay or TTL logic for indirect control of the lamp, in which case the wiring illustrated for the fail-safe output can be followed (Figure 5-4), except terminals 1 and 2 of J1 are used. A small lamp may be driven directly, as illustrated in Figure 5-5.

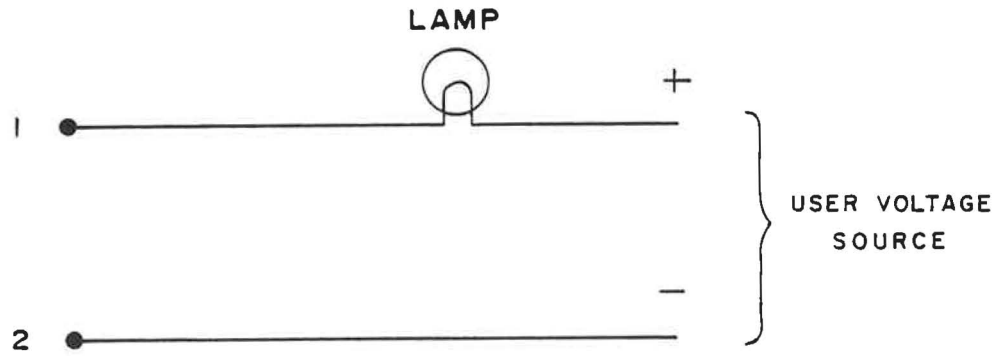


FIGURE 5-5 TYPICAL MAINTENANCE OVERRIDE CONNECTION

5.12 INPUT/OUTPUT CONNECTORS

The connectors for telemetry (analog), status and commands may now be wired up. A definite wiring pattern has been established for the telemetry (analog) input, TTL status input, optically isolated status input, open collector command output, and the optically isolated command output printed circuit modules through both the filtered and unfiltered interface cards. The most positive voltages of the 16 inputs or outputs are wired consecutively from pins 1 through 16. The negative (or ground return) input or output is wired consecutively from pins 20 through 35. This allows twisted pairs to be used as connections to the modules to reduce external field noise pickup and, at the same time, allows a simple pattern to the connection with the two leads at a slight diagonal on the connector. Proper grounding and shielding techniques should be followed throughout.

For those applications requiring control of high voltage or AC power, a relay isolated command output option is available. The connection from the relay panel to a command output module through an interface card has been pre-wired and only requires it be plugged in.

5.3 INSTALLATION COMPLETION

This completes installation of a Remote Terminal. Power may now be applied to the terminal. Depress the "ACK" key on the Remote Terminal front panel in order to clear the "cold start" condition which occurs whenever power is applied to the Remote Terminal after the contents of memory have been lost. You will observe the three power indicator LEDs on the internally-mounted CPU board illuminate. After a short period, the Reset LED on the CPU board will go out. After a short delay (less than 1 second), the Output and Input LEDs on the modem board should begin to flicker indicating that data is being sent and received. The modems are factory

adjusted for +0.0 dBm output level and a -16.0 dBm receive level. Should the actual levels of your system be radically different, some adjustment of the send and receive levels may be required. Refer to Section 8 for wireline modem and/or subcarrier modem adjustments. External loads if run from DC must have a damping diode across them (e.g. DC relay coil). Connect the diode so that it will normally not conduct. External loads, if AC, must have a series R.C. network across them. (Values of 1 μf and 100Ω are suggested.)

At this point, you may enter command sequences at the keyboard to calibrate telemetry (analog) channels, observe and set up status channels, and to set up command outputs.

For the user's convenience, a set of tables (Tables 5-1, 5-2, and 5-3) are provided that allow the user to record the manner in which he has set up the Remote Terminal. You may reproduce these forms as required for your purposes.

Each of the 32 telemetry channels is indicated on the left side of each table and, when completed, they will provide the user a guide for future reference as to how the Remote Terminal was set up. Most column headings are directly related to the set up functions outlined in Section 4 of this manual. The columns labeled "+ Input" and "- Input" are filled in to indicate the connector pins at the interface card. For the command outputs, since the output is mapped to the telemetry channel, the terminals actually connected must be inserted by the user. In Table 5-1, the column labeled "TYPE" is for the type of calibration; i.e., linear (L), power (P), or indirect (I).

TELEMETRY (ANALOG) DATA

TELE-METRY CHANNEL	DESCRIPTION OF VALUE MEASURED	TYPE L,P,I	NOMINAL CALIBRATION	HIGH LIMITS	LOW LIMITS	MUTED BY STATUS	+ INPUT	- INPUT
1							1	20
2							2	21
3							3	22
4							4	23
5							5	24
6							6	25
7							7	26
8							8	27
9							9	28
10							10	29
11							11	30
12							12	31
13							13	32
14							14	33
15							15	34
16							16	35
17							1	20
18							2	21
19							3	22
20							4	23
21							5	24
22							6	25
23							7	26
24							8	27
25							9	28
26							10	29
27							11	30
28							12	31
29							13	32
30							14	33
31							15	34
32							16	35

TABLE 5-1

TELEMETRY (ANALOG) DATA TABLE

STATUS DATA

TELE-METRY CHANNELS	DESCRIPTION OF SOURCE OF STATUS	INVERT	LATCH	ALARM ⌋	ALARM ⌊	+ INPUT	- INPUT
1	VFIL					1	20
2	HV					2	21
3	Body		X			3	22
4	Beam		X			4	23
5	VSWR		X			5	24
6	Cav Air.		X			6	25
7	H.V. ARC					7	26
8	FLOW					8	27
9	A FIL					9	28
10	HV					10	29
11	Body		X			11	30
12	Beam					12	31
13	H.V. ARC		X			13	32
14	FLOW					14	33
15						15	34
16						16	35
17						1	20
18						2	21
19						3	22
20						4	23
21						5	24
22						6	25
23						7	26
24						8	27
25						9	28
26				-		10	29
27						11	30
28						12	31
29	PWR TRANSFER SWITCH			X		13	32
30	AIR					14	33
31	Door			X		15	34
32	Door			X		16	35

TABLE 5-2

STATUS DATA TABLE

TELE-METRY CHANNEL	RAISE COMMAND				LOWER COMMAND			
	OUTPUT NUMBER	FUNCTION PERFORMED	+ OUT	- OUT	OUTPUT NUMBER	FUNCTION PERFORMED	+ OUT	- OUT
1								
2								
3								
4								
5								
6								
7								
8								
9								
10								
11								
12								
13								
14								
15								
16								
17								
18								
19								
20								
21								
22								
23								
24								
25								
26								
27								
28								
29								
30								
31								
32								

TABLE 5-3

COMMAND OUTPUT TABLE

6.0 HARDWARE/SOFTWARE OVERVIEW

6.1 INTRODUCTION

The purpose of this section is to provide the user with a general overview of the hardware and software of the MRC-1 Remote Terminal. It is not a detailed explanation of microprocessors, but rather, the basic design concepts incorporated into the MRC-1. The user is referred to many excellent texts on microprocessors including M6800 Microcomputer System Design Data, published by Motorola, Inc.

Figure 6-1 is a block representation of the major components of an MRC-1 Remote Terminal. The chassis houses the assemblies. A mother board is located approximately three quarters of the way back from the front of the terminal. The functional cards (i.e., CPU, memory, modem, options, etc.) plug into the mother board from the front.

The user's connection to a functional card occurs through an interface card that plugs into the rear of the mother board. The interface card provides the physical connectors, terminals or barrier strips to which the user makes his connection. In some cases, there can be several interface cards that can be associated with a given functional card. For example, a modem card can have one of four interface cards depending upon the type of communications circuit. In other cases, the same interface card can serve several functional cards. As an example, the Filtered Interface card is normally used with the Telemetry (Analog), Status and Command cards.

The mother board provides;

- o power distribution to all cards,
- o interconnection between functional and interface cards,

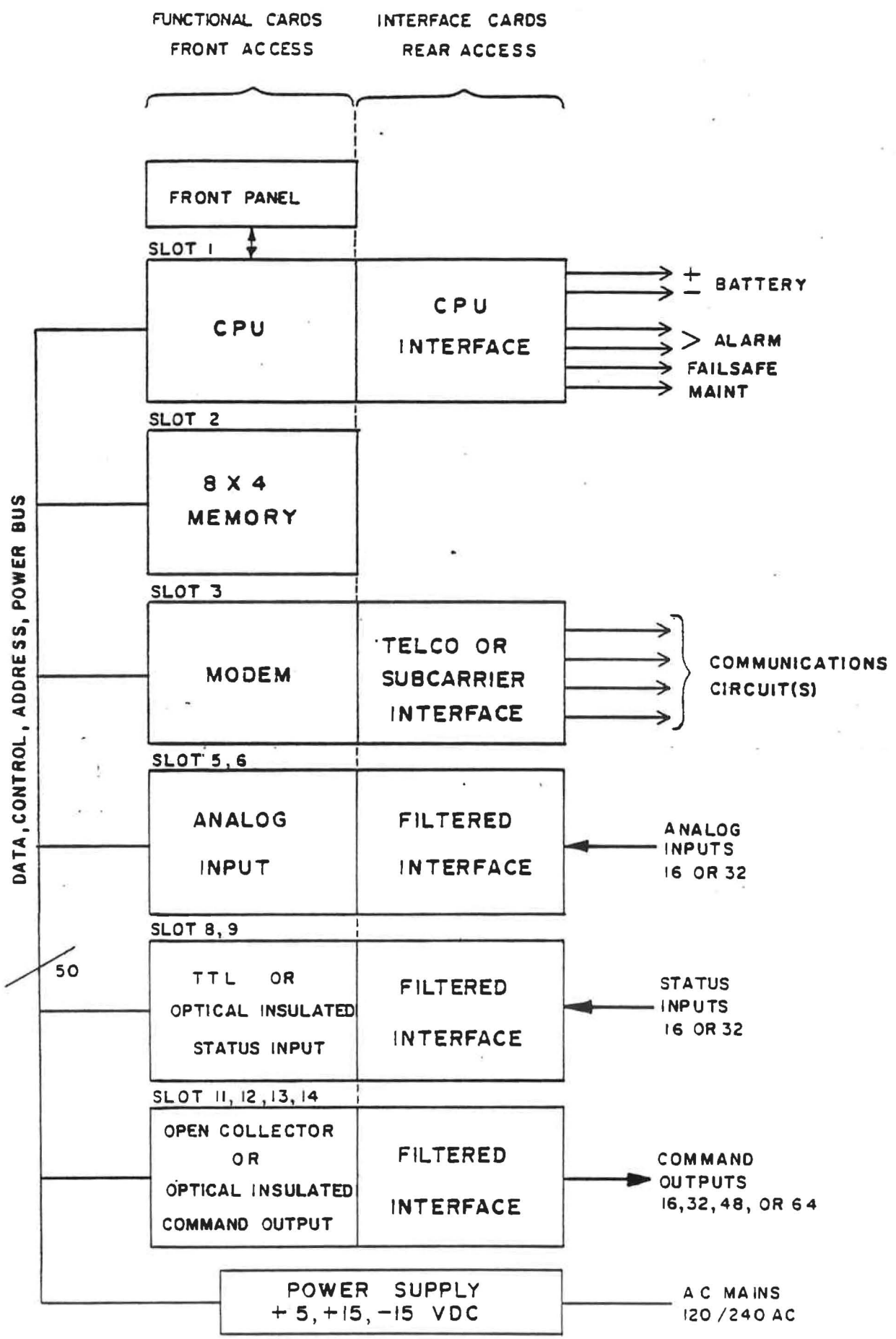


FIGURE 6-1 REMOTE TERMINAL BLOCK DIAGRAM

- and distribution of control, data, and address busses to the functional cards.

All modules and subassemblies, except for the mother board, are removable without disassembling the chassis.

6.2 BUS ARCHITECTURE

The MRC-1 is designed using a bus structure which allows flexible configuration changes. Fifty control signals and power lines are bussed to each card slot. Cards are accessed by digital words on the address bus and do not require an absolute physical slot to be assigned for each card. An exception to this rule is the CPU card, which must always be plugged into the first slot to obtain an AC power sample for the real-time clock and power fail circuits.

Each printed circuit card edge connector has 100 pins. The even pins contain the common bus signals. The odd pins are used to communicate via interface cards to the external world through the rear panel. To prevent confusion, the even wire-wrap pins are sheared off during manufacturing, leaving only the odd pins for card input/output connections. Signal assignments for the connector pins are shown in Table 6-1.

Note that signal ground, +5, +15, and -15 voltages are available to both functional and interface cards.

TABLE 6-1

MRC-1 BUS ARCHITECTURE

PIN	NAME	DESCRIPTION
1,2,3,4	GROUND	System common signal ground
5,6	PLUS 15V	Positive 15V supply Remote 1.5 amps capacity Control .8 amps capacity
7,8	NEGATIVE 15V	Negative 15V supply Remote 1.5 amps capacity Control .8 amps capacity
9,10	STANDBY 5V	5-volt supply back up by an external battery
12	DØ	
14	D1	
16	D2	
18	D3	Bidirectional 3-state data bus
20	D4	is used to transfer data between
22	D5	the microprocessor, its peripher-
24	D6	als and memory
26	D7	
28	AØ	
30	A1	
32	A2	
34	A3	
36	A4	
38	A5	
40	A6	
42	A7	16-pin address bus
44	A8	Both memory and input/output
46	A9	devices are addressed using these
48	A10	lines.
50	A11	
52	A12	
54	A13	
56	A14	
58	A15	
60	*RESET	This active low input is used to reset and start the microprocessor

TABLE 6-1 (continued)

PIN	NAME	DESCRIPTION
		from a power down condition, resulting from a power failure or an initial start-up of the processor. The signal is generated by the CPU interface card and is used to reset functions in the CPU and various cards that have reset capability.
62	E	1 MHz clock signal used to synchronize all system functions
64	R/*W	This output signals the peripherals and memory devices whether the CPU is in the READ (High) or WRITE (Low) state. The normal standby state of this signal is READ.
66	VMA	Valid Memory Address. This output from the CPU card indicates to peripheral devices that there is a valid address on the bus.
68	PRE	Input/Output Preselect. This line is high when the input/output device address space is accessed.
70	RTC	Real Time Clock. A 50 or 60 Hz signal derived from the AC power line and used as a timing signal.
72	*DMA	Direct Memory Access. When this signal goes low, the CPU card releases control over the address bus.
74	BA	Bus Available. This signal will normally be in the low state; it will go to a high state to indicate that the microprocessor has stopped and the address bus is available. This will occur if the processor is in a HALT state, or if a WAIT instruction is encountered by the microprocessor.

TABLE 6-1 (continued)

PIN	NAME	DESCRIPTION
76	*HALT	When this signal is in the low state, all microprocessor activity will be halted. In the HALT mode, the microprocessor will stop at the end of an instruction, Bus Available will be at a high state, Valid Memory Address will be at a low state.
78	BAUD	19230 Hz square wave used to set the baud rate of ACIA's (Asynchronous Communications Interface Adapters). Data rates of 1200 or 300 baud are possible using this clock.
80	*INTØ	Lowest Priority
82	*INT1	Active low prioritized interrupts. When one of these lines goes to a low state, the microprocessor suspends its normal operation and begins servicing an interrupt routine. A higher priority routine takes precedence over a lower priority.
84	*INT2	
86	*INT3	
88	*INT4	
90	*INT5	
92	*INT6	
94	*INT7	Highest Priority
96	*NMI	Non-Maskable Interrupt When this line is pulled to a low state, the processor completes its current instruction and then branches to an interrupt routine. Interrupt cannot be disabled by setting a mask bit.
97 thru 100	PLUS 5V	Positive 5V power supply Remote: 6 amps Control: 3 amps

6.3 SOFTWARE OVERVIEW

When power is restored to a Remote Terminal, there are two things that could have occurred. First, memory could have been lost because of an extended power interruption. If this condition is detected by the software, it is assumed that the Remote Terminal must be recalibrated prior to any use. This requires manual intervention. An alarm condition exists and must be acknowledged by an operator at the Remote Terminal before recalibration can proceed. During this period, the software determines the identification number of the Remote Terminal by reading the switches on the rear of the front panel. Note that each Remote Terminal must have a unique address.

If the Remote Terminal did not lose its memory data as the result of a power failure, a brief internal re-initialization cycle occurs where the software determines the number and type of modules that are in the Remote Terminal. This allows the user to add additional modules within the design capabilities at any time. Power must be turned off and the battery disconnected before removing or inserting printed circuit cards. When power is restored, the software takes inventory of what is currently available and adjusts its internal record keeping accordingly.

As the user performs setup key sequence functions, the data from the key sequence, i.e., telemetry (analog) calibration factors, limits, etc., are retained in the Remote Terminal memory. This data may be recalled by other key sequences either from the Remote or Control Terminals. The point to note is that all factors that affect a Remote Terminal are retained at that Remote Terminal.

Once the Remote Terminal is active, it is always listening to the communications circuit for a message addressed to itself from the Control Terminal. This is called a polling message. In response

to the poll, the Remote Terminal sends a brief answer indicating whether or not an alarm condition exists at the Remote Terminal. For convenience of operation, the software in the Remote Terminal allows the Control Terminal user and the operator of the front panel independent display of all data concerning the Remote Terminal. The Control Terminal operator may view any telemetry channel at the same time the Remote Terminal user is displaying any other or the same telemetry channel. There is one function - the Maintenance Override - which can be activated at the Remote Terminal to disable command activation from the Control Terminal. However, all other display functions at the Control Terminal are enabled.

Telemetry (analog) data is acquired in a cyclic sequence from the analog-to-digital (A/D) converters. When an A/D completes one conversion, the input number is incremented and the next conversion started while the previous conversion is applied through a digital filter and then limit checked. Note that limit checks occur on each conversion as each new sample is acquired. If there are two analog cards in the Remote Terminal, the process is being applied to both simultaneously.

Approximately every four seconds, the software causes each A/D converter to be switched to a set of four reference voltages. At this time, the A/D gain and offset values are determined and all subsequent input samples are corrected.

Status input data is sampled approximately 60 times per second. The attributes that have been assigned to each status input are checked and the results displayed on the front panel.

As a result of a RAISE or LOWER key being depressed, the software determines the output line that has been mapped to the telemetry channel, activates the specified output, and then, checks the output register for operation. If operational, it activates the RAISE or LOWER LED.

During communications with the Control Terminal, extensive error checking is performed to ensure receipt of valid data. The Remote Terminal must receive one valid message within 45 seconds of the previous valid message in order to maintain the fail-safe output active. If the time period is exceeded, the fail-safe output is de-activated.

7.0 MAINTENANCE

7.1 PURPOSE

The purpose of this section is to provide a guide to the maintenance of the MRC-1 at the module level. Section 8 of this manual provides the schematics, card layouts, troubleshooting and adjustment information for the individual card or assembly.

> **CAUTION**
>
> ALWAYS REMOVE POWER FROM THE TERMINAL AND DISCONNECT THE BATTERY WHENEVER PRINTED CIRCUIT MODULES ARE REMOVED OR REPLACED IN THE UNIT. FAILURE TO OBSERVE THIS CAUTION MAY CAUSE DAMAGE TO ONE OR MODULES.

7.2 HANDLING CMOS DEVICES

The MRC-1 contains several CMOS devices, such as 6802 MPU, 6821 PIA, 6850 ACIA, and 2716 EPROMS, which, unfortunately, can be damaged by severe electrical transient voltages. A person walking over a waxed floor, depending upon floor conditions and humidity, can generate voltage potential in excess of 15kV. The following is recommended to reduce damage to the CMOS devices:

1. All CMOS devices should be stored in materials that are anti-static. CMOS devices must not be inserted into Styrofoam.

2. All CMOS devices should be placed on a grounded bench surface and the user should be grounded before touching the device.

3. Nylon, or other static generating materials, should not come into contact with the device.

4. Do not remove boards or CMOS devices with power applied or with battery connected.

5. Treat boards that contain CMOS devices just like the device itself.

6. When wrapping a module for shipment, never use any plastic material that is not marked as being anti-static. Most anti-static plastic material is a pale pink color and identified as such.

7. Always use grounded test equipment to diagnose problems and ground the test equipment to the unit before placing probes on the circuits.

7.3 CARD ADDRESS AND OPTION SWITCHES -

Most card assemblies contain small switches referred to as DIP switches that select the address of the card and, in some cases, provide various common options on the card. Each switch is explained in Section 8 of this manual for the specific module.

Since each card (except the CPU card) can be placed in any card slot, 2 through 15 on the mother board, there needs to be some way of identifying the card when it is inserted. This identification is called the board address and is composed of two parts:

1. A fixed hardwired address that identifies the card type
2. A variable part of the address that identifies the particular card of a given type

For example, if the system contains two Status Input cards, they are identical in all respects except for the DIP switch positions. This allows the software to distinguish between the card that is assigned to Channels 1-16 and the card that is assigned to Channels 17-32.

A uniform convention has been established for setting the switch positions within a given type of board. This is diagrammed below. The UP arrow represents the switch in the ON position; the DOWN arrow, the OFF position. (Note: On most cards, ON is UP, OFF is DOWN, but it can be the other way. Refer to the switch itself.)

DEVICE NUMBER	CHANNEL ASSOCIATION	BCD SWITCH POSITION	DIP SWITCH POSITIONS 1 2 3 4
1	1 - 16	0	↓ ↓ ↓ ↓
2	17 - 32	1	↑ ↓ ↓ ↓
3	33 - 48	2	↓ ↑ ↓ ↓
4	49 - 64	3	↑ ↑ ↓ ↓

For troubleshooting purposes, you may interchange cards of the same type - BUT - be sure to set the switches to the proper setting before inserting the card.

7.4 FAULT ISOLATION - LEVEL 1

The MRC-1 contains several indications to aid in fault isolation down to the card level. Always go through these steps before attempting to service the equipment.

1. The three power LED indicators on the CPU card indicate the presence of voltages. The LED's should all glow with approximately the same brightness. If in doubt, check the voltages with a voltmeter.

2. Depress the RESET switch on the CPU board. This forces the CPU to begin the program from the beginning. When reset, all LED's on the front panel will illuminate briefly. Should the LED's remain ON, the fault could be either in the CPU or memory cards.

3. If simple command functions like site, lamp test or channel keys function properly, the most likely candidate is the modem. In most likelihoods, the levels need adjustment (refer to the card description in Section 8). If the top LED of the modem is flashing, it indicates that the modem is being keyed. An AC voltmeter across the output circuit should indicate a voltage that varies in step with the LED. If there is no voltage, check the fuses in the interface card.

   If data is getting out onto the communications circuit from the Control Terminal, determine if the Remote Terminal is receiving data. The bottom LED on the Remote modem should flash in step with the transmit LED of the Control Terminal. When the Remote Terminal transmits, its transmit LED will illuminate which, in turn, should cause the receive LED at the Control Terminal to be illuminated. Note that you can force the modem to transmit by activating the TEST switch on the front of the modem card.

   When using a 2-wire line, the modem hears itself transmit. You will see the transmit LED flash and the receive LED ON most of the time with a periodic short duration OFF period.

7.5 FAULT ISOLATION - LEVEL 2

The following is a guide to the isolation of problems that are associated with the various sensor inputs to the MRC-1. Each input or output, if subjected to an overvoltage or overcurrent condition, will, in general, affect only a single sensor. If any single telemetry (analog), status or command function fails to function properly, first check the external wiring carefully. With the suspect module placed on the extender card, determine if the signal is present at the input (or output) of the final transistor or gate on the card to your system. If optically-isolated inputs or outputs are involved, be sure that a source is provided and measure the voltages differentially with respect to the chassis. Also, with the analog signals, a minimum voltage of 0.256V must be present across the two inputs in order to calibrate a telemetry channel.

Because of the very heavy filtering that is done on all the lines that pass through the interface cards, do not expect the system to respond to very short-duration pulses. The problem of keeping stray RF energy out of the Remote Terminal places a number of constraints on the response time of all inputs and outputs of the MRC-1.

Along the same line, it is possible that opening up and/or operating a Remote Terminal with cards on an extender board may run into problems due to the RF field present. MRC-1's have been subjected to operation in AM, FM, TV and combination transmitter environments with confirmed success. However, since we have no control over your particular environment, no guarantee is made that the unit will function open in all circumstances.

8.0 CIRCUIT DESCRIPTIONS

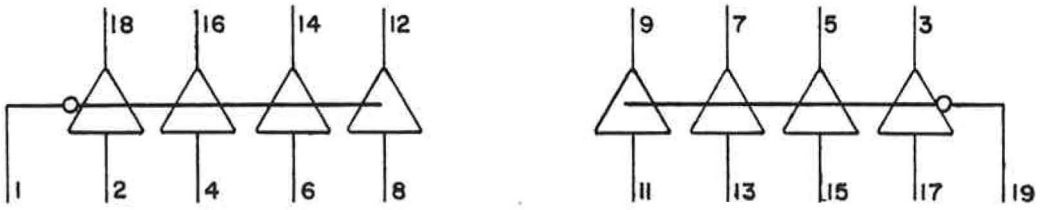
8.1 INTRODUCTION

The circuit description for the various printed circuit modules and assemblies in a standard MRC-1 are contained in this section in the form of a documentation package for each assembly.

Note: On some boards, early production units may contain DM81LS97 integrated circuits in place of the SN74LS244 I.C.'s shown in the prints and mentioned in the descriptions. Similarly, early production units may contain DM81LS98 circuits in place of SN74LS240. (These changes were made due to considerations of parts availability, not due to problems with the older parts.)

Figure 8.1 shows pin-outs for the older and newer parts.

SN74LS244 (on newer production units)



DM81LS97 (on some older production units)

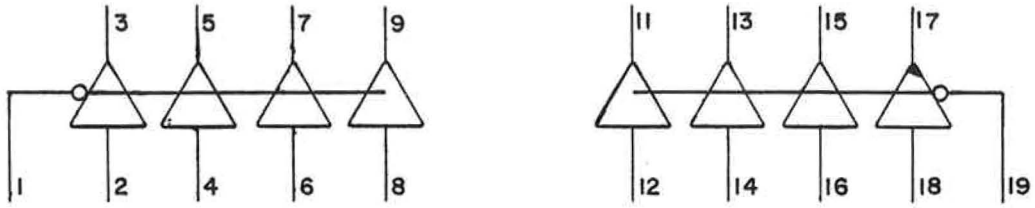


Figure 8.1

SN74LS240 is the same as SN74LS244 except for inversion of the outputs. Similarly, DM81LS98 is an inverting version of DM81LS97.

REMOTE TERMINAL FRONT PANEL

Assembly 20C2703
Schematic 91C7127
PC Board 51B5842

I. PURPOSE

This module has five functions:

1. Display site number, channel number, and value on seven-segment displays
2. Display thirty-two user status inputs (if installed) on discrete LED's
3. Display system status on discrete LED's
4. Provide an audible alarm
5. Encode keyboard entries for use by the CPU board

II. THEORY OF OPERATION

A. Overall: The front panel can be looked upon as a X-Y matrix, the X direction being data, and the Y direction being a location. The X path consists of six bits, while the Y path is five bits describing 32 (2^5) locations, 21 of which are used.

Location bits B0-B4 are decoded using a 4 to 16-bit decoder (U22) to provide locations 1 through 16, and a 3 to 8-bit decoder (U23) to provide locations 17 through 21. When accessing locations 1 through 16, all inputs of U20 are high, forcing the output low. This enables tri-state

buffer U17, allowing data to be sent to U1-U16. When accessing locations 17 through 21, one of the inputs of U20 will be low, forcing the output high, causing pin 12 of U19 to go low. This enables tri-state buffer U21, allowing data from the keyboard matrix to be sent to the CPU board. No locations are accessed unless CB2 (J2-11) is low. This signal is normally high, and pulses low for 7 microseconds when writing new data into locations 1 through 16. It is held low while reading the keyboard.

B. Seven-Segment Displays: Y locations 1 through 8 are used to select the eight seven-segment displays. Data is applied at J2-1 through J2-6 (A0-A5) to the inputs of U17. U17 is used to buffer the relatively low drive capabilities of the signals from the CPU board. Bits A0 through A3 are applied to the A, B, C, and D inputs of the TIL-308 displays. The resultant displays are shown in Fig. 1. Bit A4 is used to control the left-hand decimal point.

C. User Status: Data for the user status appears on A0-A5 and is clocked into hex D latches U1 through U6. This data is active low; the LED is ON if the corresponding bit is low. Resistors R1-R32 are used to limit the current through the LED's.

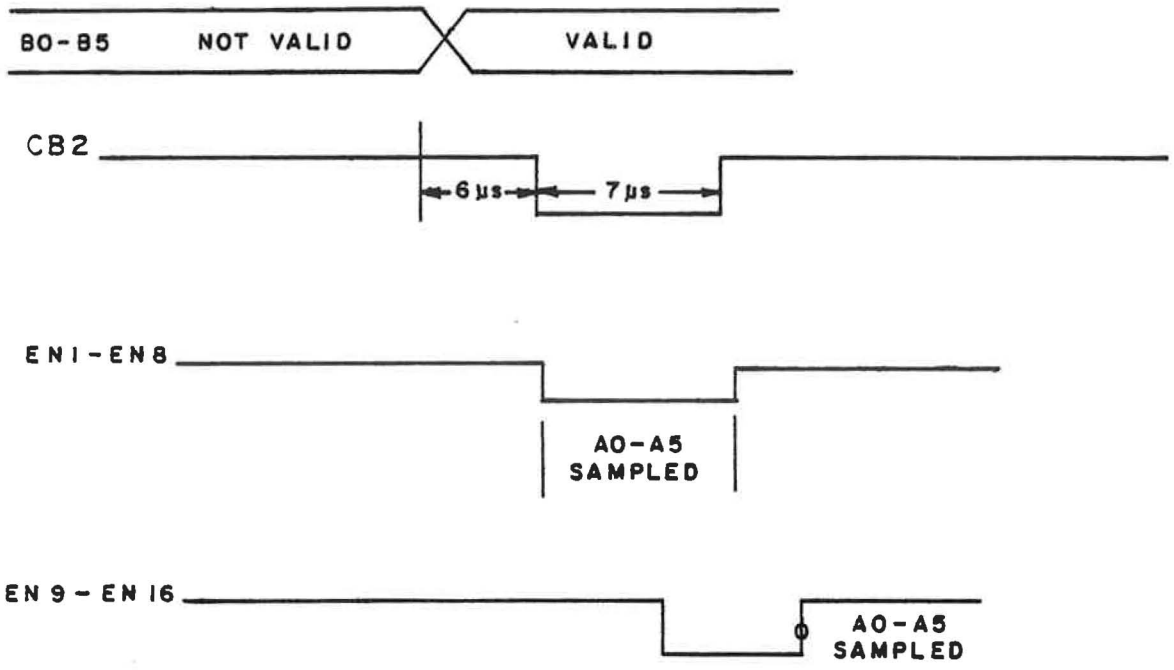
D. System Status: Data for system status is supplied in the same manner as the user status. U7 and U8 are used to store the status and drive the LED's.

E. Audible Alarm: Data bit A4 at location 16 (U8) is latched in at U8 and fed to audible alarm driver Q1. This

bit is active high and drives the Sonalert if J2-15 (alarm drive) and J2-16 (internal alarm) are connected together by the user.

F. Keyboard: During accessing of locations 17 through 21, data lines A0-A5 will normally be low, indicating that no push buttons are activated. A push-button activation will cause the appropriate location line to be connected to a data line, causing the data bit to go high.

III. TIMING DIAGRAMS



IV. TROUBLESHOOTING

1. Verify that the site, channel, and value displays blank out, and all of the discrete LED's are lit during reset (depressing the RESET switch on the CPU board). If this does not occur, check pins 14 and 13 of U18; both should go low during reset. If this does not occur, refer to the section on the CPU interface board.

2. If certain numbers will not appear on a display, suspect the display IC. If certain numbers will not appear on all the displays, there may be a stuck bit on A0-A5. A stuck bit should also show up on the status lights; this will show up on LAMP TEST, where the LED will not change its state. Stuck bits may be caused by a defective U1-U17 or U21, or a failure on the CPU board. Remove U17 from its socket. All LED's should be OFF and the BCD displays should read "F". If they do not, this indicates either a short to ground or a defective input on U1-U16. Remove U1-U16, one at a time, (leaving only one out at a time) until the displays read correctly. If doing this for all of U1-U16 does not solve the problem, check with an ohmmeter (with the power OFF) from A0-A5 to ground to check for shorts.

3. Most failures in the keyboard will be caused by a malfunctioning key-switch. If a key-switch will not function, try shorting across its two contacts on the rear of the PC board with a jumper wire. If this performs the appropriate function, replace the switch. Another possible problem is if the key-switch is shorted, this

will result in an apparently dead keyboard. The easiest way to check for this is to remove power from the unit and check across each key-switch with an ohmmeter, looking for a shorted switch.

FIRST USED ON MRC-1

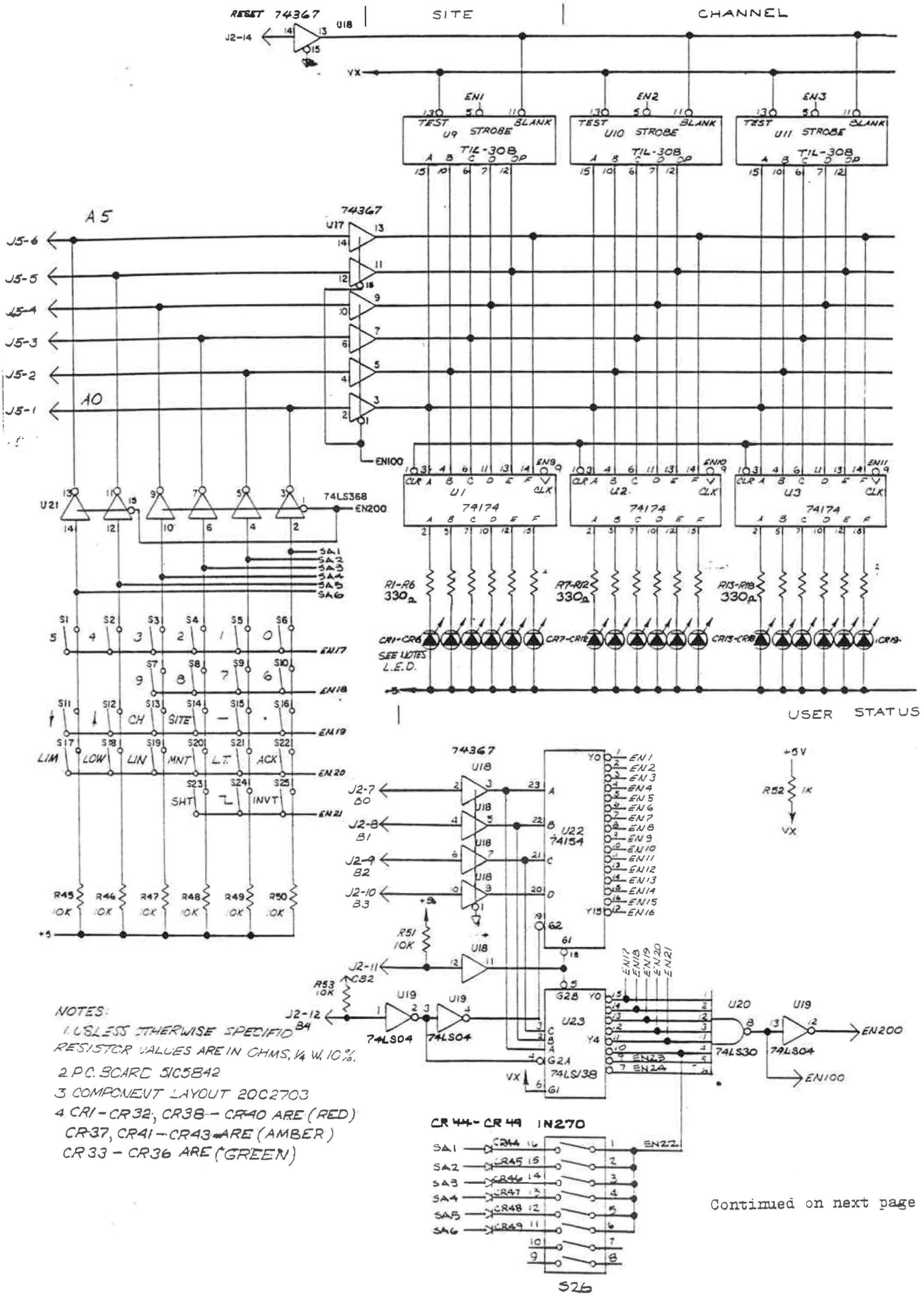
E1	ADDED RSS TO DWG. 6 NOV 80 ECO 1961 AJB	
D1	U17 & U18 WAS 74LS367 ECO 1946, 10-20-80	
C1	IDENTIFIED CR44-CR49 (INE270). PCO 1671. 3 APR 80 BWF	
C	DELETED DIODES FROM CN22. ADDED 5264 CR44 - CR49. ADDED CN23 AND CN24 ECO 1553 24 JAN 80 JRM	
B1	CHANGE DIODE ARRNG REDRAWN PER ECO 1494 AJB	
B	ADDED CN22 INFO AS WAS ADDED AS WAS ECO 1374 [illegible]	
A	RELEASED FOR PRODUCTION 8/7/79 LL	
REVISIONS	DATE	
MGMT. APPR.		

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA 93117

SCHEMATIC
REMOTE TERMINAL FRONT PANEL

TOL FRACT. ± 1/32. .XX ± .030. .XXX ± .010. ∠ ± 1/2°

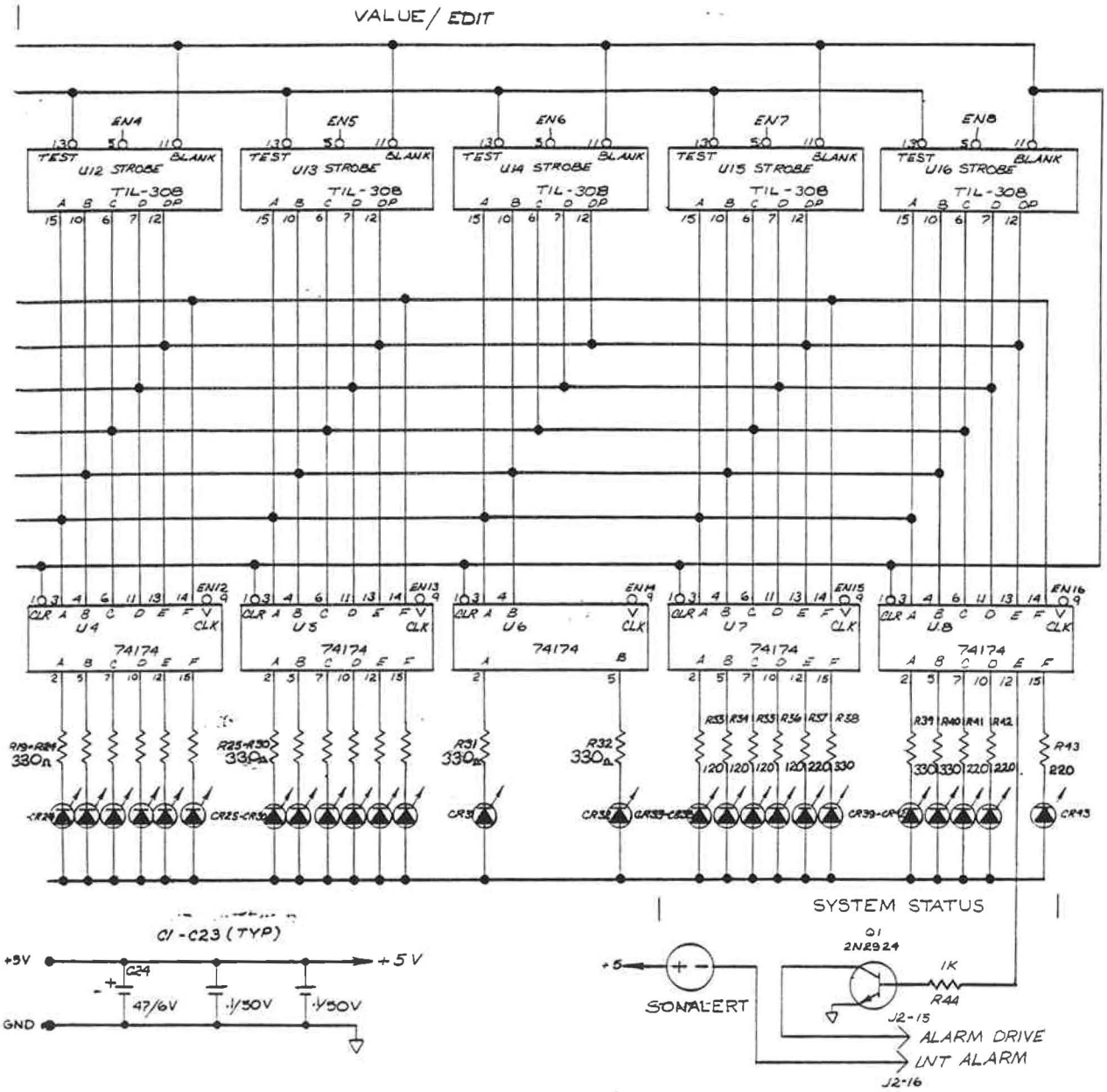
DWN	A.J.B.	4 OCT. 79	SCALE:
CHK			
ENG	HATT	10 FEB 79	91C7127 B



NOTES:

1. UNLESS OTHERWISE SPECIFIED RESISTOR VALUES ARE IN OHMS, ¼ W, 10%.
2. P.C. BOARD 5105842
3. COMPONENT LAYOUT 2002703
4. CR1 - CR32, CR38 - CR40 ARE (RED)
   CR37, CR41 - CR43 ARE (AMBER)
   CR33 - CR36 ARE (GREEN)

Continued on next page



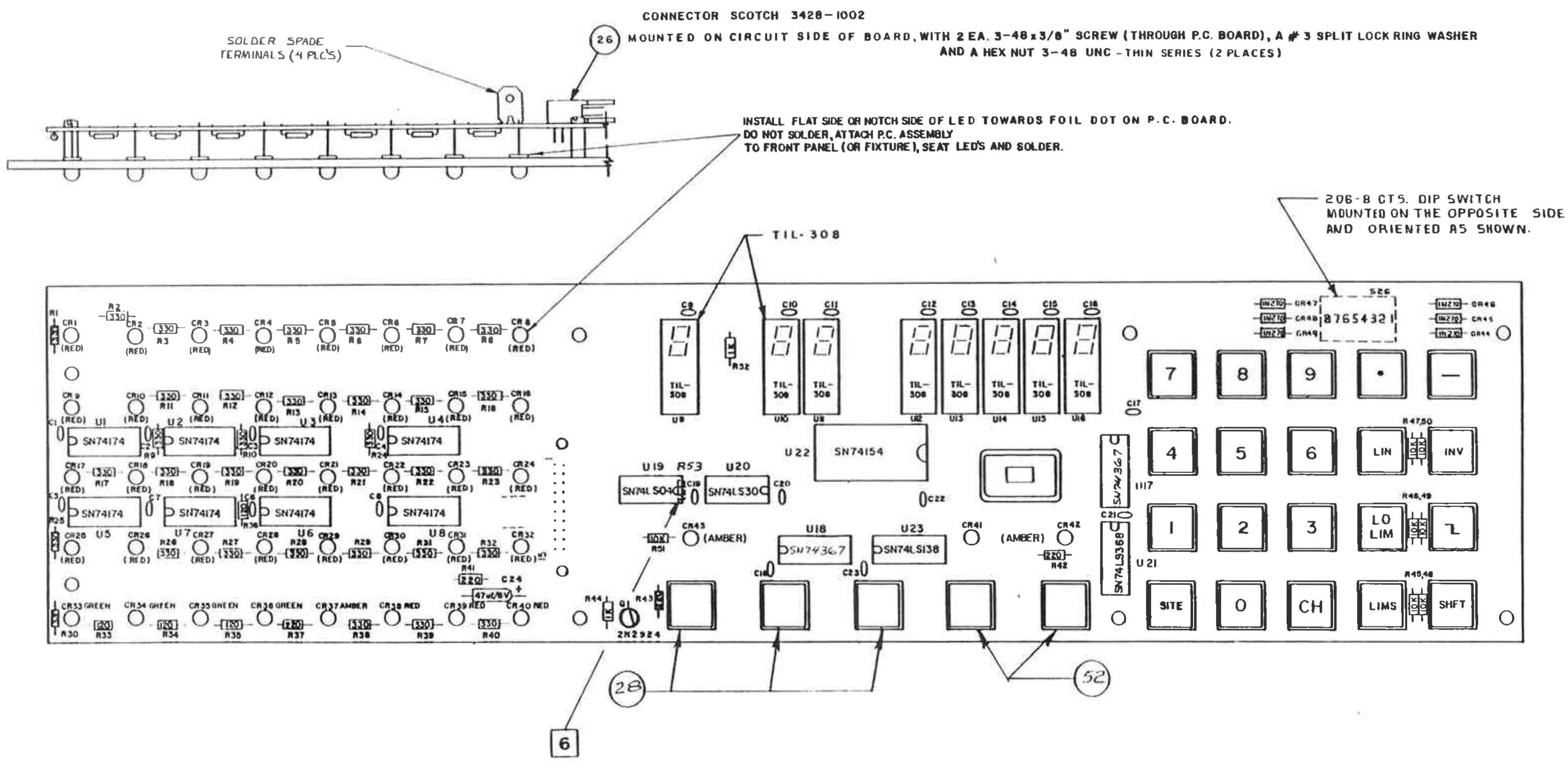
GND	+5V	I.C. TYPE
PIN 8	16	74174, TIL-308, 74367, 74LS138, 74LS368
PIN 7	14	74LS38, 74LS04
PIN 12	24	74154

FIRST USED ON MRC-1

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA 93117

SCHEMATIC
REMOTE TERMINAL FRONT PANEL

91C7127



NOTES:

1. UNLESS OTHERWISE SPECIFIED
   RESISTOR VALUES ARE IN OHMS, 1/4, 10%
   CAPACITORS ARE .1uF, 50V
2. P.C. BOARD 5185842
3. SCHEMATIC 91C7127
4. ALL TIL 308 7 SEGMENT DISPLAYS ARE TO BE SELECTED WITHIN A GRADE RANGE OF 2. EXAMPLE: 2 THRU 3; 3 THRU 4; 4 THRU 5; ETC.

FIRST USED ON MRC-1

REVISIONS	
H3	ADDED R53 UNDER U19
G3	U17 & U18 WAS SN74LS367 ECO 1946 10-20-80
F3	ADD PCO ... CHG. GRADE ...
F2	S26 AND CR44 THRU CR49 ADDED. ECO 1352 27 FEB 80 D.T.W.
E2	CHANGED "RAISE" & "LOWER" PUSHBUTTON COLORS. ECO 1481
C2	ADDED JUMPER ...
C2	FIBER WASHER DELETED FROM CONNECTOR MOUNTING PCO 1386 12 SEPT 79 D.T.W.
B2	ADDED NOTE #5 AUG. 20, 1979 ECO 1333 A.J.B.
B1	NOTE 4 ADDED. PCO 1086 27 JULY 79 D.T.W.
B	RELEASED FOR PRODUCTION 27 FEB 79 L.I.
A	REV. ARTWORK WAS 00 27 NOV. 78 A.J.B.

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA 93017

COMPONENT LAYOUT
REMOTE TERMINAL FRONT PANEL

TOL: FRACT. ± 1/32, .XX ± .030, .XXX ± .010, ∠ ± 1/2°			
DWN	A.J.B.	Oct. 10, 78	SCALE 1/1
CHK	F.XY	27 FEB 79	
ENG	HATT	27 FEB 79	20C2703 H3

CPU BOARD

Schematic 91D7132
Assembly 20B2710
PC Board 51B5849

I. PURPOSE

This module has six (6) functions:

1. CPU and Buffers
2. 2K EPROM and Priority Interrupts
3. I/O Preselect
4. Bit Rate Generator
5. Front-Panel Drive
6. Indicators and Controls for CPU Interface Board

II. ELECTRICAL ADJUSTMENTS

When power is applied to the unit for the first time, R30 should be adjusted. Turn R30 counterclockwise until CR4 (reset) illuminates. Then, turn clockwise until the LED goes off. Continue turning R30 for one more full turn. S1 is used to generate a *PF and *RESET signal, and is used mainly for troubleshooting. A jumper from U9 pin 1 to ground is used to disable the internal RAM on the CPU and is normally installed. A jumper between P1-10 and U1 pin 35 is used to supply power to the internal RAM on the CPU and is not normally installed.

III. THEORY OF OPERATION

Overall: The CPU generates the addresses from which data will be stored or retrieved. The address bus

consists of 16 bits, allowing 65536 (2^{16}) addresses. These lines are used on the CPU to select the PIA (Peripheral Interface Adapter), the EPROM (Erasable Programmable Read Only Memory), and the PIC (Priority Interrupt Controller).

The data bus (D0-D7) is used to carry the data between the CPU and other parts in the system. This bus is bi-directional. When the CPU writes data, the CPU outputs and the peripherals input. Conversely, when the CPU reads data, the CPU inputs and the peripherals output. The direction of data flow is controlled by the R/W (Read or Write) line. Data is read into the CPU when this line is high. The VMA (Valid Memory Address) output of the CPU signals to the address decoding logic that the address line has a valid address on it. No data transfers occur unless this line is high. Output line E (Enable) is a 1 MHz square used for bus timing. Data transfers occur when this line is high. BA (Bus Available) signals that the CPU has gone inactive as a result of a request generated by an external device, such as DMA (Direct Memory Access).

The PIC is used to sequence interrupts to the CPU by allowing higher priority devices to go first. The EPROM is used to store the program (or part of it). The PIA is used to drive the front panel along with six (6) miscellaneous functions. The bit rate generator is used to divide the 1 MHz E signal to approximately 19200 Hz, suitable to run 1200 or 300 baud.

A. CPU and Buffers

Y1 and U1 form a 4.00 MHz crystal oscillator, operating in the parallel resonant mode. C21 and C22 are incorporated to ensure that Y1 does not start oscillating in the third-overtone mode.

U9A disables the internal RAM of the CPU during power up and power down. If the jumper is inserted from pin 1 to ground, the internal RAM will always be disabled. This is the case when a RAM/ROM memory board is used in the system. The NMI input is used for a device requiring very fast service from the CPU. The jumper from P1-10 to U1 pin 35 is used to power the ON CPU RAM; it is not used if a RAM/ROM memory board is used in the system. The HALT input stops the CPU after it is finished executing the present instruction. The CPU then releases itself from the bus and sets the BA (U1, pin 7) output high. This action signifies to the device that pulled HALT low to commence transfer of data on the bus. Address lines A0 through A7 are buffered by tri-state octal buffer U5; likewise, lines A8 through A15 are buffered by U6. The enables for U5 and U6 are controlled by VMA from the CPU. In this way, the address lines to the rest of the system are only active when valid addresses are available. VMA is also gated with the *DMA input by U10A. This allows a DMA controller to simulate VMA to the rest of the system by pulling *DMA low. Data lines D0-D3 are buffered by U7; likewise, D4-D7 are buffered by U8. U10B and U10C are used to enable U7 and U8. One input of U10B and U10C is fed out of phase from the R/W line so only one can be enabled at a time. The other input of U10B and U10C is driven by U17B, which only allows the buffers to be activated if BA is low and if none of the I/O or memory is activated on the CPU board. This is required to prevent both the bus buffers and the PIA or EPROM from trying to feed data to the CPU simultaneously.

B. 2K EPROM and Priority Interrupts

U4 is addressed at locations F800-FFFF which are decoded by U19. Address lines A11-A15 are applied to the inputs of U19 along with VMA and R/W. The R/W is including so that a write operation to

F8000-FFFF will not cause a buss conflict between U4 and the CPU.

The PIC (U3) is addressed at locations FFE0-FFFF which are decoded by U18, U15B and U17A. Address lines A5-A15 are applied to the inputs U18 and U15B along with VMA. During normal operation, address lines A1 through A4 are passed from the A1-A4 inputs of U3 to outputs Z1-Z4 which allows normal addressing of the EPROM. If an interrupt input of U3 is pulled low, it will pull its IRQ output low, generating an interrupt of the CPU. In case of an interrupt, the CPU will fetch the address of the service routine at locations FFF8 and FFF9. These two addresses are decoded by U3, and used to modify its Z1-Z4 outputs in accordance with which interrupt is active, allowing a modified address to reach U4. In this manner, there are eight (8) interrupt service addresses instead of one (1).

C. I/O Preselect

I/O is assigned addresses 8000 through 81FF in this system. Rather than decode all 16 address lines on each I/O board, an I/O preselect system is used. Address lines A9-A15 and VMA are gated together in U16A, U16B and U15A to form *PRE.

This signal goes low when a valid address from 8000 to 81FF is on the address bus. This signal is inverted by U12C to form an active high signal and put on the bus. Most I/O boards conform to the following addressing convention:

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	0	0	0	0	T	T	T	B	B	B	B	R	R

Where:
1 = High
2 = Low
T = Board Type
B = Board Number
R = Register Select

D. Bit Rate Generator

IC's U13 and U14 along with U10D form a synchronous divide by 52 circuit. U14 counts from 3 to 15 providing a division of 13 while U13 divides the output of U14 by 4. In this manner, a 1923Ø Hz square wave is generated at the baud output. This clock is used by ACIAs (Asynchronous Communications Interface Adapters) to provide data at either 1202 baud or 300.5 baud, which is within 0.2 percent of the standard 1200 and 300 baud.

E. Front-Panel Drive

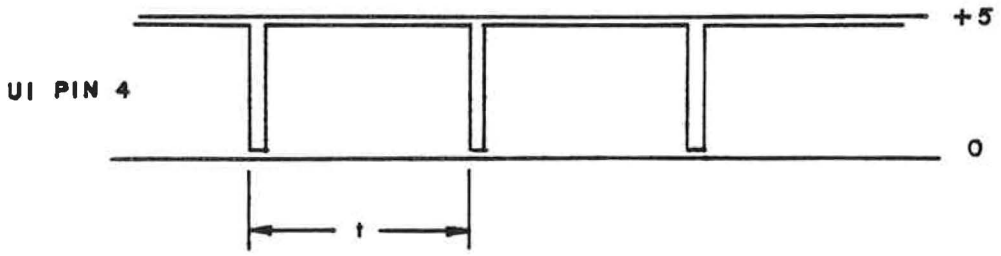
U2 is used to drive the front panel and is located at addresses 8004 through 8007. There are three chip select inputs on the MC6821; 2 active high and 1 active low. The active low input is connected to *PRE which will go active with addresses 8000-81FF. Address lines A6, A7 and A8 are NOR'ed together at U16C and fed to the first active high input. Address line A2 is applied to the second active high input to U2 providing the "04" offset to the base address of 8000. Lines CA1 and CA2 are used as interrupt inputs and allow interrupts every 16.7 ms for 60 Hz or 20 ms for 50 Hz, and also for loss of main power. The interrupt output of U2 is connected on the board to interrupt input 7 of U3. This is the highest priority interrupt. Output lines PA6 and PA7 are applied to the CPU interface card and used for an external maintenance override and failsafe outputs. Output line PB6 and input line PB7 are used for control of the low-battery detector on the CPU interface card. Lines PA0-PA5 are bi-directional and carry data to and from the front panel. Output lines PB0-PB4 are used

to access various elements on the front panel.

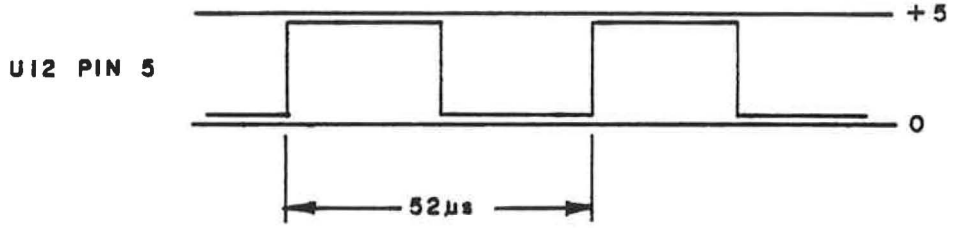
F. Indicators and Controls for CPU Interface Board

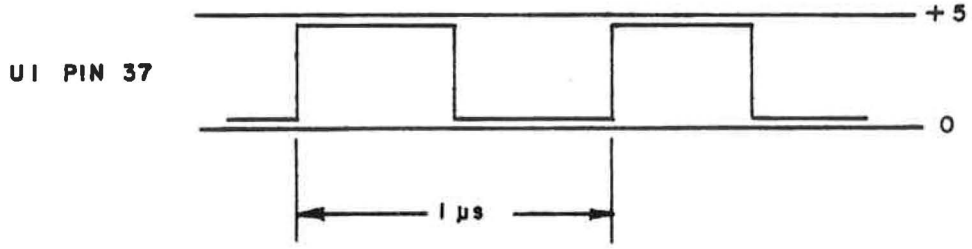
Switch S1 is connected from *PF to ground and is used to simulate a power down/power up sequence. This switch is mainly used for troubleshooting. CR4 indicates activity of the reset line and is used to adjust the power fail threshold potentiometer R30. CR1-CR3 are provided to give a visual indication of operation of the +15, -15 and +5V power sources.

IV. TIMING DIAGRAMS



FOR 50 Hz t = 20 ms
FOR 60 Hz t = 16.7 ms





V. TROUBLESHOOTING

1. CPU and Buffers

A. Verify +5, +12 and -12 volts are present on board.

B. The RESET LED (CR4) should be OFF except when switch S1 is depressed or during initial power up.

C. Verify the ENABLE signal by checking IC U1 pin 37. A 1 MHz square wave should be observed. If this signal is not present, verify proper +5 volt supply voltage is present at pin 8. Pins 1 and 21 should be grounded. If proper IC voltages are present, suspect the crystal or MC6802 IC.

D. If RAM enable jumper is present, IC U1 pin 36 should be low. If no jumper is present, verify pin 36 of IC U1 is high.

E. Verify the following levels on IC U1 (MC6802):

*HALT	Pin 2	=	+5 volts (±.25V)
*NMI	Pin 6	=	+5 volts (±.25V)
BA	Pin 7	=	0 volts (±.25V)
*RESET	Pin 40	=	+5 volts (±.25V)

F. Check IC U1 pin 4 for real time clock interrupt signal (60 Hz pulse). If this signal is absent, check IC U2 pin 40 for the real time clock signal from the CPU interface card.

G. Check for activity on the Read/Write line, pin 34, and valid memory address, pin 5. Both lines should toggle in a non-periodic manner. If this is not observed, the problem may be in the microprocessor IC or another IC connected to these lines.

H. Using an oscilloscope, observe the address and data lines,

pins 9 through 33. These lines are three-state and often appear to float in between HI and LOW. The inputs and outputs of the SN74LS244 should appear similar. The data and address lines may be observed using an extender card and checking the even numbered pins between 12 and 58.

2. 2K EPROM and Priority Interrupt

A. Check IC U4 (TMS2716) for proper supply voltages.

+5V	Pin 24
-5V	Pin 21
GND	Pin 12
+12V	Pin 19

B. Attach an oscilloscope to chip select (pin 18) of IC U4. After pushing the reset push button, two low-going pulses should be seen. If pulses are not present, check IC U19.

C. Check data and address lines for activity.

D. Observe pin 23 of IC U3. It should be normally high with low-going pulses approximately every 20 ms. If these pulses are not present, check IC U3 pin 11 for these pulses.

3. I/O Preselect

A. Check the inputs of IC U16A and IC U16B for activity coincidental with activity on addresses A9 through A14.

B. Check pin 8 or IC U15A for low-going pulses. If no pulses are observed, check input signals on pins 9, 10, 12 and 13.

C. Output from the Inverter Buffer (IC U12C) should look similar to IC U15A pin 8, only inverted.

4. Bit Rate Generator

A. Check for the 1 MHz ENABLE signal on pin 2 of IC U13 and IC U14. If signal is not present, trace back to the origin, IC U1 pin 37.

B. Check each pin of IC U13 and IC U14, which is pulled high by R7 to verify a "HIGH" very near +5 volts.

C. Pin 15 of IC U14 should have a 1 µs pulse every 13 µsec. IC U13 pin 13 should have a 52 µsec square wave.

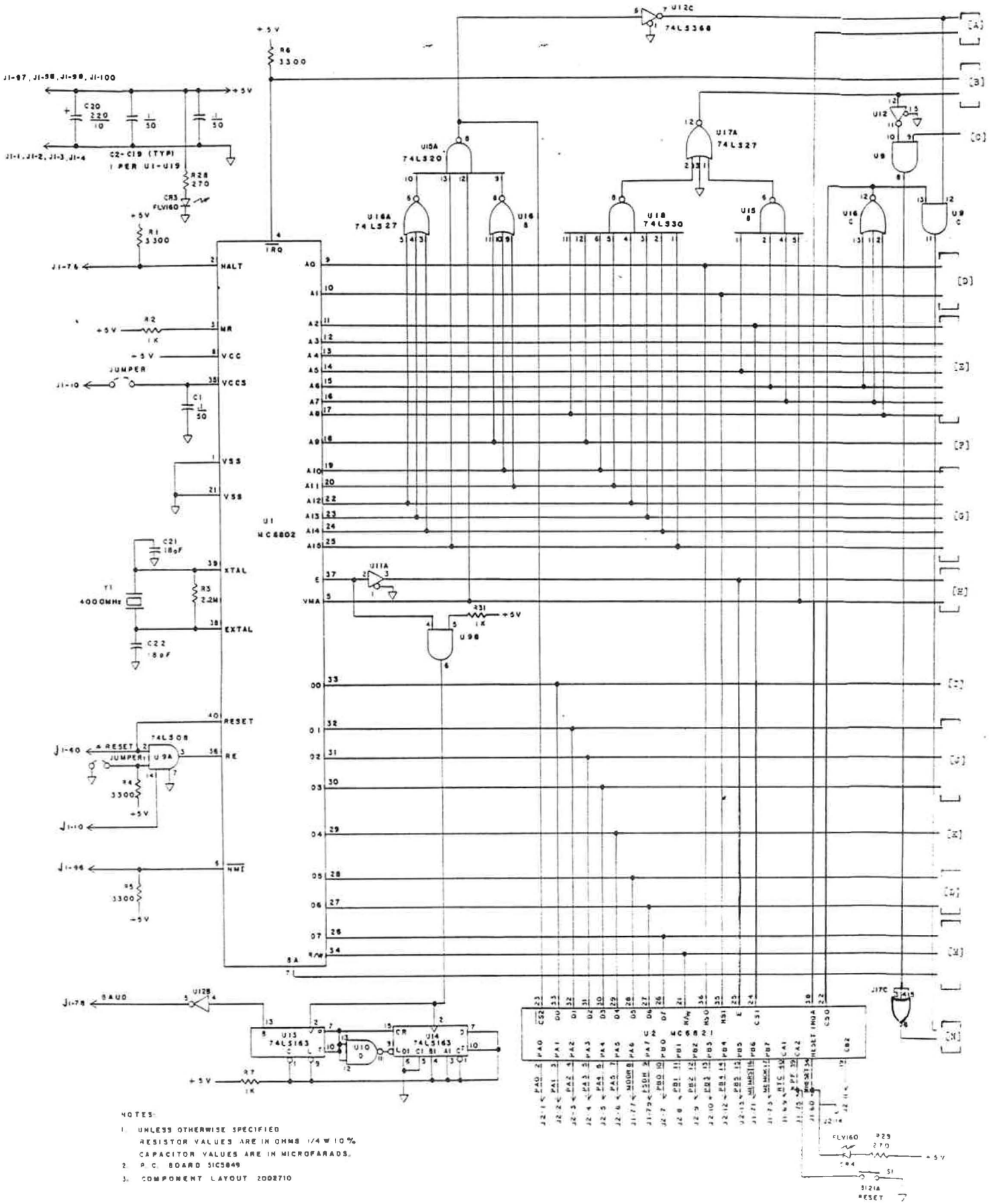
MOSELEY ASSOCIATES, INC. SANTA BARBARA RESEARCH PARK, GOLETA, CALIFORNIA 93017			
SCHEMATIC MRC-1 CPU			
TOL: FRACT. ± 1/32, .XX ± .030, .XXX ± .015, ∠ ± 1/2°			
DWN	L.I.	10 NOV 78	SCALE: NONE
CHK	FXY	20 FEB 79	91D7132 D∅
ENG	HATT	21 FEB 79	

REVISIONS

REV	DESCRIPTION
A	RELEASED FOR PRODUCTION 21 FEB 79 JAM
B	REMOVED TIME USING PIN 1 TO SIDE PIN 2. ECO1193 28 JUN 79 JAM
C∅	REMOVED R10 - R15, R24 & R23. ECO 1448. 6 NOV 79 BWF
D∅	ECO 1549, ECO 1567 CHANGED U5-U8 FROM 81LS97 DRIVERS TO 74LS244 DRIVERS, U6 PINS 18 19 AND U5 PINS 16 19 SWITCHED FROM VMA TO BA 1/21/80 JRM

DATE

MGMT. APPR.



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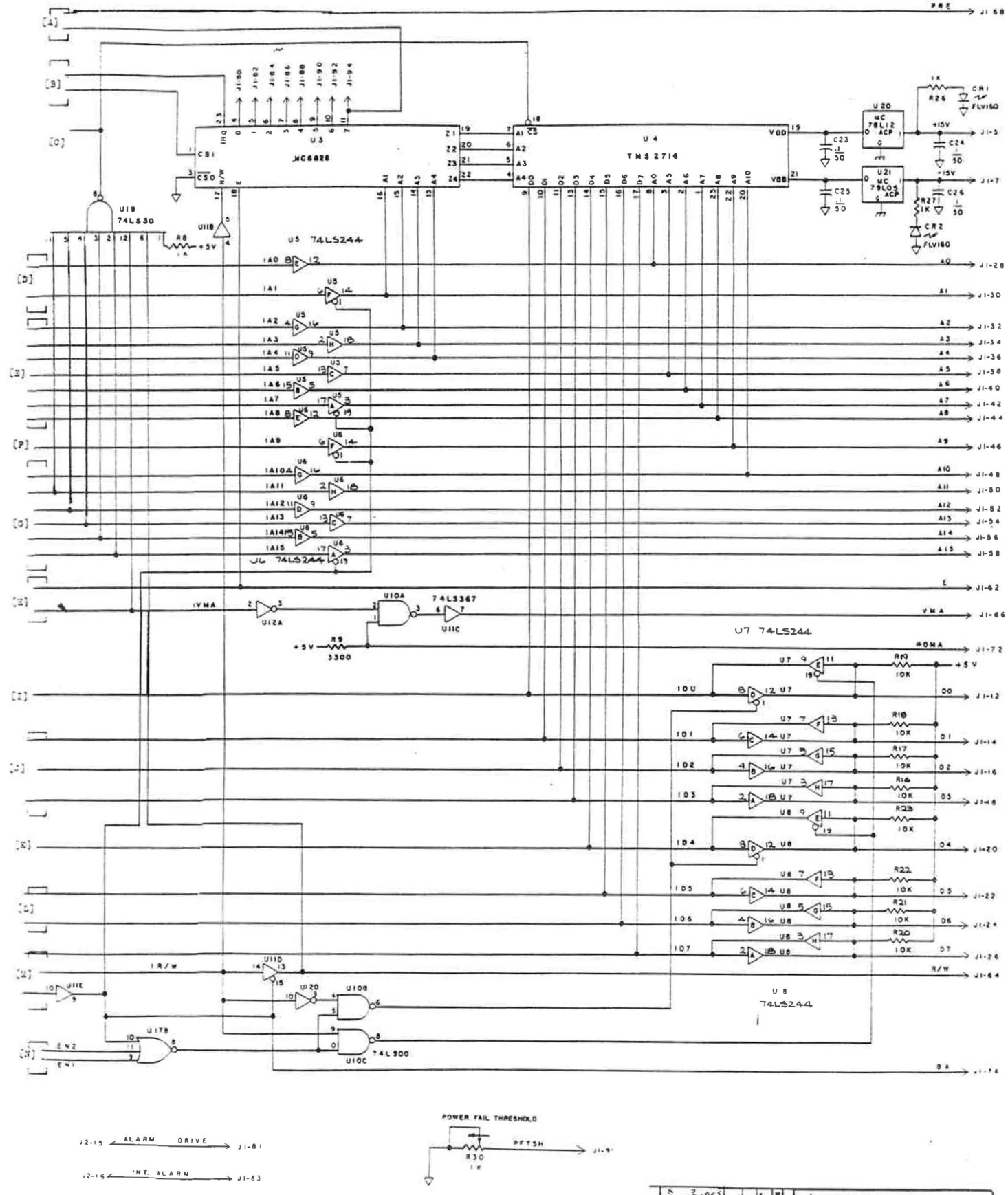
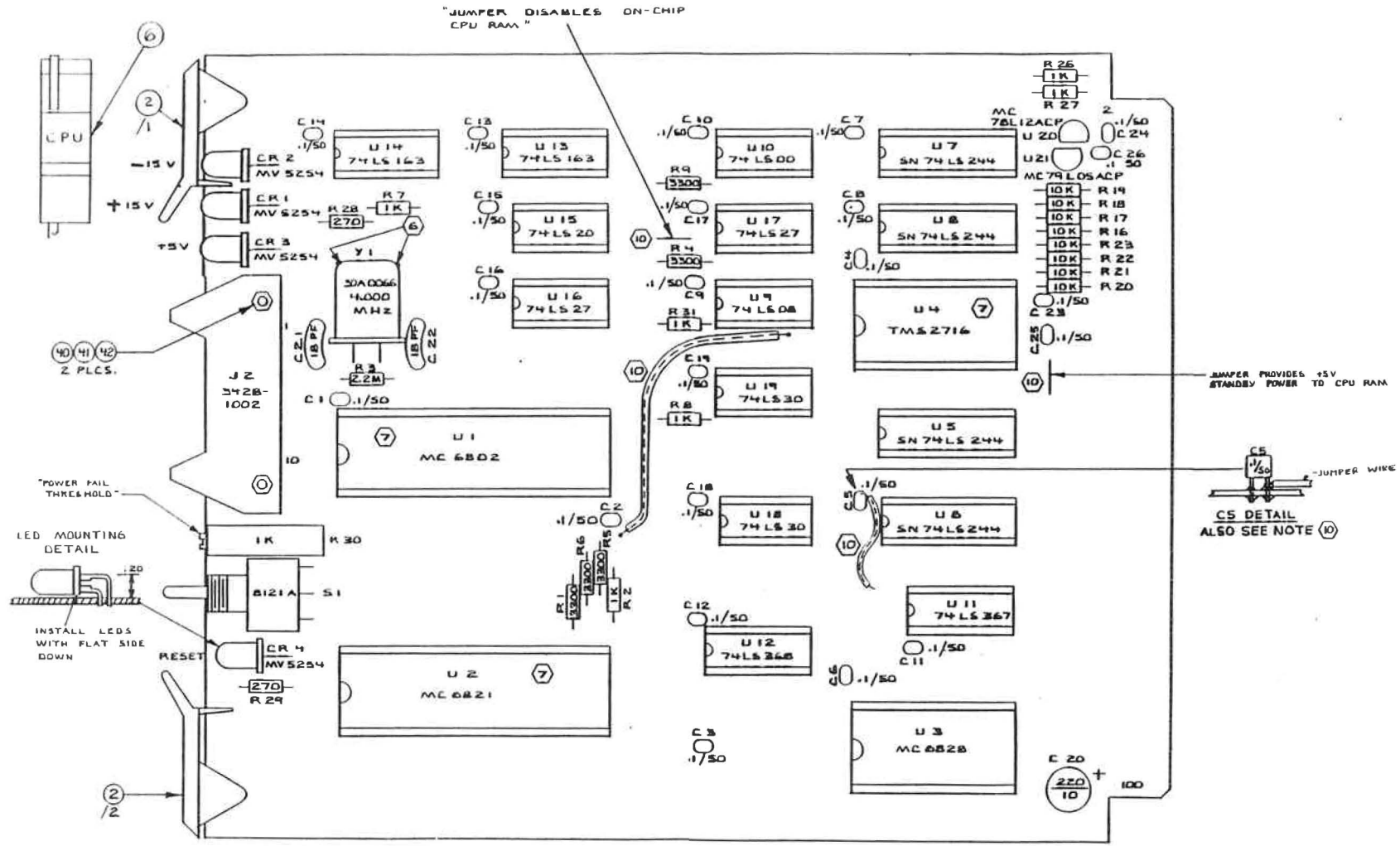

PRE
U3
MC6828
U4
TMS 2716
U19
74LS30
U5 74LS244
U6 74LS244
U7 74LS244
U8
74LS244
U10A
74LS367
U11C
U10C
74LS00
VMA
R/W
E
+5V
3300
ALARM DRIVE
INT. ALARM
POWER FAIL THRESHOLD
PFTSH
R30
MOSSLEY ASSOCIATES, INC.
SCHEMATIC
MRC-1 CPU
9107132



NOTES:

1. UNLESS OTHERWISE SPECIFIED RESISTOR VALUES ARE IN OHMS, 1/4 W, 10 %. CAPACITOR VALUES ARE IN MICROFARADS.
2. P.C. BOARD SIC 5849-11,-21
3. SCHEMATIC 910 7132 REV. DØ
4. ALL TRANSISTORS SOLDERED WITHOUT SOCKETS
5. ALL I.C.'S ARE MOUNTED IN SOCKETS

(6) TACK SOLDER Y1 TO PAD 2 PLCS.

(7) I.C. SHOWN FOR REFERENCE ONLY TO BE SPECIFIED AND INSTALLED AT ANOTHER ASSEMBLY LEVEL.

(10) ALL JUMPERS ARE #30 AWG, SINGLE STRAND INSULATED WIRE-WRAP WIRE, ADD JUMPERS AS SHOWN.

AT LOCATION C5: WRAP AND SOLDER JUMPER WIRE AROUND LEAD OF CAPACITOR. INSERT LEADS OF CAPACITOR INTO BOARD AND SOLDER.

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA

COMPONENT LAYOUT
P.C. ASSEMBLY CPU

SCALE:

2002710 H7

ITEM NO.	DESCRIPTION	REF. DESIG.	STOCK NO.	QTY
42	HEX NUT THIN SERIES #3-48		1030055	2
41	LOCKWASHER, SPLIT RING #3		1030089	2
40	S.H. SCREW 3-48 X 3/8		1030030	2
39				
38	I.C. SOCKET AMP 640379-1	U1,2	3250099	2
37	" " 640361-1	U3,4	3250073	2
36	" " 640464-1	U5-8	3250057	4
35	" " 640369-1	U11-14	3250032	4
34	I.C. SOCKET AMP 640357-1	U9,10,15-19	3250024	7
33	TRANSISTOR MC 79 L05ACP	U21	3650132	1
32	TRANSISTOR MC 78 L12ACP	U20	3650124	1
31	I.C. MC 6825P	U3	3710035	1
30				
29				
28				
27	I.C. SN 74LS244	U5-8	3660859	4
26	" SN 74LS368	U12	3660875	1
25	" SN 74LS367	U11	3660867	1
24	" SN 74LS163	U13,14	3660826	2
23	" SN 74LS30	U18,19	3660735	2
22	" SN 74LS27	U17,16	3660727	2
21	" SN 74LS20	U15	3660719	1
20	" SN 74LS08	U9	3660693	1
19	I.C. SN74LS00	U10	3660669	1
18	L.E.D. MV5254	CR1-4	3390150	4
17	POT 1K	R30	4630075	1
16	RESISTOR 2.2M	R3	4410619	1
15	" 10K	R16-23	4410379	8
14	" 3300	R1,6,5,9,4	4410304	5
13	RESISTOR 1K	R7,28,31, 26,27	4410247	6
12				
11				
10	RESISTOR 270	R28,29	4410171	2
9	CAPACITOR .1/50	C1-19 C23-26	4310207	23
8	" 18 PF	C21,22	4210084	2
7	CAPACITOR 220/10	C20	4230186	1
6	LABEL	10A1068-1	3430287	1
5	CRYSTAL 30A0066	Y1	3340163	1
4	CONNECTOR SCOTCH 3428-1002	J2	3110305	1
3	SWITCH 8121A	S1	3170065	1
2	EJECTOR VERO 012409/14/2		1250075	1
1	PC BOARD	SIC5849-11-21	3471927	1

ITEM 1 & NOTE 2 ADDED PER ECO 1903 AJA
ADDITION TO NOTE 10 AND C5 CHANGED TO 18PF
ADD JUMPER NOTE 10 DELETED PER ECO 1903 AJA
ADD ITEM 6
REVISED & REDRAWN WAS 20D2710 ECO 1844 5 MAR 81 BWF

REVISIONS | DRAFT. APPR. | DATE

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA 93017

COMPONENT LAYOUT
P.C. ASSEMBLY CPU

TOL FRACT. = 1/32. XX = .030. XXX = .010. < = 1/2°
DWN BWF MARCH SCALE:
CHK
ENG
20D2710 H6

CPU INTERFACE

Schematic 91C7215
Assembly 20C2781
P.C. Board 51C5907

I. PURPOSE

This module has eight functions:

1. Power failure sensing.
2. Power-on reset.
3. 50-Hz or 60-Hz real time clock.
4. Battery Backup Switching and Charging.
5. Low Battery Voltage Sensing.
6. Output Relays for Failsafe and Maintenance Override Indication.
7. Connection for Audible Alarm Muting.
8. Auto-restart in the event of malfunction.

II. SPECIFICATIONS

1. The maximum battery charging current is 75 mA. This is suitable for up to 7.5 AH Gel-Cell batteries. For a larger battery, use an external charger.
2. For a battery voltage of 6 V, it is float-charged at 6.75 volts. The battery is considered discharged when the battery voltage under load drops below 5.0 volts. The maximum voltage applied to the battery terminals should not exceed 7.0 volts.
3. The voltage and current ratings of the maintenance override and failsafe relays are 24 VDC and 1A. Relay contacts are brought on to the rear panel connector.

4. Aural external drive output

   maximum voltage = 12 V

   maximum current = 25 mA

   maximum current from +5 V output = 25 mA (internal defeat)

   Power user supplied, output is O.C. sink to chassis

III. ELECTRICAL ADJUSTMENTS

1. Battery Charge Voltage (R28): This control is set at the factory for 6.75 V across the binding posts. This is the correct float-charge voltage for the supplied batteries and should not need adjustment.

IV. THEORY OF OPERATION

1. Power Failure Sensing

   AC from the secondary of the power supply transformer is suplied at pins P1-11 and P1-13. The AC is full-wave rectified with CR1 and CR2, then filtered using C1. A potentiometer is connected to P1-91 and ground on the CPU board. R1, R2 and the potentiometer form an adjustable attenuator that is used to compensate for variances in local line voltage and frequency. U1A, along with R4, form a comparator with hysteresis. The threshold is maintained constant with CR3, a 3.1 V Zener diode. When normal line voltage is applied, the positive input of U1A is above the 3.1 V, causing the output to be high. If the AC supply should fail for a period of time (nominally 10 ms), the positive input to the comparator will fall below 3.1 V and cause the output *PF to go low.

2. Power-On Reset

When power is applied to the unit, *PF will go high, allowing C4 to charge through R8. This voltage is applied to the negative input of a comparator consisting of U1B and the 3.1 V reference. After approximately 400 ms, the negative input will reach the reference level causing the output of U1B to go low, which removes the base drive to Q1 allowing the collector to be pulled high by R14. When power is removed from the unit, *PF will go low discharging C4 through R7 and CR4. Operation is much quicker in this direction and reactivates *RESET approximately 3 ms after *PF goes low.

3. Real Time Clock

AC from the power supply transformer secondary is supplied at P1-13 and rectified by CR5. This is applied through voltage divider R15, R16 to the positive input of a voltage comparator (U1C). On the output of the comparator is a rectangular wave having a duty cycle of about 55%.

4. Battery Backup Switching and Charging

Fifteen volts from the power supply is regulated down to 7.45 volts by U2. This is passed through CR10 to the battery terminal. R28 is adjusted such that 6.75 V is applied at the battery terminals with no load. R29 is used to protect U2 in case of a short across the battery terminals. During normal operation, Q3 is biased on through R26 by the +15 V supply; this allows the main 5 V supply to be applied to the 5 V standby bus. When either the +15 V or main 5 V supply fails, the base of Q5 is pulled toward ground by either CR7 or CR8. This forward biases Q4 allowing the battery voltage to be passed to the 5 V

standby bus. The 6 volts at the battery terminals is reduced to an acceptable voltage by the voltage drops of CR9, Q4 and Q5.

5. Low Battery Voltage Sensing

A comparator (U1D) is used as a bistable multivibrator. When main power is not applied, the voltage at the output of U1D will reflect the voltage of the 5 V standby bus. This voltage is dropped 0.6 V by CR6 and fed back to the positive input of U1D to keep the output high. If the voltage at the positive input falls below the reference voltage, the output of U1D will be forced low. This occurs when the 5 V standby bus falls to 3.1 V. This removes the voltage at the positive input which effectively latches the output low. Upon reapplication of main power, C6 filters out any glitches that might alter the state of U1D. If the output of U1D did go low, this will tell the computer that the battery failed during the power outage. To reset the latch, a pulse of at least 10 ms is applied by the CPU to P1-71. This causes Q2 to conduct, removing the reference voltage to the comparator. The voltage divider of R22 and R25 is used to provide at least 0.4 V at the positive input to cause the output to go high when the reference voltage is removed.

6. Maintenance Override and Failsafe Relays

To activate the Failsafe output, P1-79 is set high from the CPU board. U5 ensures that the relay will not close when the *RESET line is in its low state, thus preventing a "glitch" when the unit is plugged in or the reset button is pushed. Each gate of U5 has an open-collector output which can sink the current required to activate

a relay when both inputs to the gate are in their "high" state. Voltage regulator U4 provides +12 V to the other side of the coil. When the relay is activated a closure occurs between pins 3 and 4 of the rear connector.

The Maintenance Override output is almost identical. P1-77 is set high from the CPU board to activate the relay. A closure will then be observed between pins 1 and 2 of the rear connector.

The closure between the Failsafe terminals will be observed when the unit is not in a failsafe condition. The closure across the Maintenance Override terminals will be observed when the unit is in a Maintenance Override condition.

In boards installed at an MRC-1 Control Terminal these relays are never activated and serve no function. The relays are installed, however, to preserve interchangeability with boards installed in remote terminals.

These relays are capable of switching a load of up to 24 VDC at currents of up to 1 ampere. Inductive loads (relay coils, etc.) should have a "clamping" diode wired across them to inhibit negative voltage spikes. External relays should be used when it is desired to switch greater loads (or AC loads).

These relays may also be interfaced with transistor-transistor logic (TTL) digital circuits. The relay contacts should be wired so that one side is referenced to the digital common (ground), and the other relay contact to the digital input. A pull-up resistor may be necessary, and it is advisable to wire a 1 μF capacitor and a 100-ohm

resistor (in series) across the relay output to suppress contact bounce. See FIGURE I.

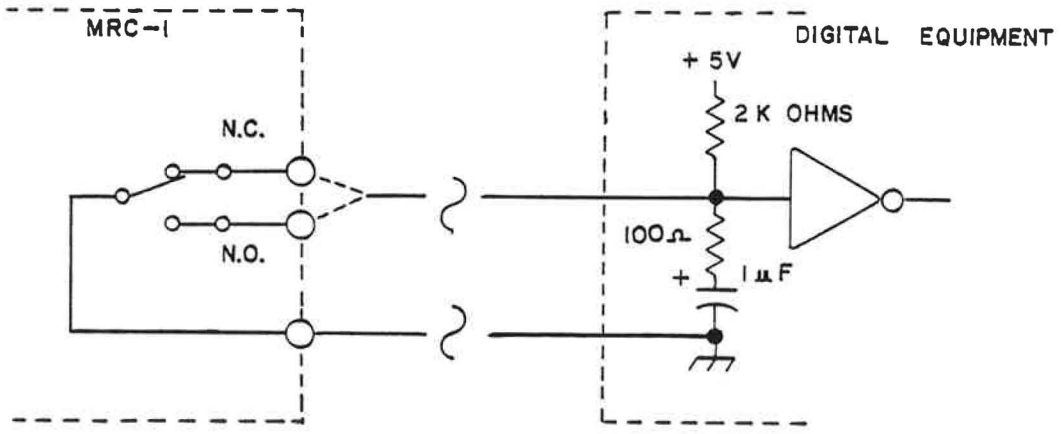


FIGURE I

7. Auto-Restart in the Event of Program Malfunction

Integrated circuit U3 (74LS123) is a dual retriggerable monostable multivibrator ("one-shot"). During normal program operation, line P1-71 is continually strobed from the CPU board. Each pulse reaching pin 1 of U3 "retriggers" the first stage of U3 for another 500 msec. The output at pin 13 will remain high as long as pulses at pin 1 arrive at least every 500 msec. Should these pulses cease (because for any of a number of reasons the program has ceased running properly), the output at pin 13 falls to ground. The falling edge at pin 9 causes a 1-msec pulse at pin 5. If the jumper marked "Auto-Restart" has been installed, transistor Q6 is switched on, causing the *RESET line to fall to ground and re-initiating operation of the program.

The jumper marked "Continuous Restart" enables continuous retries, should the first attempt to restart be unsuccessful. This feature does not appear on some early production units.

VI. TROUBLESHOOTING

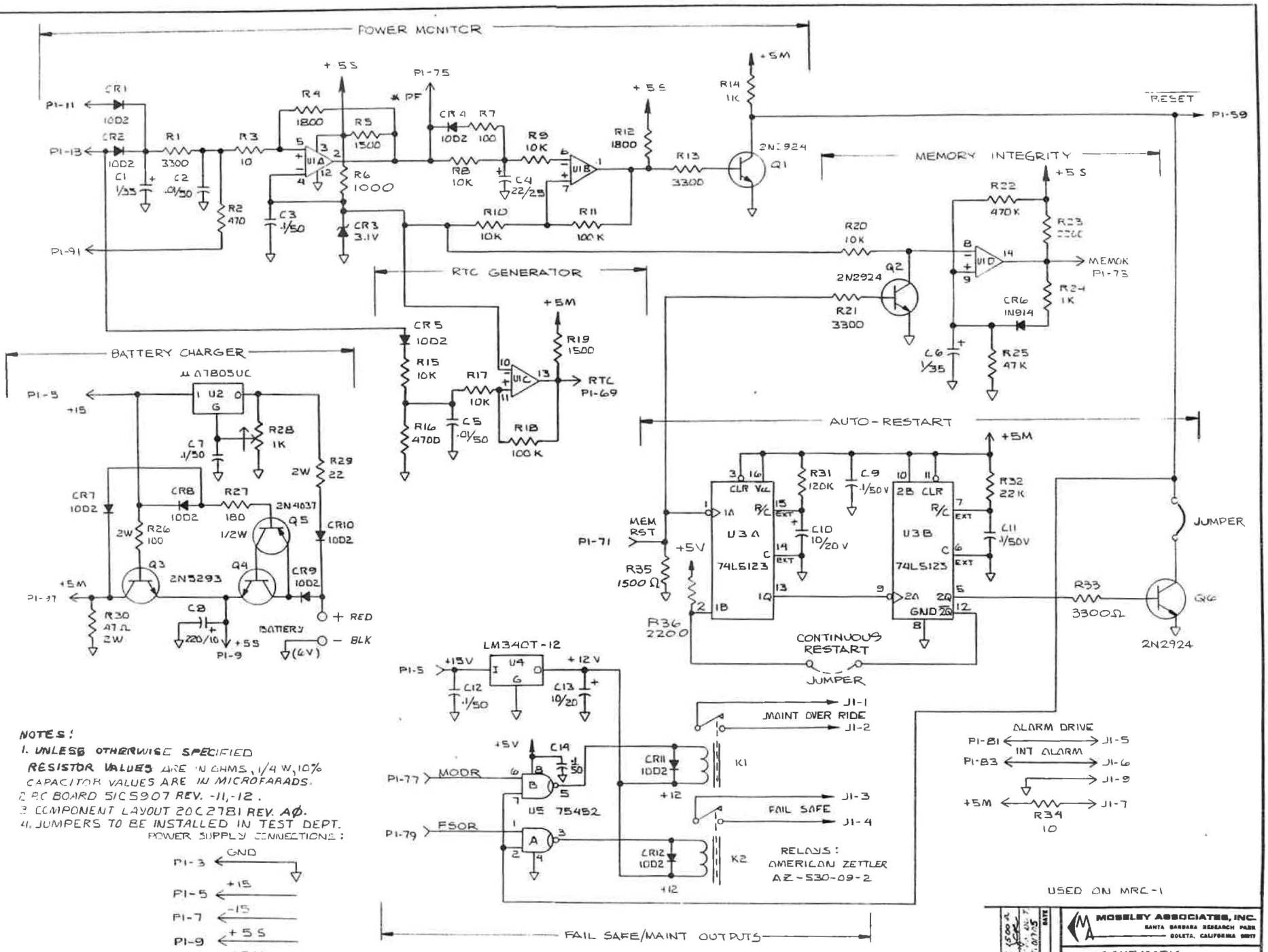
1. Read the section on troubleshooting presented in Section 7.4.

2. Specific areas on this board that must be functional for any operation of the CPU are as follows:
   a. Verify presence of +5 V on the 5 V standby bus. If it is not there, check for short to ground or Q3 open.
   b. Check for waveform at P1-11 and P1-13 (AC in). If not there, check CR1, CR2, C1, and the two 100-ohm resistors mounted on the power supply.
   c. Check voltage at pin 4 of U1. It should be between 3.0 and 3.2 volts. If not, check U1 and CR3.
   d. Check waveform at U1 pin 2 (*PF). If it is low, try readjusting the trim potentiometer on the CPU board (R30). If this does not correct it, check for shorts or replace U1.
   e. If *PF is normal but *RESET is still low, check for at least 4.5 V at pin 6 of U1 and 2.5 to 3.5 V at pin 7. If these are normal, pin 1 of U1 should be less than 0.5 V. If not, suspect U1. If so, the collector of Q1 (P1-59) should be near +5 V. If not, check U3 pin 5, which should be near ground. If not, suspect U3. If U3 pin 5 is indeed near ground, suspect Q1, Q6, or a short ground at P1-59.
   f. Check waveform at U1 pin 13. If it is not correct, suspect CR5 or U1.

3. Circuits that will not stop operation of the CPU are:
   a. Maintenance override and failsafe drivers can be checked with a VOM; most probable cause of failure is U4 or U5.

b. When main power is applied to the unit, U1 pin 14 should be near +5 V. If it is not, try momentarily grounding pin 8. If pin 14 is still low, suspect CR6, C6 or U1.

c. If voltage at the red (+) battery terminal is not 6.75 V ±0.1 V, with the battery disconnected, check the voltage on R29. If should be approximately 7.45 V. If not, suspect U2, or R28.



NOTES:

1. UNLESS OTHERWISE SPECIFIED
   RESISTOR VALUES ARE IN OHMS, 1/4 W, 10%
   CAPACITOR VALUES ARE IN MICROFARADS.
2. PC BOARD SICS907 REV. -11,-12.
3. COMPONENT LAYOUT 20C2781 REV. AØ.
4. JUMPERS TO BE INSTALLED IN TEST DEPT.

POWER SUPPLY CONNECTIONS:

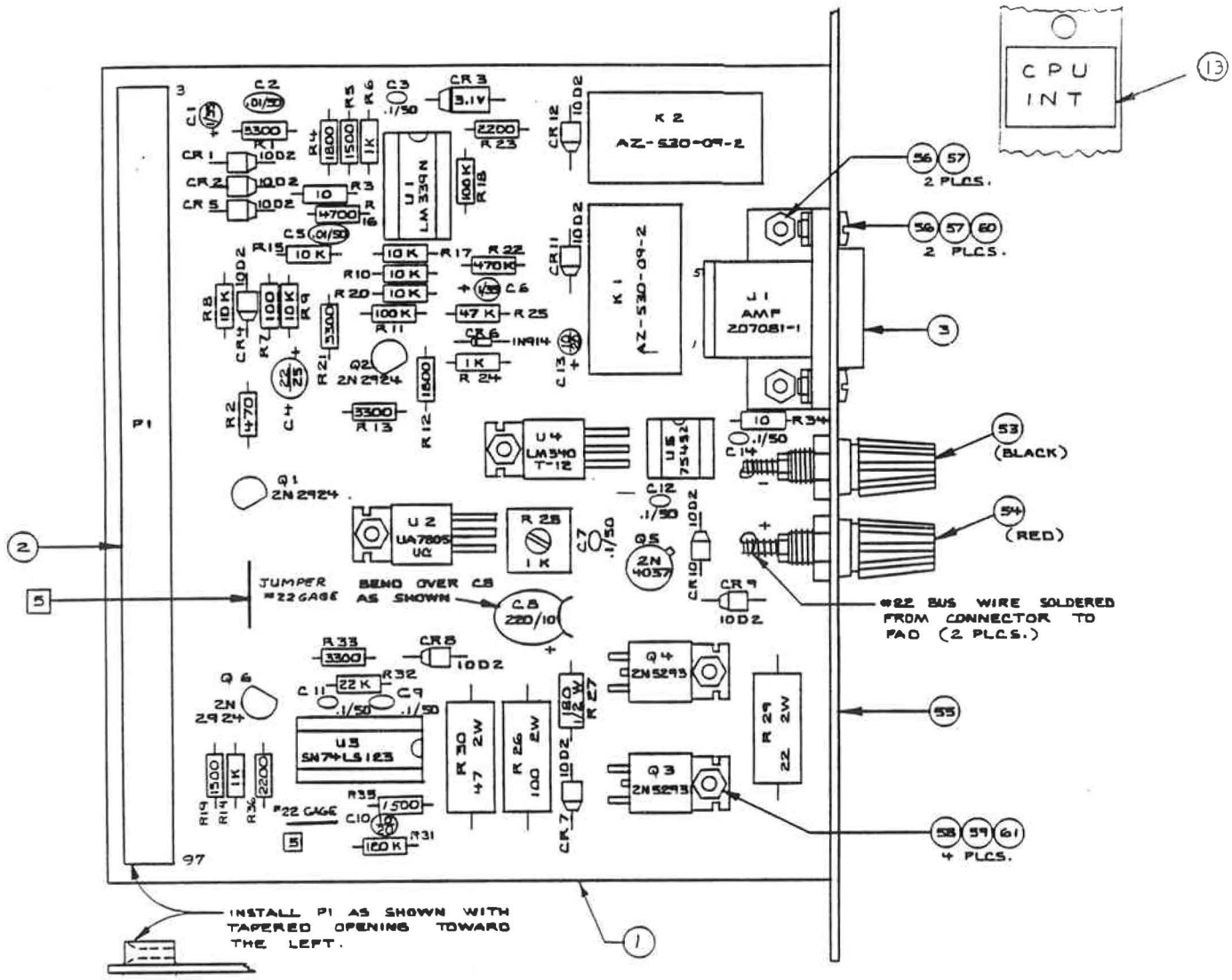
- P1-3 ← GND
- P1-5 ← +15
- P1-7 ← -15
- P1-9 ← +5S
- P1-97 ← +5M

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA 93117

SCHEMATIC
CPU INTERFACE

DWN RJB 5-11-80
CHK JCC 5-14-80
ENG DJD 5-22-80

9107215 BØ



NOTES :

1. UNLESS OTHERWISE SPECIFIED RESISTOR VALUES ARE IN OHMS, 1/4 W, 10 %. CAPACITORS ARE IN MICROFARADS.
2. P.C. BOARD SIC 5907 REV. -11,-21.
3. SCHEMATIC 91C 72/5 REV. AØ

REVISIONS		DATE	APPR.
BØ	AØ RELEASE TO PRODUCTION PER ECO 1145	19 SEPT 80	
	R6 WAS 33 Ω, R35 WAS 2500 Ω, ADDED R33 & R34 TO P/C CONFIG. PER ECO 1143	22 APR 80	

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA 93017

COMPONENT LAYOUT
CPU INTERFACE ASSY.

TOL: FRACT. ± 1/32, .XX ± .030, .XXX ± .010, ∠ ± 1/2°

DWN	BWF	24 MAR 80	SCALE: 2X1
CHK	[illegible]	24 MAR 80	20C2781 BØ
ENG	[illegible]	22 APR 80	

ITEM NO.	DESCRIPTION	REF. DESIG.	STOCK NO.	QTY.
61	SPLIT RING LOCKWASHER #6		1090596	4
60	SPLIT RING LOCKWASHER #4		1050632	2
59	NUT 6-32 THIN SERIES		1090554	4
58	SCREW B.H. 6-32 X 1/4		1090182	4
57	NUT 4-40 THIN SERIES		1050590	4
56	SCREW B.H. 4-40X5/16		1050145	4
55	PANEL	5A2640	2060374	1
54	BINDING POST EFJ 111-202	RED	3290004	1
53	BINDING POST EFJ 111-203	BLACK	3290012	1
52				
51	RELAY AZ-530-09-2	K1,2	3270113	2
50				
49	DIODE IN914	CR 6	3600053	1
48	" SZ 3.1 1%	CR 3	3610169	1
47	DIODE 10D2	CR1,2,4,5,7-12	3610003	10
46				
45	" 10/20	C 10,13	4280079	2
44	" 220/10	C 8	4280186	1
43	" 22/25	C 4	428009E	1
42	" .1/50	C3,7,9,11,12,14	4310207	6
41	" .01/50	C2,5	4310132	2
40	CAPACITOR 1/35	C1,6	4280038	2
39				
38	POT 1K 0.5 W	R 28	4630067	1
37				
36	RESISTOR 470	R 2	4410205	1
35	" 10	R 3,34	4410023	2
34	" 100	R 7	4410122	1
33	" 47K	R 25	4410452	1
32	" 1K	R6,14,24	4410247	3
31	" 1500	R5,19,35	4410262	3
30	" 1800	R12,4	4410270	2
29	" 2200	R23,36	4410288	2
28	" 3300	R 1,13,21,33	4410304	4
27	" 4700	R 16	4410338	1
26	" 10 K	R8-10,15,17,20	4410379	6
25	" 22K	R 32	4410411	1
24	" 100 K	R 11,18	4410494	2
23	" 120 K	R 31	4410502	1
22	" 470 K	R 22	4410577	1
21				
20	" 180 1/2W	R 27	4420170	1
19	" 22 2W	R 29	4440020	1
18	" 47 2W	R 30	4440053	1
17	RESISTOR 100 2W	R 26	4440079	1
16	TRANSISTOR 2N4037	Q 5	3630191	1
15	" 2N2924	Q1,2,6	3630027	3
14	TRANSISTOR 2N5293	Q 3,4	3630316	2
13	LABEL, LOGIC CARD	10A1069-1	3430485	1
12	I.C. SN 74LS123	U 3	3660768	1
11	" SN 75452	U 5	3660925	1
10	" LM 340T-12	U 4	3650074	1
9	" UA 7805 UC	U 2	3650173	1
8	I.C. LM 339 N	U 1	3730207	1
7				
6	I.C. SOCKET AMP 640463-1	U5	3250016	1
5	" " " 640357-1	U 1	3250024	1
4	I.C. SOCKET AMP 640358-1	U 3	3250032	1
3	CONN. AMP 207081-1	J 1	3050234	1
2	CONN. BERG 65001-081	P 1	3110442	1
1	P.C. BOARD 5IC5907	REV. -11,-21	3472271	1

REVISIONS		DATE	MGMT. APPR.
B	R6 WAS 33 Ω, R35 WAS 2500 Ω, ADDED R35 & 36 TO P/L, ECO 1191 R 4-17-80 CR		
A	RELEASE TO PROD. T/W 19 SEPT 80 ECO 1135		

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA 93017

COMPONENT LAYOUT
CPU INTERFACE ASSY.

TOL: FRACT. ± 1/32. .XX ± .030. .XXX ± .010. ∠ ± 1/2°

DWN	BWF	24 MAR 80	SCALE: 2X1
CHK	[illegible]	4-3-80	20C2781 . B
ENG	CARL	22 MAR 80	

MEMORY BOARD 8 X 4

Schematic 91D7135
Component Layout 20B2712
PC Board 51B5850

I. PURPOSE

This memory board contains additional memory for program and data storage. Up to 8 kilobytes of erasable programmable read only memory (EPROM) may be installed for program storage. Data is both written and read into random access memory (RAM). This board has provisions for four kilobytes of RAM.

II. TECHNICAL DESCRIPTION

Address ranges for both PROM and EPROM are selected independently using slide switches of DIP switch S1, allowing multiple memory boards to be used in special applications. Slide switches 1 and 2 are used to assign EPROM addresses, which occur in 8kbyte blocks from 8000 to FFFF hex. The output of IC U12, Pin 6 is used as an enable strobe for the EPROM chip select decoder (IC U13), allowing the proper memory IC to be selected. Slide switches 3 and 4 are used in assigning RAM addresses which are in 4kbyte blocks ranging from ØØØØ to 3FFF hex. Pin 8 of IC U12 is used as a RAM access enable strobe for the half of IC U13 used to select the proper RAM IC.

Each TMS2716 EPROM is 8 bits by 2048 words; however, the

TMS4045 RAM is only 4 bits wide by 1024 words. Two RAM IC's are enabled at the same time to allow storage and retrieval of 8-bit data words.

Slide switch 5 disables the address buffers when EPROM is selected. Normally, this switch is closed so EPROM can be read. In applications which require additional memory cards with RAM only, this switch would be opened on the cards without EPROM. Slide switch 6 disables EPROM when RAM is accessed. Its operation is similar to the operation of slide switch 5.

III. TROUBLESHOOTING

A. Make sure the slide switches are in proper position. In a standard Remote or Control Terminal, all memory board slide switches should be in the ON position.

B. Verify proper +12, -5, +5 volt supply voltages are present. It is best to measure these voltages at the actual memory IC pins.

C. Check EPROM ENABLE signal (IC U12, Pin 6) by observing waveform. EPROM should be enabled frequently when the system is operating properly. If no toggling is observed, check the address select circuitry (IC U11 and U12).

D. Check the RAM ENABLE signal (IC U12, Pin 8) by observing waveform. It should frequently toggle if address selection circuitry is operating properly.

E. Verify that the SN74LS244 bus drivers are enabled, allowing data to be read and written from the data bus.

FIRST USED ON: MRC-1

Rev.	Revision	Date
DØ	PER ECO 1551	LDH 22 JAN 80
CØ	U10 WAS 74LS260. ECO 1526	8 JAN 80 D.T.W.
B	ADDED TRACE A15 ECO 1194	28 JUN 79 JAM
A	RELEASED FOR PRODUCTION	21 FEB 79 A.J.B.
REVISIONS		DATE

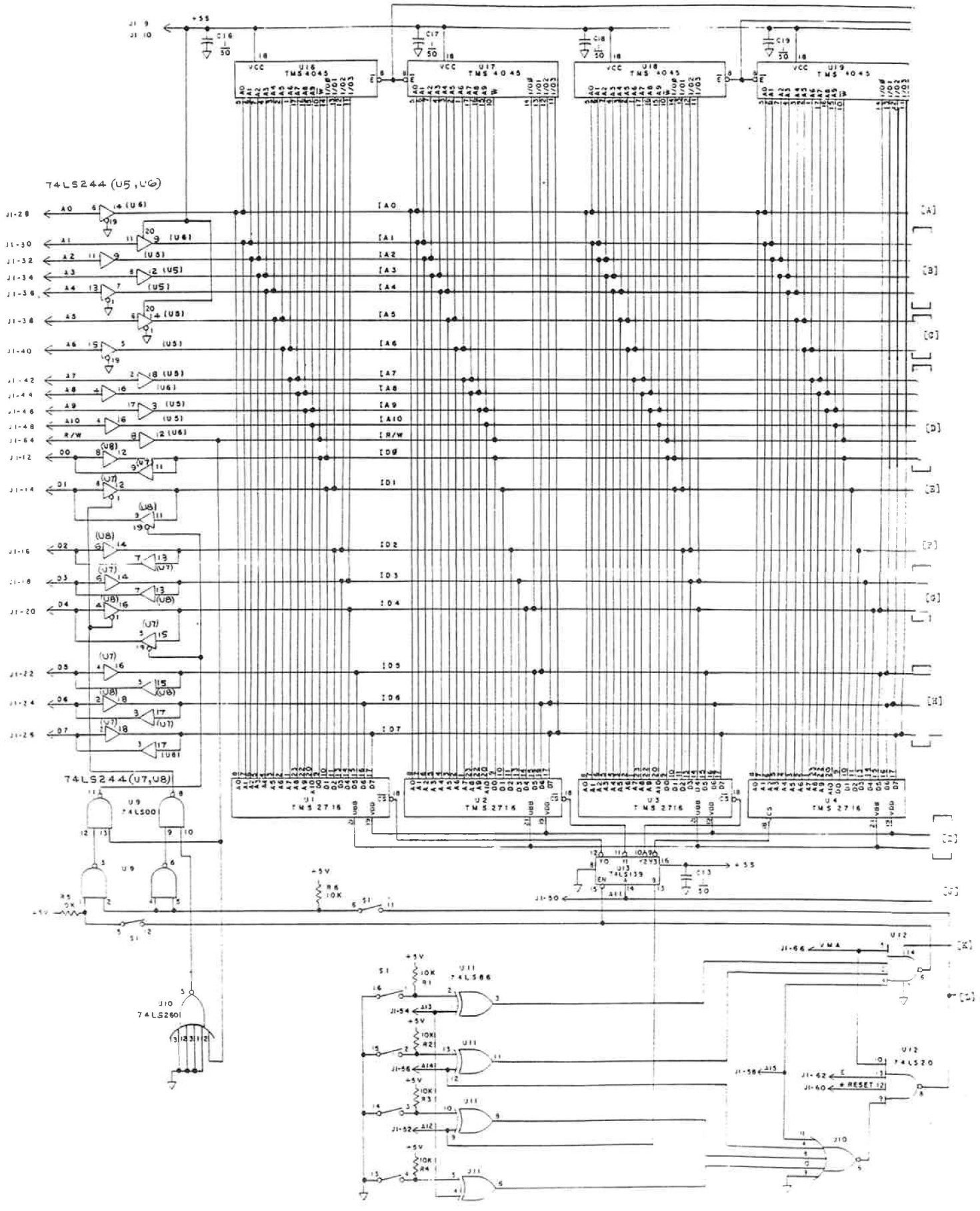
MGMT. APPR.

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA 93017

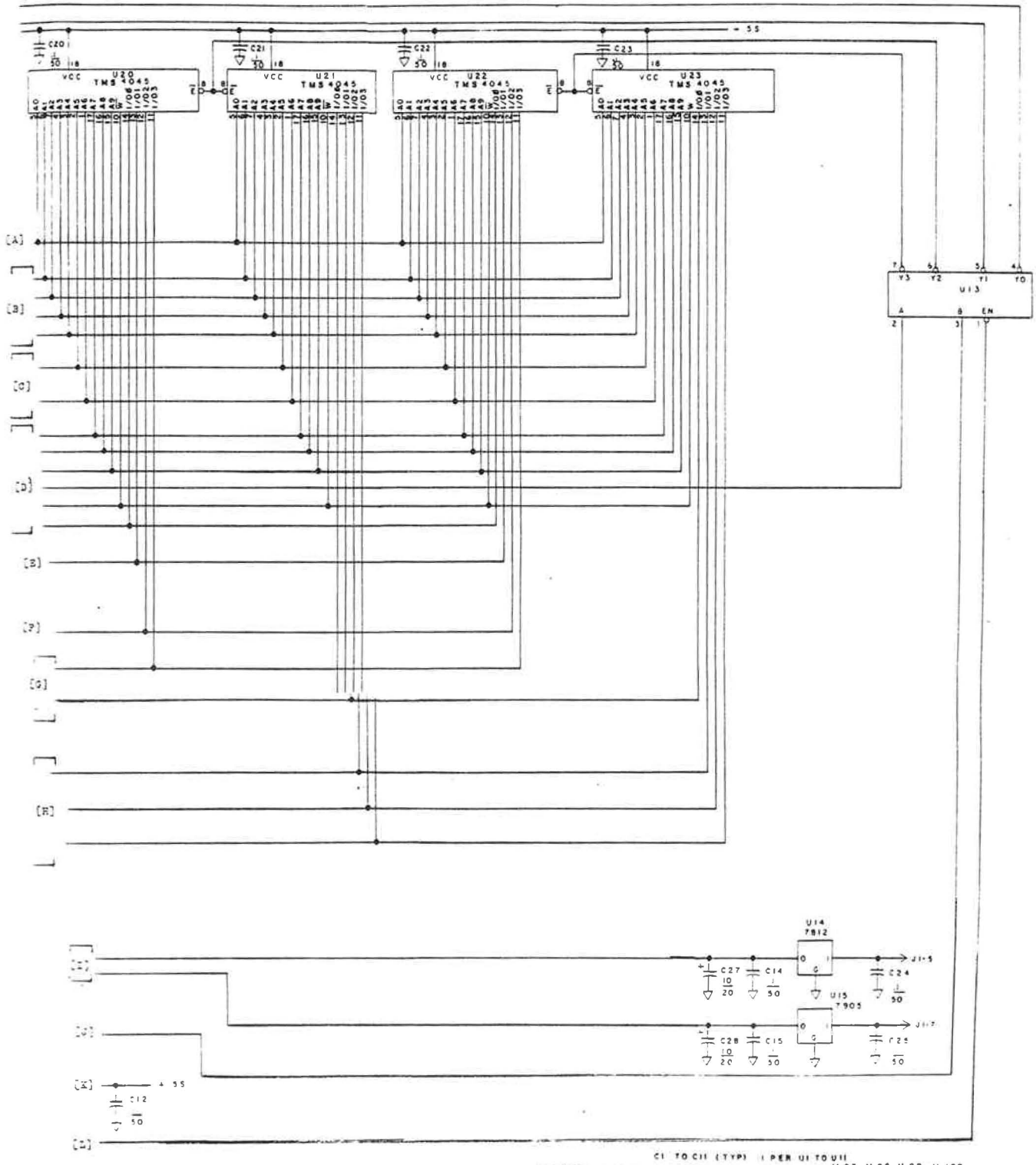
SCHEMATIC
P.C. ASSEMBLY — MEMORY BOARD 8x4

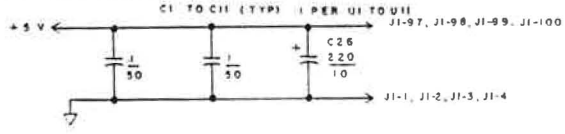
TOL: FRACT. ± 1/32, .XX ± .030, .XXX ± .010, ∠ ± 1/2°

DWN	L.I.	20 NOV 78	SCALE: NONE	
CHK	FXY	20 FEB 79	91D7135	DØ
ENG	MATT	21 FEB 79		



Continued on next page





NOTES

1. U1 – U4 EPROM MEMORY INSTALLED AS REQUIRED FOR SPECIFIC APPLICATION. PART NUMBERS OF EPROM AND LOCATION SPECIFIED ELSEWHERE.
2. U16 – U23 INSTALLED AS REQUIRED.
3. UNLESS OTHERWISE SPECIFIED: RESISTOR VALUES ARE IN OHMS, 1/4 W, 10%; CAPACITOR VALUES ARE IN MICROFARADS.
4. P.C. BOARD 91C5850.
5. COMPONENT LAYOUT 20D2710.

FIRST USED ON MRC-1

REVISIONS					DATE	APPD
D	PER ECO 1551 LOH 22 JAN 80					
C						
B						
A	RELEASED FOR PRODUCTION					

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA 93117

SCHEMATIC
P.C. ASSEMBLY – MEMORY BOARD 8K-4

TOLERANCES: X = 1/16, XX = .030, XXX = .010, ∠ = 1/2°			
DWN	L.T.	20NOV78	SCALE: NONE
CHK	F.X.T.	20FEB79	91D7135 D0
ENG	MATT	21FEB79	

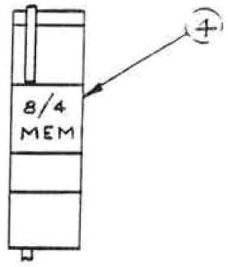
NOTES :

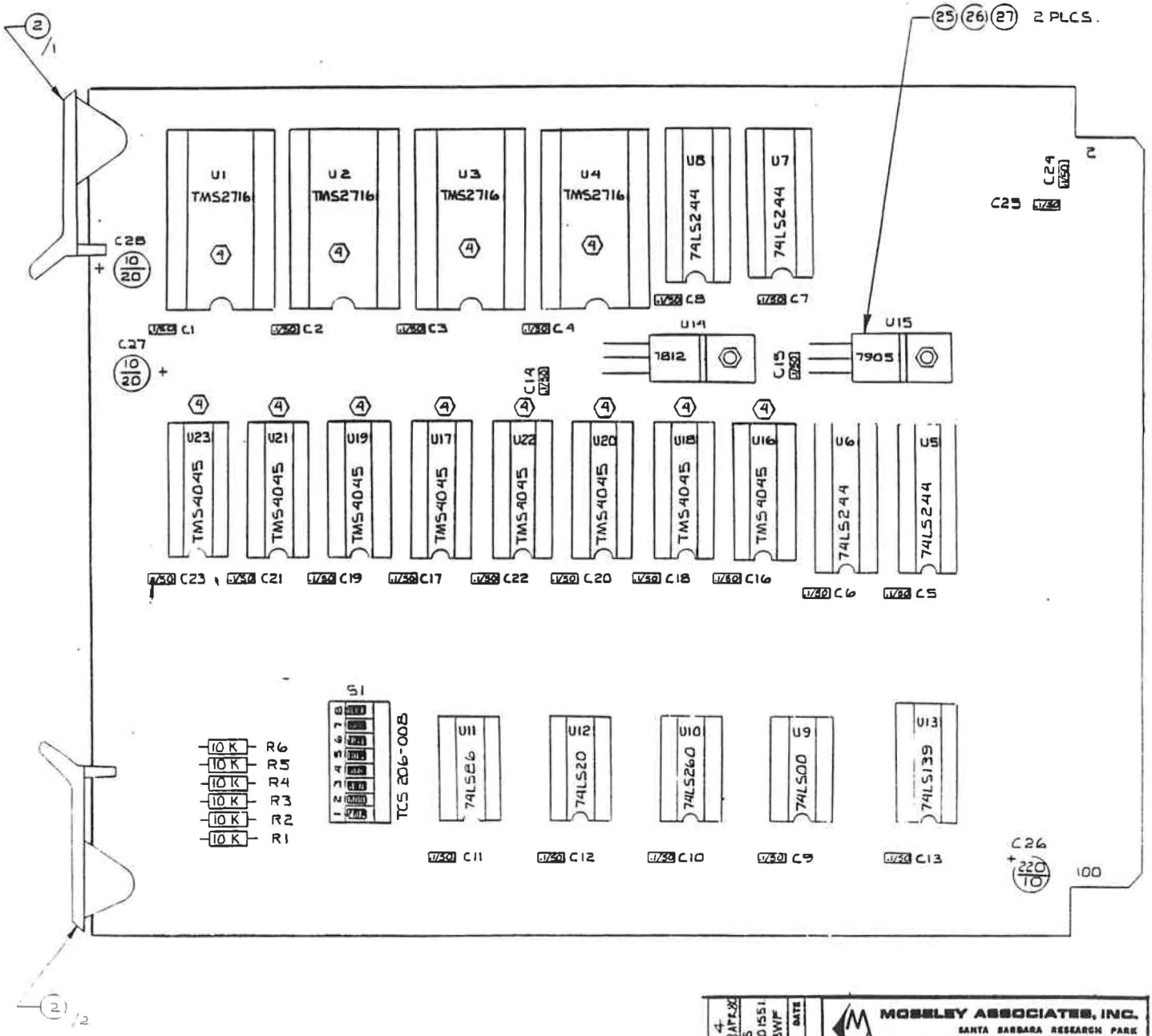
1. UNLESS OTHERWISE SPECIFIED
   RESISTOR VALUES ARE IN OHMS, 1/4 W, 10%
   CAPACITOR VALUES ARE IN MICROFARDS
2. P.C. BOARD SIC5850-50
3. SCHEMATIC 9107135

(4) CMOS I.C. COMPONENTS IDENTIFIED FOR REFERENCE ONLY.
CMOS I.C.'S TO BE INSTALLED ON A HIGHER ASSEMBLY LEVEL.

5. I.C. SOCKETS TO BE INSTALLED IN EACH I.C. POSITION.
6. DIPSWITCH (S1) INSTALLED WITHOUT SOCKET.
   INSTALL WITH SWITCH NO. 1 ON BOTTOM
   WHEN VIEWING BOARD AS SHOWN.

LEFT SIDE VIEW





D3	ADD ITEM 4 ECO1646 MP628 APR 80		MOSELEY ASSOCIATES, INC. SANTA BARBARA RESEARCH PARK GOLETA, CALIFORNIA 93017	
C3	REDRAWN, WAS 2082712. ECO1551 25 FEB 80 BWF		COMPONENT LAYOUT P.C. ASSEMBLY MEMORY 8x4	
	REVISIONS	DATE	TOL: FRACT. ± 1/32, .XX ± .030, .XXX = .015, ∠ = 1/2°	
	MGMT. APPR.		DWN AJB 15 FEB 80 SCALE: 2 X	
			CHK [illegible] 5 MAR 80	
			ENG [illegible] 12 MAR 80 2002712 D3	

ITEM	DESCRIPTION	REF. DES.	STOCK NO.	QTY.
29				
28	I.C. SOCKET 18 PIN	U16-U23 640359-1	3250040	8
27	NUT	4-40 PAN OR BINDER HD.	1050582	2
26	LOCK WASHER	#4 INT. TOOTH	1050624	2
25	SCREW	4-40 X 1/4	1050103	2
24	I.C. SOCKET 14 PIN	U9,U10,U11,U12 640357-1	3250024	4
23	I.C. SOCKET 16 PIN	U13 640358-1	3250032	1
22	I.C. SOCKET 20 PIN	U5,U6,U7,U8 640464-1	3250057	4
21	I.C. SOCKET 24 PIN	U1,U2,U3,U4 640361-1	3250073	4
20	CAPACITOR K220E10	C26 220/10	4280186	1
19	CAPACITOR 196D	C27-28 10/20	4280079	2
18	CAPACITOR CY20C104M	C1-25 .1/50	4310207	25
17				
16	RESISTOR	R1-R6 10K	4410379	6
15				
14	SWITCH, DIP	S1 TCS 206-008	3190089	1
13	I.C.	U14 NC7812T	3650074	1
12	I.C.	U13 SN74LS139	3660800	1
11	I.C.	U9 SN74LS00	3660669	1
10	I.C.	U10 SN74LS260	3660966	1
9	I.C.	U12 SN74LS20	3660719	1
8	I.C.	U11 SN74LS86	3660743	1
7	I.C.	U5-U8 74LS244	3660859	4
6				
5				
4	LABEL		3430295	1
3	I.C.	U15 NC7905T	3650165	1
2	EJECTOR KIT	VARO C12409/1 ½/2	1250075	1
1	P.C. BOARD	5ICS250	3472412	1

REV	DESCRIPTION	DATE
D3	ADD ITEM 4 ECO1696	WPG 28APR80
C3	REDRAWN, WAS 20B2712, ECO1551	BWF 25 FEB 80

REVISIONS | MGMT. APPR.

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA 93017

COMPONENT LAYOUT
P.C. ASSEMBLY MEMORY 8x4

TOL: FRACT. ± 1/32, .XX = ±.03, .XXX = ±.010, ∠ = 1/2°
DWN A.J.B. 15 FEB 80 SCALE: 2 X
CHK 5 MAR 80
ENG 5 MAR 80

20D2712 - D3

CPU BOARD

Schematic 91D7132
Assembly 20B2710
PC Board 51B5849

I. PURPOSE

This module has six (6) functions:

1. CPU and Buffers
2. 2K EPROM and Priority Interrupts
3. I/O Preselect
4. Bit Rate Generator
5. Front-Panel Drive
6. Indicators and Controls for CPU Interface Board

II. ELECTRICAL ADJUSTMENTS

When power is applied to the unit for the first time, R30 should be adjusted. Turn R30 counterclockwise until CR4 (reset) illuminates. Then, turn clockwise until the LED goes off. Continue turning R30 for one more full turn. S1 is used to generate a *PF and *RESET signal, and is used mainly for troubleshooting. A jumper from U9 pin 1 to ground is used to disable the internal RAM on the CPU and is normally installed. A jumper between P1-10 and U1 pin 35 is used to supply power to the internal RAM on the CPU and is not normally installed.

III. THEORY OF OPERATION

Overall: The CPU generates the addresses from which data will be stored or retrieved. The address bus

consists of 16 bits, allowing 65536 (2^{16}) addresses. These lines are used on the CPU to select the PIA (Peripheral Interface Adapter), the EPROM (Erasable Programmable Read Only Memory), and the PIC (Priority Interrupt Controller).

The data bus (D0-D7) is used to carry the data between the CPU and other parts in the system. This bus is bi-directional. When the CPU writes data, the CPU outputs and the peripherals input. Conversely, when the CPU reads data, the CPU inputs and the peripherals output. The direction of data flow is controlled by the R/W (Read or Write) line. Data is read into the CPU when this line is high. The VMA (Valid Memory Address) output of the CPU signals to the address decoding logic that the address line has a valid address on it. No data transfers occur unless this line is high. Output line E (Enable) is a 1 MHz square used for bus timing. Data transfers occur when this line is high. BA (Bus Available) signals that the CPU has gone inactive as a result of a request generated by an external device, such as DMA (Direct Memory Access).

The PIC is used to sequence interrupts to the CPU by allowing higher priority devices to go first. The EPROM is used to store the program (or part of it). The PIA is used to drive the front panel along with six (6) miscellaneous functions. The bit rate generator is used to divide the 1 MHz E signal to approximately 19200 Hz, suitable to run 1200 or 300 baud.

A. CPU and Buffers

Y1 and U1 form a 4.00 MHz crystal oscillator, operating in the parallel resonant mode. C21 and C22 are incorporated to ensure that Y1 does not start oscillating in the third-overtone mode.

U9A disables the internal RAM of the CPU during power up and power down. If the jumper is inserted from pin 1 to ground, the internal RAM will always be disabled. This is the case when a RAM/ROM memory board is used in the system. The NMI input is used for a device requiring very fast service from the CPU. The jumper from P1-10 to U1 pin 35 is used to power the ON CPU RAM; it is not used if a RAM/ROM memory board is used in the system. The HALT input stops the CPU after it is finished executing the present instruction. The CPU then releases itself from the bus and sets the BA (U1, pin 7) output high. This action signifies to the device that pulled HALT low to commence transfer of data on the bus. Address lines A0 through A7 are buffered by tri-state octal buffer U5; likewise, lines A8 through A15 are buffered by U6. The enables for U5 and U6 are controlled by VMA from the CPU. In this way, the address lines to the rest of the system are only active when valid addresses are available. VMA is also gated with the *DMA input by U10A. This allows a DMA controller to simulate VMA to the rest of the system by pulling *DMA low. Data lines D0-D3 are buffered by U7; likewise, D4-D7 are buffered by U8. U10B and U10C are used to enable U7 and U8. One input of U10B and U10C is fed out of phase from the R/W line so only one can be enabled at a time. The other input of U10B and U10C is driven by U17B, which only allows the buffers to be activated if BA is low and if none of the I/O or memory is activated on the CPU board. This is required to prevent both the bus buffers and the PIA or EPROM from trying to feed data to the CPU simultaneously.

B. 2K EPROM and Priority Interrupts

U4 is addressed at locations F800-FFFF which are decoded by U19. Address lines A11-A15 are applied to the inputs of U19 along with VMA and R/W. The R/W is including so that a write operation to

F8000-FFFF will not cause a buss conflict between U4 and the CPU.

The PIC (U3) is addressed at locations FFE0-FFFF which are decoded by U18, U15B and U17A. Address lines A5-A15 are applied to the inputs U18 and U15B along with VMA. During normal operation, address lines A1 through A4 are passed from the A1-A4 inputs of U3 to outputs Z1-Z4 which allows normal addressing of the EPROM. If an interrupt input of U3 is pulled low, it will pull its IRQ output low, generating an interrupt of the CPU. In case of an interrupt, the CPU will fetch the address of the service routine at locations FFF8 and FFF9. These two addresses are decoded by U3, and used to modify its Z1-Z4 outputs in accordance with which interrupt is active, allowing a modified address to reach U4. In this manner, there are eight (8) interrupt service addresses instead of one (1).

C. I/O Preselect

I/O is assigned addresses 8000 through 81FF in this system. Rather than decode all 16 address lines on each I/O board, an I/O preselect system is used. Address lines A9-A15 and VMA are gated together in U16A, U16B and U15A to form *PRE.

This signal goes low when a valid address from 8000 to 81FF is on the address bus. This signal is inverted by U12C to form an active high signal and put on the bus. Most I/O boards conform to the following addressing convention:

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	0	0	0	0	T	T	T	B	B	B	B	R	R

Where: 1 = High
2 = Low
T = Board Type
B = Board Number
R = Register Select

D. Bit Rate Generator

IC's U13 and U14 along with U10D form a synchronous divide by 52 circuit. U14 counts from 3 to 15 providing a division of 13 while U13 divides the output of U14 by 4. In this manner, a 1923Ø Hz square wave is generated at the baud output. This clock is used by ACIAs (Asynchronous Communications Interface Adapters) to provide data at either 1202 baud or 300.5 baud, which is within 0.2 percent of the standard 1200 and 300 baud.

E. Front-Panel Drive

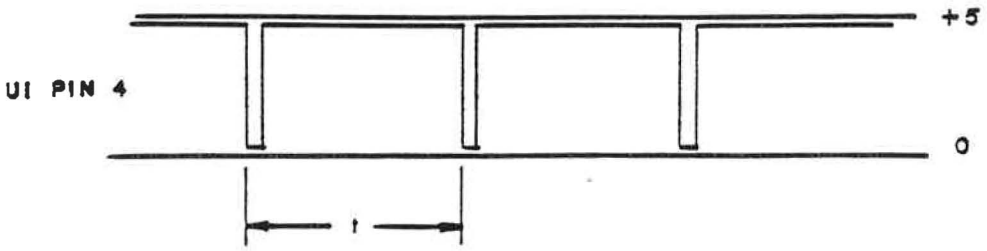
U2 is used to drive the front panel and is located at addresses 8004 through 8007. There are three chip select inputs on the MC6821; 2 active high and 1 active low. The active low input is connected to *PRE which will go active with addresses 8000-81FF. Address lines A6, A7 and A8 are NOR'ed together at U16C and fed to the first active high input. Address line A2 is applied to the second active high input to U2 providing the "04" offset to the base address of 8000. Lines CA1 and CA2 are used as interrupt inputs and allow interrupts every 16.7 ms for 60 Hz or 20 ms for 50 Hz, and also for loss of main power. The interrupt output of U2 is connected on the board to interrupt input 7 of U3. This is the highest priority interrupt. Output lines PA6 and PA7 are applied to the CPU interface card and used for an external maintenance override and failsafe outputs. Output line PB6 and input line PB7 are used for control of the low-battery detector on the CPU interface card. Lines PA0-PA5 are bi-directional and carry data to and from the front panel. Output lines PB0-PB4 are used

to access various elements on the front panel.

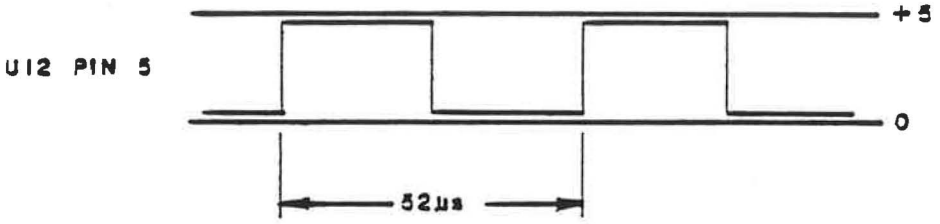
F. Indicators and Controls for CPU Interface Board

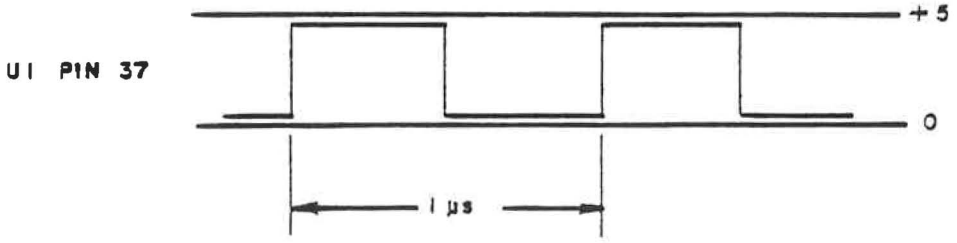
Switch S1 is connected from *PF to ground and is used to simulate a power down/power up sequence. This switch is mainly used for troubleshooting. CR4 indicates activity of the reset line and is used to adjust the power fail threshold potentiometer R30. CR1-CR3 are provided to give a visual indication of operation of the +15, -15 and +5V power sources.

IV. TIMING DIAGRAMS



FOR 50 Hz t = 20 ms
FOR 60 Hz t = 16.7 ms





V. TROUBLESHOOTING

1. CPU and Buffers

A. Verify +5, +12 and -12 volts are present on board.

B. The RESET LED (CR4) should be OFF except when switch S1 is depressed or during initial power up.

C. Verify the ENABLE signal by checking IC U1 pin 37. A 1 MHz square wave should be observed. If this signal is not present, verify proper +5 volt supply voltage is present at pin 8. Pins 1 and 21 should be grounded. If proper IC voltages are present, suspect the crystal or MC6802 IC.

D. If RAM enable jumper is present, IC U1 pin 36 should be low. If no jumper is present, verify pin 36 of IC U1 is high.

E. Verify the following levels on IC U1 (MC6802):

*HALT	Pin 2	=	+5 volts (±.25V)
*NMI	Pin 6	=	+5 volts (±.25V)
BA	Pin 7	=	0 volts (±.25V)
*RESET	Pin 40	=	+5 volts (±.25V)

F. Check IC U1 pin 4 for real time clock interrupt signal (60 Hz pulse). If this signal is absent, check IC U2 pin 40 for the real time clock signal from the CPU interface card.

G. Check for activity on the Read/Write line, pin 34, and valid memory address, pin 5. Both lines should toggle in a non-periodic manner. If this is not observed, the problem may be in the microprocessor IC or another IC connected to these lines.

H. Using an oscilloscope, observe the address and data lines,

pins 9 through 33. These lines are three-state and often appear to float in between HI and LOW. The inputs and outputs of the SN74LS244 should appear similar. The data and address lines may be observed using an extender card and checking the even numbered pins between 12 and 58.

2. 2K EPROM and Priority Interrupt

A. Check IC U4 (TMS2716) for proper supply voltages.

+5V	Pin 24
-5V	Pin 21
GND	Pin 12
+12V	Pin 19

B. Attach an oscilloscope to chip select (pin 18) of IC U4. After pushing the reset push button, two low-going pulses should be seen. If pulses are not present, check IC U19.

C. Check data and address lines for activity.

D. Observe pin 23 of IC U3. It should be normally high with low-going pulses approximately every 20 ms. If these pulses are not present, check IC U3 pin 11 for these pulses.

3. I/O Preselect

A. Check the inputs of IC U16A and IC U16B for activity coincidental with activity on addresses A9 through A14.

B. Check pin 8 or IC U15A for low-going pulses. If no pulses are observed, check input signals on pins 9, 10, 12 and 13.

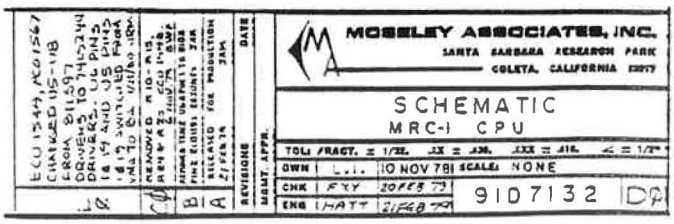
C. Output from the Inverter Buffer (IC U12C) should look similar to IC U15A pin 8, only inverted.

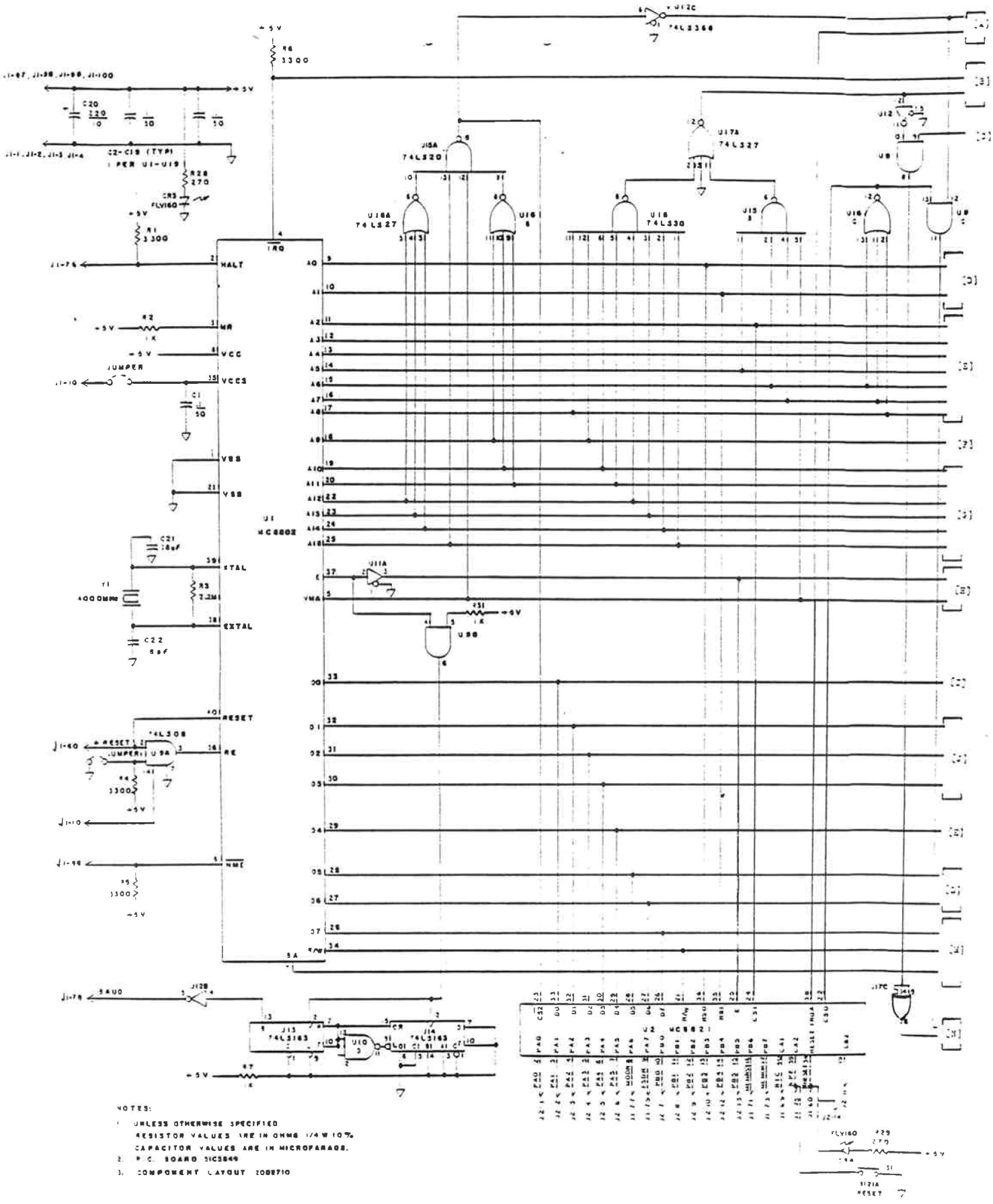
4. Bit Rate Generator

A. Check for the 1 MHz ENABLE signal on pin 2 of IC U13 and IC U14. If signal is not present, trace back to the origin, IC U1 pin 37.

B. Check each pin of IC U13 and IC U14, which is pulled high by R7 to verify a "HIGH" very near +5 volts.

C. Pin 15 of IC U14 should have a 1 µs pulse every 13 µsec. IC U13 pin 13 should have a 52 µsec square wave.

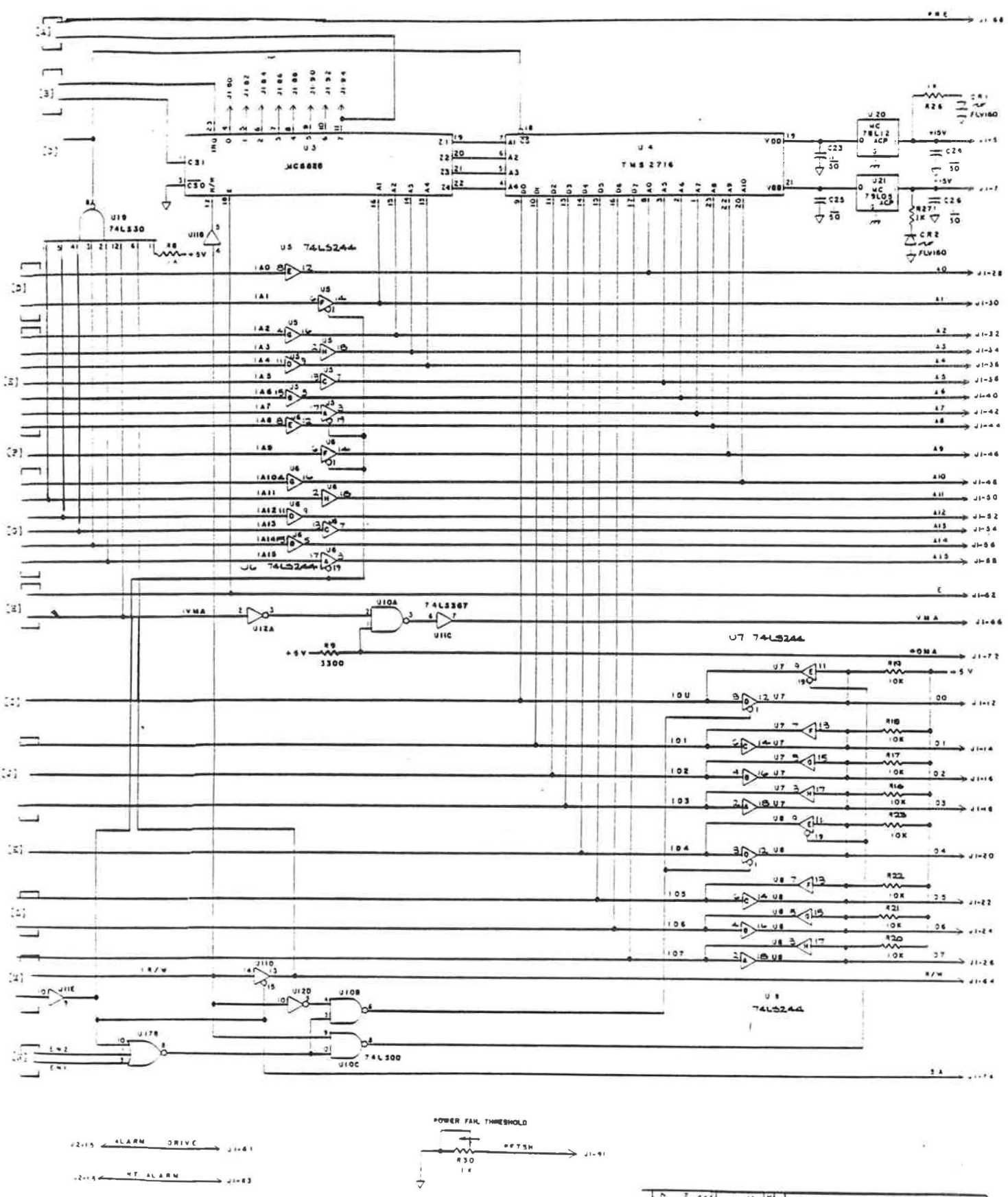

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA
SCHEMATIC
MRC-1 CPU
10 NOV 78
NONE
9107132



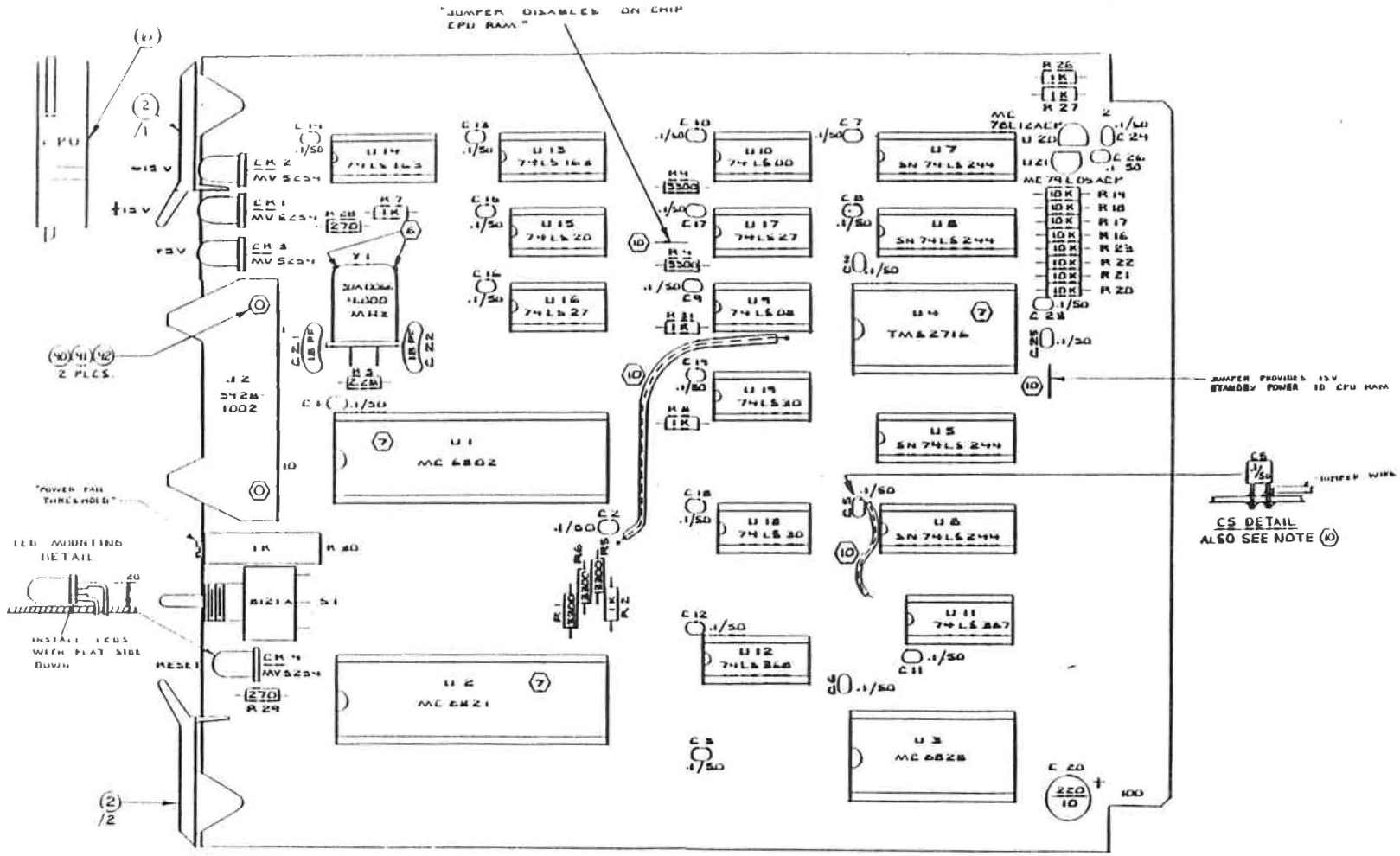
NOTES:

1. UNLESS OTHERWISE SPECIFIED RESISTOR VALUES ARE IN OHMS 1/4 W 10% CAPACITOR VALUES ARE IN MICROFARADS.
2. P.C. BOARD SIC5849
3. COMPONENT LAYOUT 2088710

Continued on next page



MOSLEY ASSOCIATES, INC.			
SCHEMATIC			
MRC-1 CPU			
DWN	L...	10 NOV 78	SCALE NONE
CHK	F.Y.Y.	10 NOV 78	9107132
ENG	TIMOTHY	10 NOV 78	



NOTES:

1. UNLESS OTHERWISE SPECIFIED RESISTOR VALUES ARE IN OHMS, 1/4 W, 10 %. CAPACITOR VALUES ARE IN MICROFARADS.
4. P.C. BOARD 5-C 8849-11-21
5. SCHEMATIC 710 7132 REV DØ
6. ALL TRANSISTORS SOLDERED WITHOUT SOCKETS
7. ALL IC'S ARE MOUNTED IN SOCKETS
(6) TACK SOLDER Y1 TO PAD 2 PLCS.
(7) IC SHOWN FOR REFERENCE ONLY TO BE SPECIFIED AND INSTALLED AT ANOTHER ASSEMBLY LEVEL.

(10) ALL JUMPERS ARE #30 AWG, SINGLE STRAND INSULATED WIRE-WRAP WIRE, ADD JUMPERS AS SHOWN.

AT LOCATION C5: WRAP AND SOLDER JUMPER WIRE AROUND LEAD OF CAPACITOR. INSERT LEADS OF CAPACITOR INTO BOARD AND SOLDER.

MOSELEY ASSOCIATES, INC.
SANTA BARBARA AIRPORT
GOLETA, CALIFORNIA

COMPONENT LAYOUT
P.C. ASSEMBLY CPU

200 2710 H7

ITEM NO.	DESCRIPTION	REF DESIG.	STOCK NO.	QTY
42	HEX NUT 3-48		1030055	2
41	LOCKWASHER, SPLIT RING #3		1030089	2
40	R.H. SCREW 3-48 X 3/8		1030030	2
39				
38	SOCKET I.C. AMP 640357-1	U1,2	3250099	2
37	" " 640361-1	U3,4	3250073	2
36	" " 640446-1	U5-8	3250057	4
35	" " 640358-1	U11-14	3250032	4
34	SOCKET I.C. AMP 640357-1	U9,10,15-19	3250024	7
33	TRANSISTOR 2N 74 ACP	U21	3650132	1
32	TRANSISTOR 2N 74 ACP	U20	3650124	1
31	I.C. MC 6828P	U3	3770035	1
30				
29				
28				
27	I.C. SN 74 LS 244	U5-8	3660859	4
26	" SN 74 LS 368	U12	3660875	1
25	" SN 74 LS 367	U11	3660867	1
24	" SN 74 LS 163	U13,14	3660826	2
23	" SN 74 LS 30	U18,19	3660735	2
22	" SN 74 LS 27	U17,16	3660727	2
21	" SN 74 LS 20	U15	3660719	1
20	" SN 74 LS 08	U9	3660693	1
19	I.C. SN 74 LS 00	U10	3660669	1
18	L.E.D. MV 5253	CR1-4	3390150	4
17	POT 1K	R30	4630075	1
16	RESISTOR 2.2 M	R3	4410619	1
15	" 10 K	R16-25	4410309	8
14	" 3300	R1,2,3,9,4	4410304	5
13	RESISTOR 1 K	R7,8,31	4410247	6
12				
11				
10	RESISTOR 270	R28,29	4410171	2
9	CAPACITOR .1/50	C3-19 C23-26	4310207	23
8	" 18 PF	C21,22	4210084	2
7	CAPACITOR 220/10	C20	4330186	1
6	LABEL	10A1068-1	3430237	1
5	CRYSTAL 30A 0066	Y1	3340163	1
4	CONNECTOR EDGE TECH 3429-1002	J2	3130305	1
3	SWITCH 8121 A	S1	3170065	1
2	EJECTOR 75X9 [illegible]		3500075	1
1	P.C. BOARD	51C5849-11-21	3471827	1

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA

COMPONENT LAYOUT
P.C. ASSEMBLY CPU

200 2710 H6

CPU INTERFACE

Schematic 91C7215
Assembly 20C2781
P.C. Board 51C5907

I. PURPOSE

This module has eight functions:

1. Power failure sensing.
2. Power-on reset.
3. 50-Hz or 60-Hz real time clock.
4. Battery Backup Switching and Charging.
5. Low Battery Voltage Sensing.
6. Output Relays for Failsafe and Maintenance Override Indication.
7. Connection for Audible Alarm Muting.
8. Auto-restart in the event of malfunction.

II. SPECIFICATIONS

1. The maximum battery charging current is 75 mA. This is suitable for up to 7.5 AH Gel-Cell batteries. For a larger battery, use an external charger.
2. For a battery voltage of 6 V, it is float-charged at 6.75 volts. The battery is considered discharged when the battery voltage under load drops below 5.0 volts. The maximum voltage applied to the battery terminals should not exceed 7.0 volts.
3. The voltage and current ratings of the maintenance override and failsafe relays are 24 VDC and 1A. Relay contacts are brought on to the rear panel connector.

4. Aural external drive output

   maximum voltage = 12 V

   maximum current = 25 mA

   maximum current from +5 V output = 25 mA (internal defeat)

   Power user supplied, output is O.C. sink to chassis

III. ELECTRICAL ADJUSTMENTS

1. Battery Charge Voltage (R28): This control is set at the factory for 6.75 V across the binding posts. This is the correct float-charge voltage for the supplied batteries and should not need adjustment.

IV. THEORY OF OPERATION

1. Power Failure Sensing

   AC from the secondary of the power supply transformer is suplied at pins P1-11 and P1-13. The AC is full-wave rectified with CR1 and CR2, then filtered using C1. A potentiometer is connected to P1-91 and ground on the CPU board. R1, R2 and the potentiometer form an adjustable attenuator that is used to compensate for variances in local line voltage and frequency. U1A, along with R4, form a comparator with hysteresis. The threshold is maintained constant with CR3, a 3.1 V Zener diode. When normal line voltage is applied, the positive input of U1A is above the 3.1 V, causing the output to be high. If the AC supply should fail for a period of time (nominally 10 ms), the positive input to the comparator will fall below 3.1 V and cause the output *PF to go low.

2. Power-On Reset

When power is applied to the unit, *PF will go high, allowing C4 to charge through R8. This voltage is applied to the negative input of a comparator consisting of U1B and the 3.1 V reference. After approximately 400 ms, the negative input will reach the reference level causing the output of U1B to go low, which removes the base drive to Q1 allowing the collector to be pulled high by R14. When power is removed from the unit, *PF will go low discharging C4 through R7 and CR4. Operation is much quicker in this direction and reactivates *RESET approximately 3 ms after *PF goes low.

3. Real Time Clock

AC from the power supply transformer secondary is supplied at P1-13 and rectified by CR5. This is applied through voltage divider R15, R16 to the positive input of a voltage comparator (U1C). On the output of the comparator is a rectangular wave having a duty cycle of about 55%.

4. Battery Backup Switching and Charging

Fifteen volts from the power supply is regulated down to 7.45 volts by U2. This is passed through CR10 to the battery terminal. R28 is adjusted such that 6.75 V is applied at the battery terminals with no load. R29 is used to protect U2 in case of a short across the battery terminals. During normal operation, Q3 is biased on through R26 by the +15 V supply; this allows the main 5 V supply to be applied to the 5 V standby bus. When either the +15 V or main 5 V supply fails, the base of Q5 is pulled toward ground by either CR7 or CR8. This forward biases Q4 allowing the battery voltage to be passed to the 5 V

standby bus. The 6 volts at the battery terminals is reduced to an acceptable voltage by the voltage drops of CR9, Q4 and Q5.

5. Low Battery Voltage Sensing

A comparator (U1D) is used as a bistable multivibrator. When main power is not applied, the voltage at the output of U1D will reflect the voltage of the 5 V standby bus. This voltage is dropped 0.6 V by CR6 and fed back to the positive input of U1D to keep the output high. If the voltage at the positive input falls below the reference voltage, the output of U1D will be forced low. This occurs when the 5 V standby bus falls to 3.1 V. This removes the voltage at the positive input which effectively latches the output low. Upon reapplication of main power, C6 filters out any glitches that might alter the state of U1D. If the output of U1D did go low, this will tell the computer that the battery failed during the power outage. To reset the latch, a pulse of at least 10 ms is applied by the CPU to P1-71. This causes Q2 to conduct, removing the reference voltage to the comparator. The voltage divider of R22 and R25 is used to provide at least 0.4 V at the positive input to cause the output to go high when the reference voltage is removed.

6. Maintenance Override and Failsafe Relays

To activate the Failsafe output, P1-79 is set high from the CPU board. U5 ensures that the relay will not close when the *RESET line is in its low state, thus preventing a "glitch" when the unit is plugged in or the reset button is pushed. Each gate of U5 has an open-collector output which can sink the current required to activate

a relay when both inputs to the gate are in their "high" state. Voltage regulator U4 provides +12 V to the other side of the coil. When the relay is activated a closure occurs between pins 3 and 4 of the rear connector.

The Maintenance Override output is almost identical. P1-77 is set high from the CPU board to activate the relay. A closure will then be observed between pins 1 and 2 of the rear connector.

The closure between the Failsafe terminals will be observed when the unit is not in a failsafe condition. The closure across the Maintenance Override terminals will be observed when the unit is in a Maintenance Override condition.

In boards installed at an MRC-1 Control Terminal these relays are never activated and serve no function. The relays are installed, however, to preserve interchangeability with boards installed in remote terminals.

These relays are capable of switching a load of up to 24 VDC at currents of up to 1 ampere. Inductive loads (relay coils, etc.) should have a "clamping" diode wired across them to inhibit negative voltage spikes. External relays should be used when it is desired to switch greater loads (or AC loads).

These relays may also be interfaced with transistor-transistor logic (TTL) digital circuits. The relay contacts should be wired so that one side is referenced to the digital common (ground), and the other relay contact to the digital input. A pull-up resistor may be necessary, and it is advisable to wire a 1 µF capacitor and a 100-ohm

resistor (in series) across the relay output to suppress contact bounce. See FIGURE I.

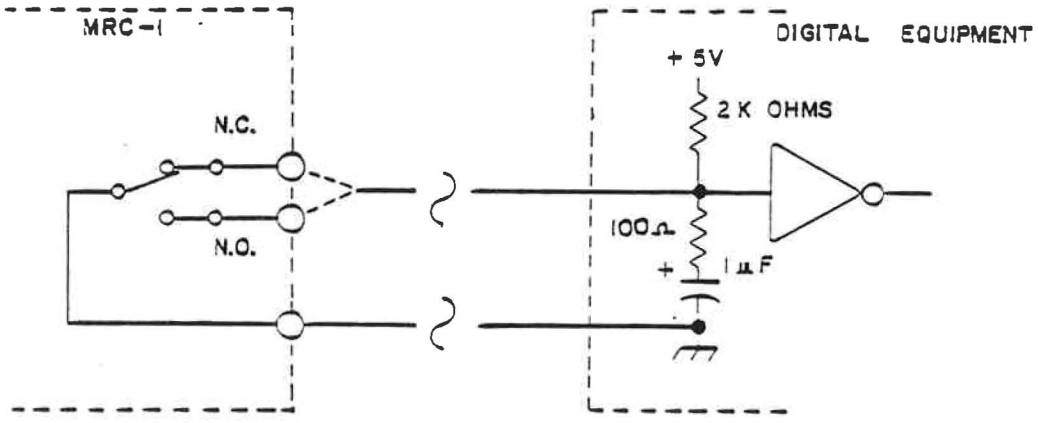


FIGURE I

7. Auto-Restart in the Event of Program Malfunction

Integrated circuit U3 (74LS123) is a dual retriggerable monostable multivibrator ("one-shot"). During normal program operation, line P1-71 is continually strobed from the CPU board. Each pulse reaching pin 1 of U3 "retriggers" the first stage of U3 for another 500 msec. The output at pin 13 will remain high as long as pulses at pin 1 arrive at least every 500 msec. Should these pulses cease (because for any of a number of reasons the program has ceased running properly), the output at pin 13 falls to ground. The falling edge at pin 9 causes a 1-msec pulse at pin 5. If the jumper marked "Auto-Restart" has been installed, transistor Q6 is switched on, causing the *RESET line to fall to ground and re-initiating operation of the program.

The jumper marked "Continuous Restart" enables continuous retries, should the first attempt to restart be unsuccessful. This feature does not appear on some early production units.

VI. TROUBLESHOOTING

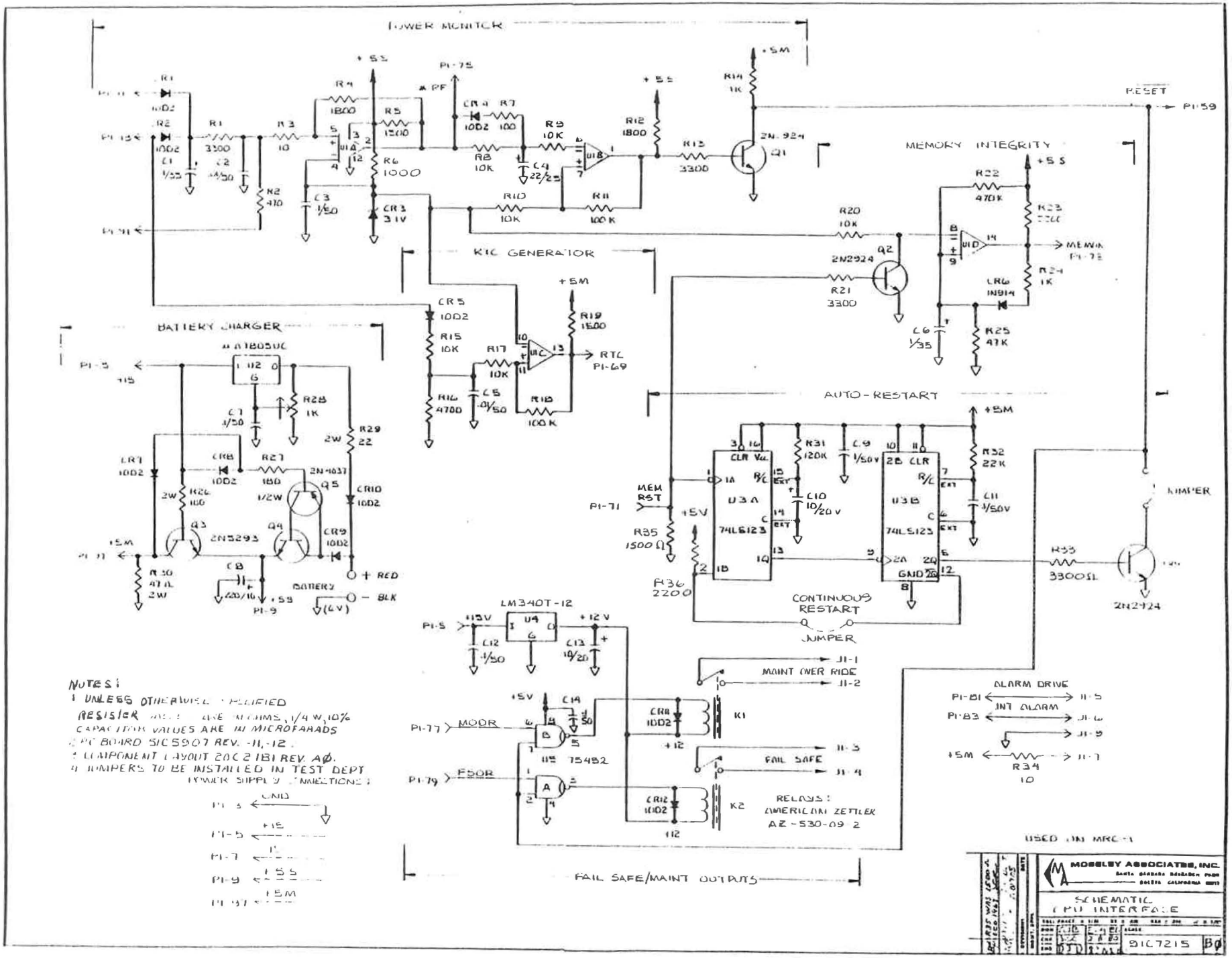
1. Read the section on troubleshooting presented in Section 7.4.

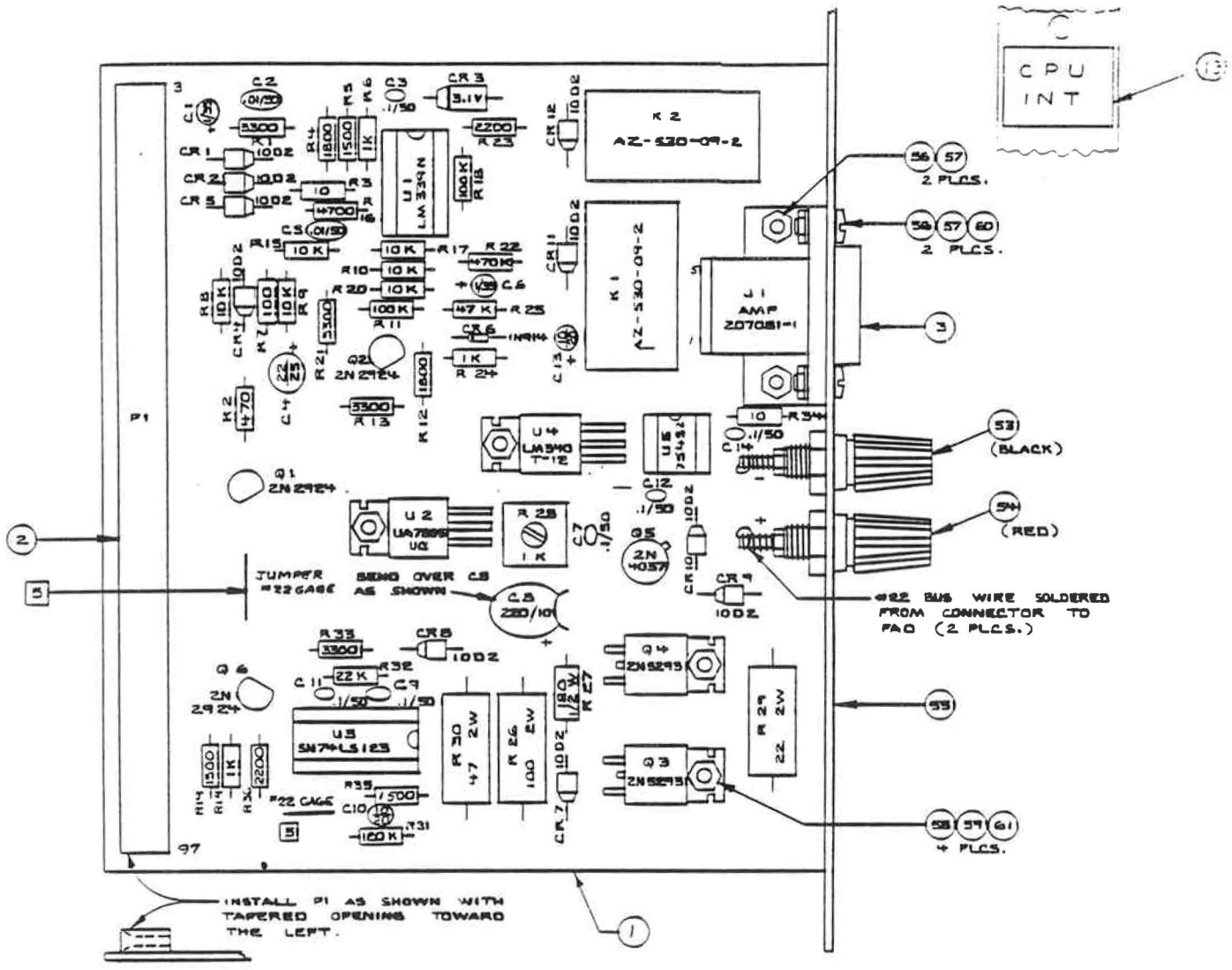
2. Specific areas on this board that must be functional for any operation of the CPU are as follows:
   a. Verify presence of +5 V on the 5 V standby bus. If it is not there, check for short to ground or Q3 open.
   b. Check for waveform at P1-11 and P1-13 (AC in). If not there, check CR1, CR2, C1, and the two 100-ohm resistors mounted on the power supply.
   c. Check voltage at pin 4 of U1. It should be between 3.0 and 3.2 volts. If not, check U1 and CR3.
   d. Check waveform at U1 pin 2 (*PF). If it is low, try readjusting the trim potentiometer on the CPU board (R30). If this does not correct it, check for shorts or replace U1.
   e. If *PF is normal but *RESET is still low, check for at least 4.5 V at pin 6 of U1 and 2.5 to 3.5 V at pin 7. If these are normal, pin 1 of U1 should be less than 0.5 V. If not, suspect U1. If so, the collector of Q1 (P1-59) should be near +5 V. If not, check U3 pin 5, which should be near ground. If not, suspect U3. If U3 pin 5 is indeed near ground, suspect Q1, Q6, or a short ground at P1-59.
   f. Check waveform at U1 pin 13. If it is not correct, suspect CR5 or U1.

3. Circuits that will not stop operation of the CPU are:
   a. Maintenance override and failsafe drivers can be checked with a VOM; most probable cause of failure is U4 or U5.

b. When main power is applied to the unit, U1 pin 14 should be near +5 V. If it is not, try momentarily grounding pin 8. If pin 14 is still low, suspect CR6, C6 or U1.

c. If voltage at the red (+) battery terminal is not 6.75 V ±0.1 V, with the battery disconnected, check the voltage on R29. If should be approximately 7.45 V. If not, suspect U2, or R28.


POWER MONITOR
BATTERY CHARGER
R.T.C. GENERATOR
MEMORY INTEGRITY
AUTO-RESTART
FAIL SAFE/MAINT OUTPUTS
RESET
MEMR
RTC
MEM RST
MAINT OVER RIDE
FAIL SAFE
CONTINUOUS RESTART
JUMPER
ALARM DRIVE
INT ALARM
MODR
FSOR
RELAYS: AMERICAN ZETTLER AZ-530-09 2
BATTERY
+ RED
- BLK
(4V)
LM340T-12
74LS123
2N5293
2N2924
2N3637
NOTES:
1 UNLESS OTHERWISE SPECIFIED
RESISTOR VALUES ARE IN OHMS, 1/4 W, 10%
CAPACITOR VALUES ARE IN MICROFARADS
2 PC BOARD SIC5907 REV. -11,-12.
3 COMPONENT LAYOUT 20C2181 REV. AØ.
4 JUMPERS TO BE INSTALLED IN TEST DEPT
POWER SUPPLY CONNECTIONS:
GND
+15
+5
+5M
USED ON MRC-1
MOSELEY ASSOCIATES, INC.
SCHEMATIC
CPU INTERFACE
91C7215
B0



NOTES :

1. UNLESS OTHERWISE SPECIFIED RESISTOR VALUES ARE IN OHMS, 1/4 W, 10 %. CAPACITORS ARE IN MICROFARADS.
2. P.C. BOARD SIC 5907 REV. -11-21.
3. SCHEMATIC 91C 725 REV. A0

REVISIONS	DATE	MOSELEY ASSOCIATES, INC. SANTA BARBARA RESEARCH PARK GOLETA, CALIFORNIA	
		COMPONENT LAYOUT CPU INTERFACE ASSY.	
		DWN BWE SCALE: 2X/1	
		CHK	
		ENG	20C2781 .180

ITEM NO.	DESCRIPTION	REF. DESIG.	STOCK NO.	QTY.
61	SPLIT RING LOCKWASHER #6		1090590	4
60	SPLIT RING LOCKWASHER #4		1050632	2
59	NUT 6-32 THIN SERIES		1090554	4
58	SCREW B.H. 6-32 X 1/4		1090182	4
57	NUT 4-40 THIN SERIES		1050590	4
56	SCREW B.H. 4-40X5/16		1050145	4
55	PANEL	5A2640	3060374	1
54	BINDING POST EFJ 111-202	RED	3290004	1
53	BINDING POST EFJ 111-203	BLACK	3290003	1
52				
51	RELAY AZ-530-09-2	K1,2	3270113	2
50				
49	DIODE IN 914	CR 6	3600053	1
48	" SZ 3.1 1%	CR 3	3610169	1
47	DIODE 10 D 2	CR1,2,4,5,7-12	3610003	10
46				
45	" 10./20	C 10,13	4280079	2
44	" 220/10	C 8	4280186	1
43	" 22/25	C 4	4280095	1
42	" .1/50	C3,7,9,11,12,14	4310207	6
41	" .01/50	C 2,5	4310132	2
40	CAPACITOR 1/35	C 1,6	4280038	2
39				
38	POT 1K 0.5 W	R 28	4630067	1
37				
36	RESISTOR 470	R 2	4410205	1
35	" 10	R 3,34	4410023	2
34	" 100	R 7	4410122	1
33	" 47K	R 25	4410452	1
32	" 1K	R6,14,24	4410247	3
31	" 1500	R5,19,35	4410262	3
30	" 1800	R 12,4	4410270	2
29	" 2200	R23,36	4410286	2
28	" 3300	R 1,13,21,33	4410304	4
27	" 4700	R 16	4410338	1
26	" 10 K	R8-10,15,17,20	4410379	6
25	" 22K	R 32	4410411	1
24	" 100 K	R 11,18	4410494	2
23	" 120 K	R 31	4410502	1
22	" 470 K	R 22	4410577	1
21				
20	" 180 1/2W	R 27	4420170	1
19	" 22 2W	R 29	4440020	1
18	" 47 2W	R 30	4440053	1
17	RESISTOR 100 2W	R 26	4440079	1
16	TRANSISTOR 2N4037	Q 5	3630191	1
15	" 2N2924	Q 1,2,6	3630027	3
14	TRANSISTOR 2N5293	Q 3,4	3630316	2
13	LABEL, LOGIC CARD	10A1069-1	3-30-55	1
12	I.C. SN 74LS123	U 3	3660762	1
11	" SN 75452	U 5	3660925	1
10	" LM 340T-12	U 4	3650074	1
9	" UA 7805 UC	U 2	3650173	1
8	I.C. LM 339 N	U 1	3730207	1
7				
6	I.C. SOCKET AMP 640463-1	U 5	3250016	1
5	" " " 640357-1	U 1	3250024	1
4	I.C. SOCKET AMP 640358-1	U 3	3250032	1
3	CONN. AMP 207081-1	J 1	3050234	1
2	CONN. BERG 65001-081	P 1	3110442	1
1	P.C. BOARD SIC5907	REV. -11,-21	3472371	1

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA 93017

COMPONENT LAYOUT
CPU INTERFACE ASSY.

SCALE: 2X1

20C2781 B0

MEMORY BOARD 8 X 4

Schematic 91D7135
Component Layout 20B2712
PC Board 51B5850

I. PURPOSE

This memory board contains additional memory for program and data storage. Up to 8 kilobytes of erasable programmable read only memory (EPROM) may be installed for program storage. Data is both written and read into random access memory (RAM). This board has provisions for four kilobytes of RAM.

II. TECHNICAL DESCRIPTION

Address ranges for both PROM and EPROM are selected independently using slide switches of DIP switch S1, allowing multiple memory boards to be used in special applications. Slide switches 1 and 2 are used to assign EPROM addresses, which occur in 8kbyte blocks from 8000 to FFFF hex. The output of IC U12, Pin 6 is used as an enable strobe for the EPROM chip select decoder (IC U13), allowing the proper memory IC to be selected. Slide switches 3 and 4 are used in assigning RAM addresses which are in 4kbyte blocks ranging from ØØØØ to 3FFF hex. Pin 8 of IC U12 is used as a RAM access enable strobe for the half of IC U13 used to select the proper RAM IC.

Each TMS2716 EPROM is 8 bits by 2048 words; however, the

TMS4045 RAM is only 4 bits wide by 1024 words. Two RAM IC's are enabled at the same time to allow storage and retrieval of 8-bit data words.

Slide switch 5 disables the address buffers when EPROM is selected. Normally, this switch is closed so EPROM can be read. In applications which require additional memory cards with RAM only, this switch would be opened on the cards without EPROM. Slide switch 6 disables EPROM when RAM is accessed. Its operation is similar to the operation of slide switch 5.

III. TROUBLESHOOTING

A. Make sure the slide switches are in proper position. In a standard Remote or Control Terminal, all memory board slide switches should be in the ON position.

B. Verify proper +12, -5, +5 volt supply voltages are present. It is best to measure these voltages at the actual memory IC pins.

C. Check EPROM ENABLE signal (IC U12, Pin 6) by observing waveform. EPROM should be enabled frequently when the system is operating properly. If no toggling is observed, check the address select circuitry (IC U11 and U12).

D. Check the RAM ENABLE signal (IC U12, Pin 8) by observing waveform. It should frequently toggle if address selection circuitry is operating properly.

E. Verify that the SN74LS244 bus drivers are enabled, allowing data to be read and written from the data bus.

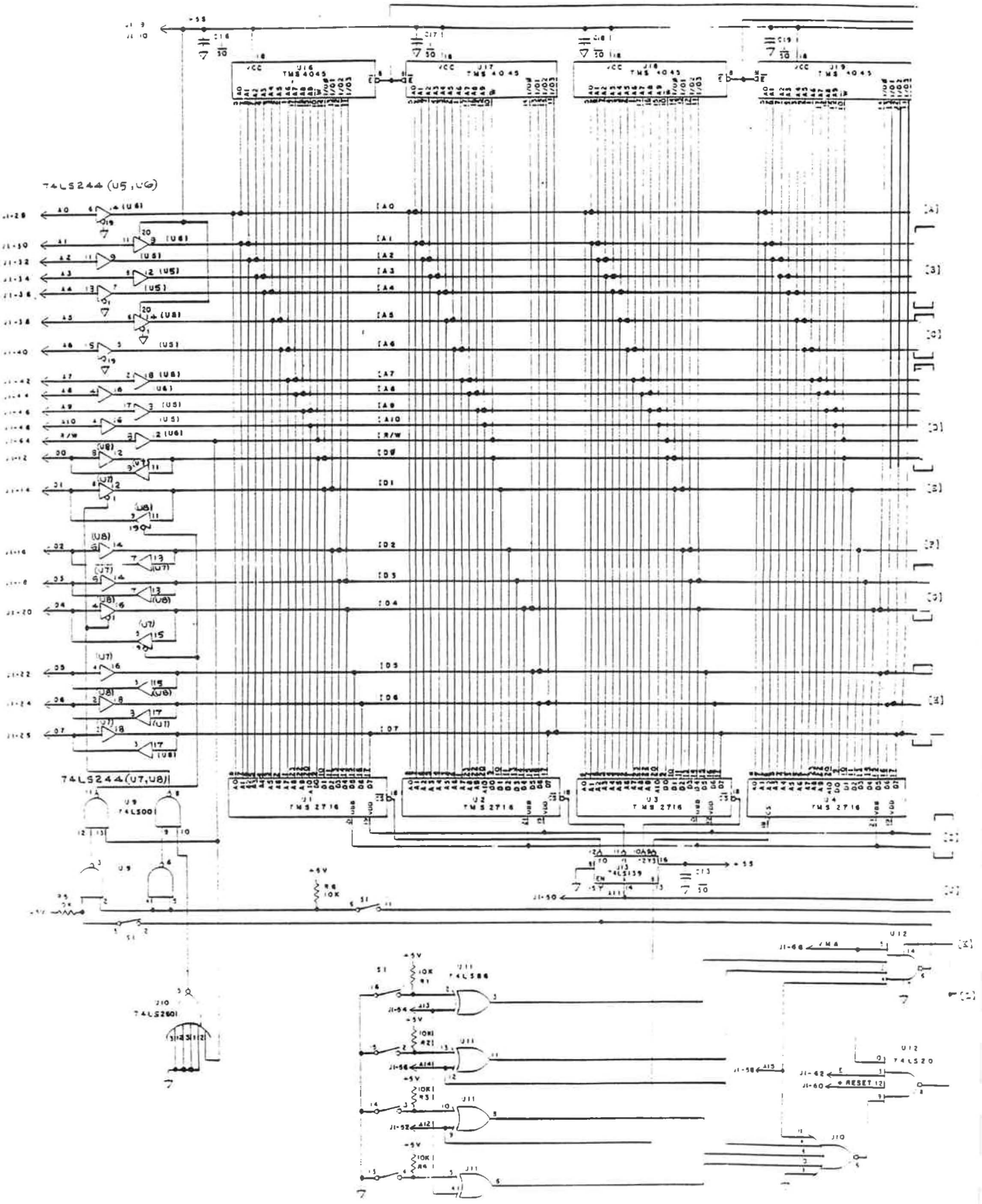
FIRST USED ON: MRC-1

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA 93017

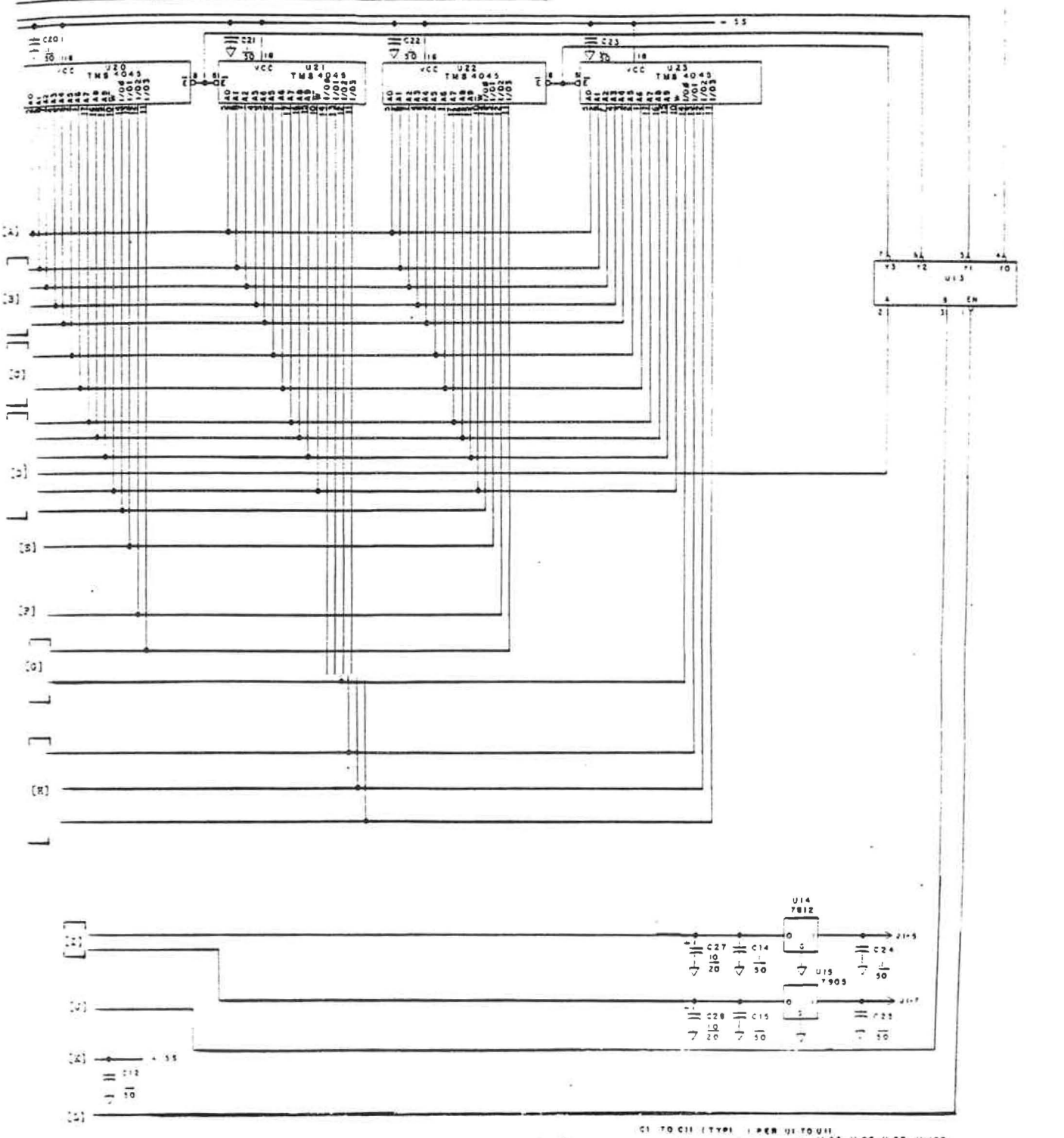
SCHEMATIC
P.C. ASSEMBLY — MEMORY BOARD 8x4

REVISIONS	DATE
DØ PER ECO 1551 LDH	22 JAN 80
CØ U10 WAS 74LS260. ECO 1126	8 JAN 80 DIW
B ADDED TRACE A15 ECO 1184	28 JUN 79 JAM
A RELEASED FOR PRODUCTION	21 FEB 79 AJB

TOL: FRACT. ± 1/32 .XX = ±.03 .XXX = ±.010 ∠ = 1/2°		
DWN L.I.	20 NOV 78	SCALE: NONE
CHK FXY	20 FEB 79	91D7135 DØ
ENG WATT	21 FEB 79	



Continued on next page



NOTES

1. U1 – U4 EPROM MEMORY INSTALLED AS REQUIRED FOR SPECIFIC APPLICATION. PART NUMBERS OF EPROM AND LOCATION SPECIFIED ELSEWHERE.
2. U16 – U23 INSTALLED AS REQUIRED.
3. UNLESS OTHERWISE SPECIFIED RESISTOR VALUES ARE IN OHMS, 1/4 W, 10%. CAPACITOR VALUES ARE IN MICROFARADS.
4. PC BOARD 91C5850
5. COMPONENT LAYOUT 2CD2712

FIRST USED ON: MAC-1

REVISIONS			
DASH	LTR	DESCRIPTION	DATE
D4		PER ECO 1551 DCN 22 JAN 80	
D3			
D2			
D1	B		
D0	A		

MOSELEY ASSOCIATES, INC.
SANTA BARBARA, CALIFORNIA
GOLETA, CALIFORNIA 93117

SCHEMATIC
P.C. ASSEMBLY – MEMORY BOARD 8x4

DRWN	20 NOV 78
ENG	
ENG MGR	
SCALE	NONE

9107135 D0

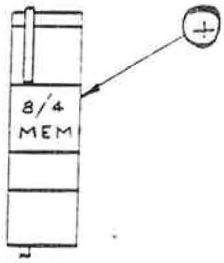
NOTES :

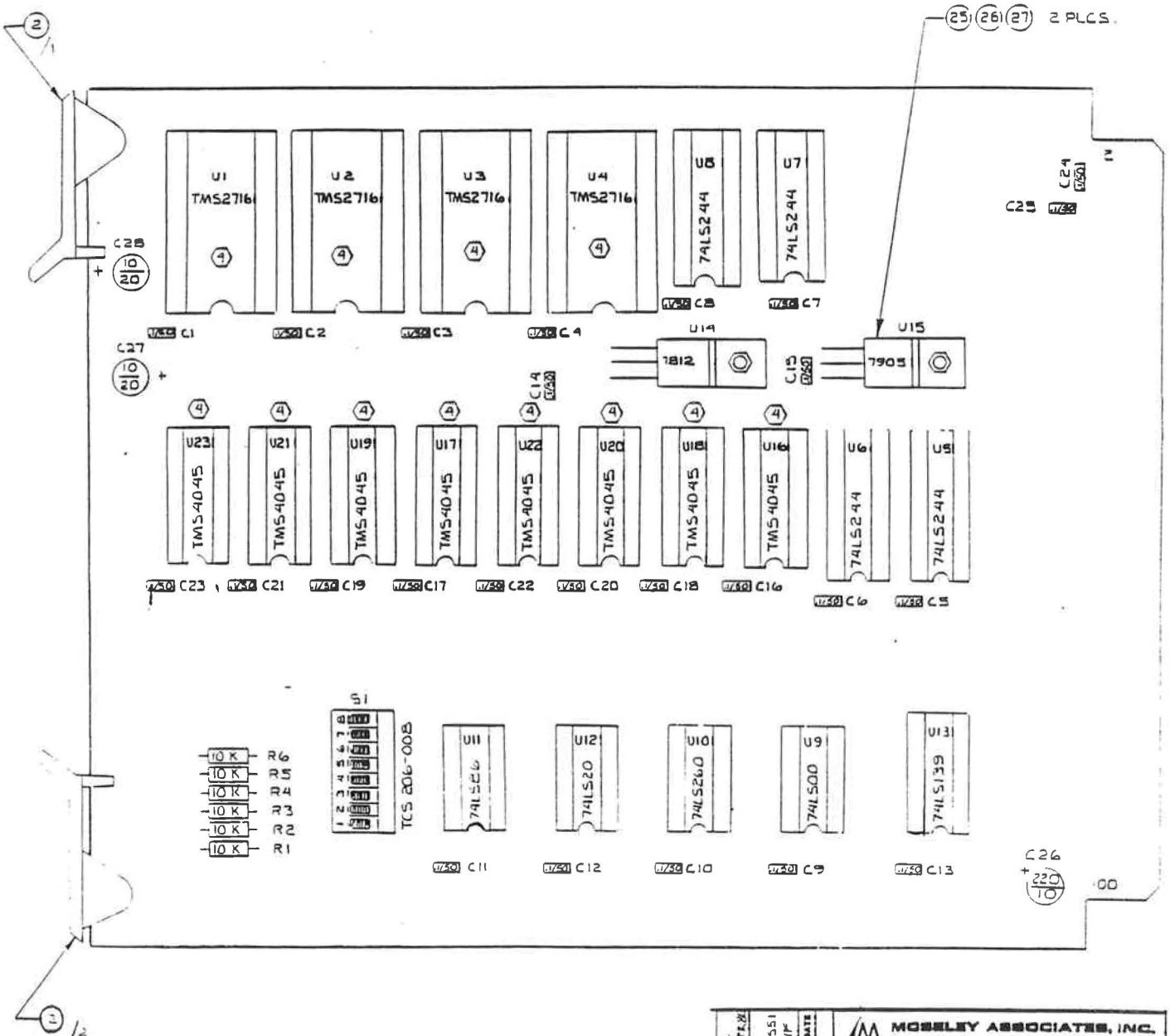
1. UNLESS OTHERWISE SPECIFIED
   RESISTOR VALUES ARE IN OHMS, 1/4 W, 10%
   CAPACITOR VALUES ARE IN MICROFARDS
2. P.C. BOARD SIC5850-50
3. SCHEMATIC 9107135

(4) CMOS I.C. COMPONENTS IDENTIFIED FOR REFERENCE ONLY.
CMOS I.C.'S TO BE INSTALLED ON A HIGHER ASSEMBLY LEVEL.

5. I.C. SOCKETS TO BE INSTALLED IN EACH I.C. POSITION.
6. DIPSWITCH (S1) INSTALLED WITHOUT SOCKET.
   INSTALL WITH SWITCH NO. 1 ON BOTTOM
   WHEN VIEWING BOARD AS SHOWN.

LEFT SIDE VIEW





REVISIONS	DATE	APPR.
ADD ITEM 4	25 FEB 80	BWF
REDRAWN, WAS 208-2712, ECO 1551		

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA 93017

COMPONENT LAYOUT
P.C. ASSEMBLY MEMORY 8x4

TOL: FRACT. ± 1/32. .XX ± .030. .XXX ± .010. ∠ ± 1/2°
DWN: CAB. 5 FEB 80 SCALE: 2 X
CHK: 5 FEB 80
ENG:

208-2712 D3

ITEM	DESCRIPTION	REF. DES.	STOCK NO.	QTY.
29				
28	I.C. SOCKET 18 PIN	U16 - U23 640359-1	3250040	8
27	NUT	4-40 PAN OR BINDER HD.	1050582	2
26	LOCK WASHER	#4 INT. TOOTH	1050624	2
25	SCREW	4-40 X 1/4	1050103	2
24	I.C. SOCKET 14 PIN	U9,U10,U11,U12 640357-1	3250024	4
23	I.C. SOCKET 16 PIN	U13 640358-1	3250032	1
22	I.C. SOCKET 20 PIN	U5,U6,U7,U8 640464-1	3250057	4
21	I.C. SOCKET 24 PIN	U1,U2,U3,U4 640361-1	3250073	4
20	CAPACITOR K220E10	C26 220/10	4280186	1
19	CAPACITOR 1960	C27-28 10/20	4280079	2
18	CAPACITOR CY20C104M	C1-25 .1/50	4310207	25
17				
16	RESISTOR	R1-R6 10K	4410379	6
15				
14	SWITCH, DIP	S1 TCS 206-008	3190089	1
13	I.C.	U14 NC7812T	3650074	1
12	I.C.	U13 SN74LS139	3660800	1
11	I.C.	U9 SN74LS00	3660669	1
10	I.C.	U10 SN74LS260	3660966	1
9	I.C.	U12 SN74LS20	3660719	1
8	I.C.	U11 SN74LS86	3660743	1
7	I.C.	U5-U8 74LS244	3660859	4
6				
5				
4	LABEL		3430295	1
3	I.C.	U15 NC7905T	3650165	1
2	EJECTOR KIT	VARO C12-99/1 & /2	1250075	1
1	P.C. BOARD	S/LS250	3472412	1

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA 93117

COMPONENT LAYOUT
P.C. ASSEMBLY MEMORY 8K

TOL. FRACT. ± 1/32 .XX = .030 .XXX = .010 ∠ = 1/2°
DWN [illegible] SCALE 2 X
CHK [illegible]
ENG [illegible]

200 2712 - D3

ADD ITEM 4
REDRAWN, WAS 200-2712, ECO 0531
25 FEB 80 EWP
REVISIONS

MODEM II BOARD

Schematic 91D7233
PC Board 51C5909
Component Layout 20D2787

I. PURPOSE

The modem (MOdulator/DEModulator) is used to communicate digital information between Remote and Control Terminals via the telephone lines.

II. SPECIFICATIONS

Transmission Format	7-bit ASCII plus even parity in a 10-bit frame. Transmissions are bi-directional and non-simultaneous.
Transmission Speed	1200 baud/300 band switchable
Error Detection	Character parity and longitudinal check-sum on messages
Modulation	Two-frequency continuous phase FSK MARK = 2200 Hz SPACE = 1200 Hz
Interface	600Ω telephone lines, strappable two or four-wire configuration.

III. TECHNICAL DESCRIPTION

The MC6850 Asynchronous Communications Interface Adapter (IC U8) provides the data formatting and control to interface serial asynchronous communications information to the 8-bit data bus. The functional configuration of the ACIA

is programmed automatically during system initialization. A programmable control register provides variable word lengths, clock division ratios, transmit control, receiver control and interrupts. The baud-rate generator (IC U16) provides the clock frequency for the ACIA.

The modem has switch-programmable address specification, allowing multiple modem boards to be used in special applications. BCD switch S3, IC U10 and IC U12 provide address decoding for the board. In normal system operation, with only one modem per unit, switch S3 is left in the "0" position. Two SN74LS244 bus drivers (IC U3 and IC U4) are used to write and read data onto the bus. Parts of IC U6 and IC U7 are used to enable reading and writing according to the status of the read/write line and the board address.

Outgoing serial data is modulated into dual tone frequency shift keying by the XR2206 function generator (IC U15). Serial data input is applied to pin 9. A high input causes a low frequency (Mark) of 1200 Hz to be generated. A low input causes a high frequency (Space) of 2200 Hz to be generated. Resistor R38 is used to reduce harmonic distortion.

Transistor Q3 serves as a switch to turn on the modulator according to the request to send ($\overline{RTS}$) from the ACIA. Switch S2 and parts of IC U11 and IC U13 will turn on the modem continuously for test purposes. The output of the oscillator is AC coupled and fed into a 741 op amp before being transmitted via the telco interface board.

The Deadman Circuit (IC U9) turns off the modulator if communications are disrupted for more than 2.5 seconds.

The incoming FSK signal is fed through a bandpass filter consisting of half of IC U14. The filtered signal is amplified via part of IC U14 and clamped by CR1 and CR2. The clamped signal is then demodulated by the XR2211 (IC U1). The output of the demodulator is buffered by part of U13.

The amplified signal from the third part of IC U13 is peak-detected by CR8, CR7, CR6, and the fourth part of IC U14. This signal is buffered by parts of IC U5 and inverted by transistor Q1 to provide data carrier detect (*DCD).

IV. BASIC MODEM ADJUSTMENT

Normally no adjustment needs be made to the high frequency, low frequency, and VCO controls (R36, R35, and R11). These are painted at the factory with red lacquer to discourage casual adjustment. The procedure for making these adjustments is described in Section V, but it should be stressed that such adjustments under normal circumstances are unnecessary.

Each of the procedures outlined below assumes a one-site system. For multi-site systems, each Remote Terminal must be connected in turn and adjusted.

It is suggested that initial adjustment be made with the units back-to-back on the bench to gain familiarity with the controls prior to installation.

It should be noted that in Section 2, a "Series 3002 (unconditioned) Data Channel per Bell System Technical Reference PUB-41ØØ4" is specified. Therefore, this type of line should be specifically requested from the phone company. (It is guaranteed to have certain characteristics when FSK data signals

are transmitted across it.)

In the following adjustment procedure refer to drawing 15B1117 which is bound in with the next group of blueprints for the location of controls and test points on the modem board.

Step 1: Connect the Control and Remote back-to-back on the bench. For a two-wire system, see Figure 1.1. For a four-wire system, see Figure 1.2. For a mixed telco and subcarrier system, see Figure 1.3. For systems using a subcarrier interconnect in both directions, see Figure 1.4.

NOTE: A simulated telephone line with 30 dB loss may be constructed using a T pad with 560 ohms in each arm and 37 ohms to common.

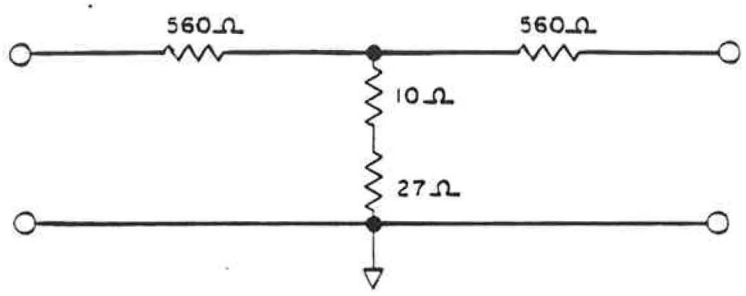


Figure 1.0 - SIMULATED 30 dB PHONE LINE

A Simpson 260 VOM or similar equipment may be used in this adjustment procedure.

Step 2: Apply power to both terminals. Push "ACK" ("acknowledge") at the Remote Terminal keyboard. Disable all active sites at the Control Terminal as follows (see Control Terminal manual Section 4.6.3 for a full explanation of this):

a. Push "SET-UP". The SET-UP LED should come on.
b. Press "SITE ENAB" ("site enable"). The SITE window will

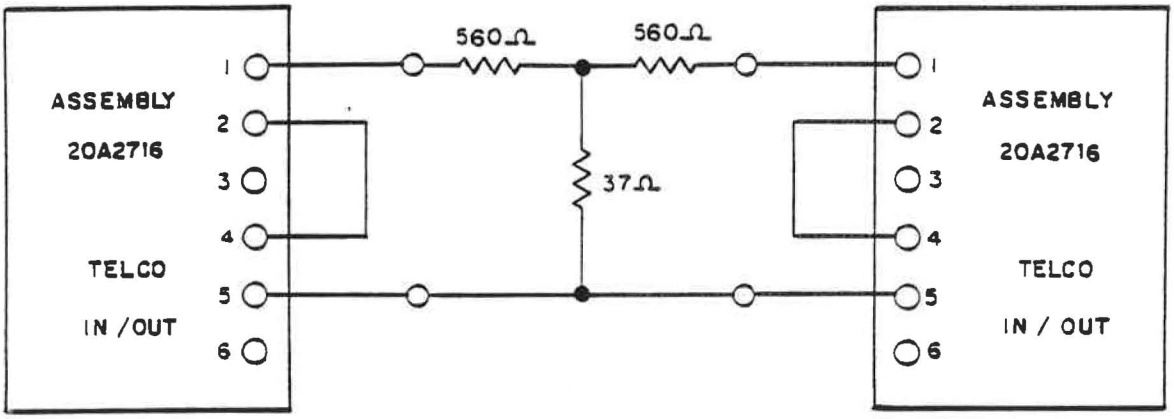


Figure 1.1 - Two-Wire Interconnect

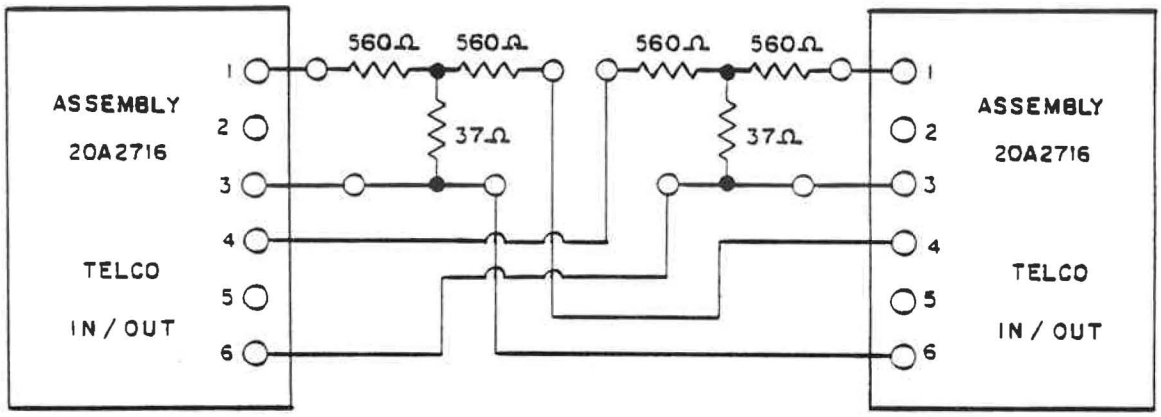


Figure 1.2 - Four-Wire Interconnect

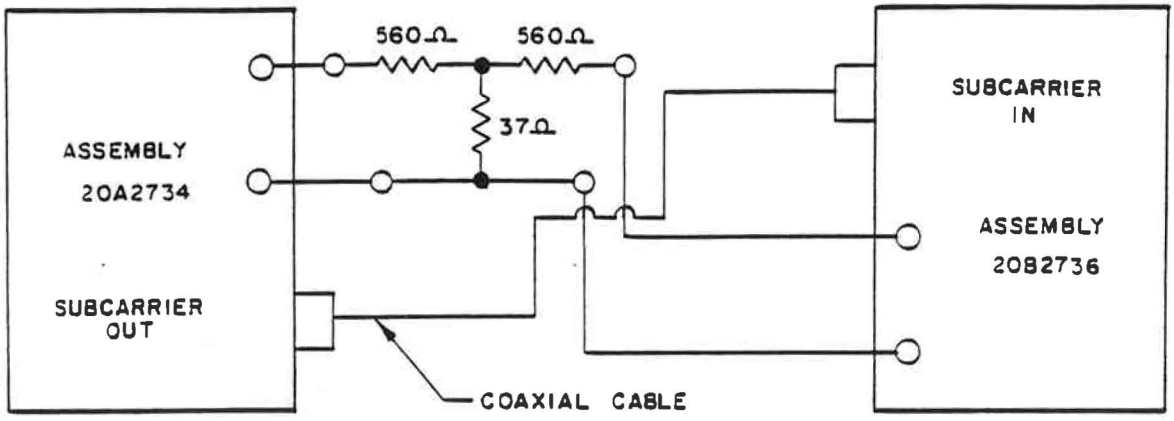


Figure 1.3 - Mixed Subcarrier and Telco

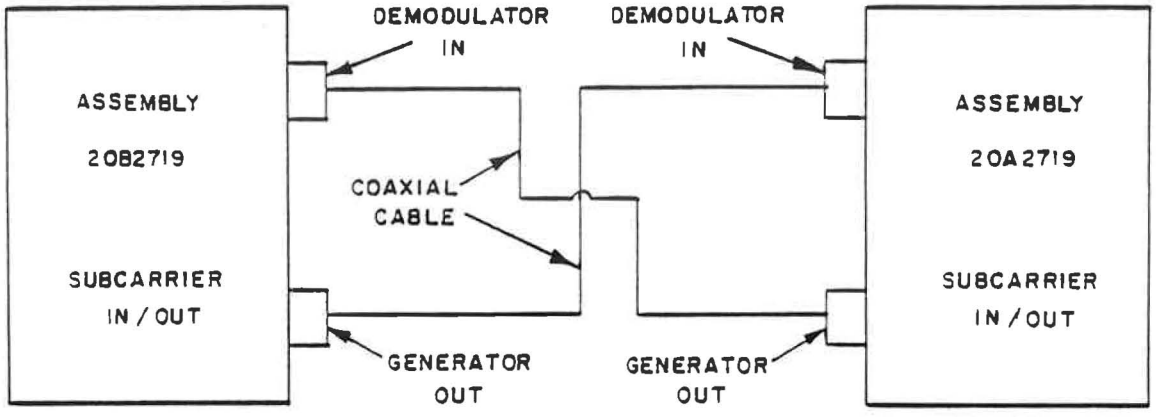


Figure 1.4 - Subcarrier Interconnect

display ".1".

c. If you have a multi-site system, repeat step (b) for each additional site (select site 2, press site enable, etc.).

d. The TRANSMIT LED on the front of the modem card should be off, indicating no sites are enabled.

Step 3: Place the toggle switch on the front of the modem cards (S2) in either TEST position at both terminals. This causes both modulators to generate a continuous tone.

Step 4: Adjust the output levels. Use R10 ("send level adjust") on the front of the modem boards.

Two-wire systems: Measure the output level across terminals 1 and 5. Zero dBm should be observed at both the Control and Remote Terminals.

Four-wire system: Measure the output level across terminals 4 and 6. Zero dBm should be observed at both the Control and Remote Terminals.

Mixed systems: Measure the output level at the Telco Output terminals at the appropriate terminal. Zero dBm should be observed. Using a calibrated oscilloscope, measure the voltage at the Subcarrier Output BNC connector at the other terminal. 1.5 volts peak-to-peak should be observed. The OUTPUT potentiometer above the BNC connector should be adjusted if necessary to meet this requirement. The waveform observed should conform to drawing 15A1114. Adjust R10 ("send level adjust") on the front of the modem board if necessary to meet this requirement. (Note: The COARSE and FINE adjustments above the BNC connector have been set at the factory and should not require further adjustment.)

Subcarrier-In/Subcarrier-Out systems: Measure the output at both terminals at the subcarrier output BNC connector and adjust as described immediately above (under "mixed systems").

Step 5: Put the Control Terminal in OPERATE mode (using S2) and the Remote terminal in the right (TEST) position. Adjust the Control Terminal input level using R12 ("receive level adjust") on the front edge of the Control Terminal's modem board. Measure the input levels across test points 6 and 3. Turn R12 clockwise to increase voltage level.

Two-wire system: Between .5 and .6 volts AC should be observed across the test points. (-30 dBm input)

All other systems: Between .5 and .6 volts AC should be observed across the test points. (-30 dBm input)

Step 6: Put the Remote Terminal in OPERATE mode and the Control terminal in the down (TEST) position (using S2). Adjust the Remote Terminal input level (exactly as was done in step 5 at the Control Terminal).

Step 7: Place both terminals in OPERATE mode. Push the RESET button on the front of the CPU boards at both terminals. Re-enable the Remote Terminal by using the "SITE ENAB" key at the Control Terminal keyboard (Refer to Section 4.6.3 of the Control Terminal manual for a full explanation.) This step is essentially the reverse operation to step 2, above.

Step 8: The Control Terminal and Remote Terminal should now be "talking" successfully. A channel number should appear in the CHANNEL display at the Control Terminal. Pushing the CH ("channel") key at the Control Terminal should cause the channel display at the Control Terminal to advance by one channel.

NOTE: The channel numbers at the Control and Remote Terminals are independent of each other. One channel may be observed at the Control Terminal and a different channel at the Remote Terminal. However, both channel numbers are stored at the

Remote Terminal and for a channel number to appear at the Control Terminal, the number must be fetched from the Remote Terminal - thus indicating a successful communication.

The Control Terminal initiates each communication by sending an interrogation to the Remote Terminal. The Remote Terminal replies with its response. As a result, a regular "heartbeat" can be observed on the Transmit LED at the Control Terminal. If the Remote Terminal does not properly receive a message it does not respond and the unit appears to "skip a beat." In a properly adjusted system, a regular pattern of long and short pulses can be observed on the Transmit LED's.

Two Wire Systems: In a two-wire system, each unit can "hear itself speak" so the Receive LED remains on most of the time. Sometimes a pulsation or flicker can be observed.

Other Systems: The Transmit and Receive LED's will flash alternately at both terminals. If a Receive LED remains steadily the input level on the board is probably too high.

Step 9:

Systems Involving Subcarrier: Upon completion of the back-to-back tests and after connection to the actual interconnecting radio link it may be necessary to adjust the OUTPUT pot on the appropriate interface cards at the rear of the terminals, in order to assure proper modulation of the interconnecting radio circuits.

V. FREQUENCY AND VOC ADJUSTMENTS

High frequency, low frequency, and VCO should not nor-

mally need adjustment. To emphasize this fact, R36, R35, and R11 are painted with red lacquer at the factory after their initial alignment. This section is included in case a need arises to re-align the board, perhaps following a repair accomplished by the user. Refer to drawing 15B1117 which is bound in with the next group of blueprints for the location of controls and test points on the Modem Board.

NOTE: If the frequency counter does not give stable readings the following steps are suggested:

A. Place a 10 KΩ resistor between the frequency counter input and TP1 (white) to increase frequency counter input impedence.

B. Reduce false triggering by placing a capacitor between TP1 (white) and ground.

It is suggested that the terminals be connected back-to-back at the same location (see preceding section) so that both ends are easily accessible.

Step 1: With the terminals not connected to each other, prepare to set the frequencies as follows: Connect frequency counter between TP1 (white) and ground (TP3, black).

Step 2: Set the high frequency. Place S2 in HI position and adjust R56 to obtain a frequency of 2200 Hz.

Step 3: Set the low frequency. Place S2 in LOW position and adjust R53 to obtain a frequency of 1200 Hz.

Step 4: Set S1 to CAL position. Connect frequency counter to TP4 (yellow). Adjust R11 (VCO fine tune) to obtain a

frequency of 1700 Hz at TP4.

Step 5: Return S1 & S2 to OPER position and adjust the input and output levels as described in Section IV above, with the terminals connected.

VI. INSTALLATION AND TROUBLESHOOTING

A. Refer to Section IV for instructions for adjustment of the input and output levels.

If trouble is encountered:

B. Check DIP Switch positions. Normally slide switch 1 is ON and other switches are in the OFF position. Make sure S1 is in the OPERATE position at all terminals.

C. Verify that proper power supply voltages are present.

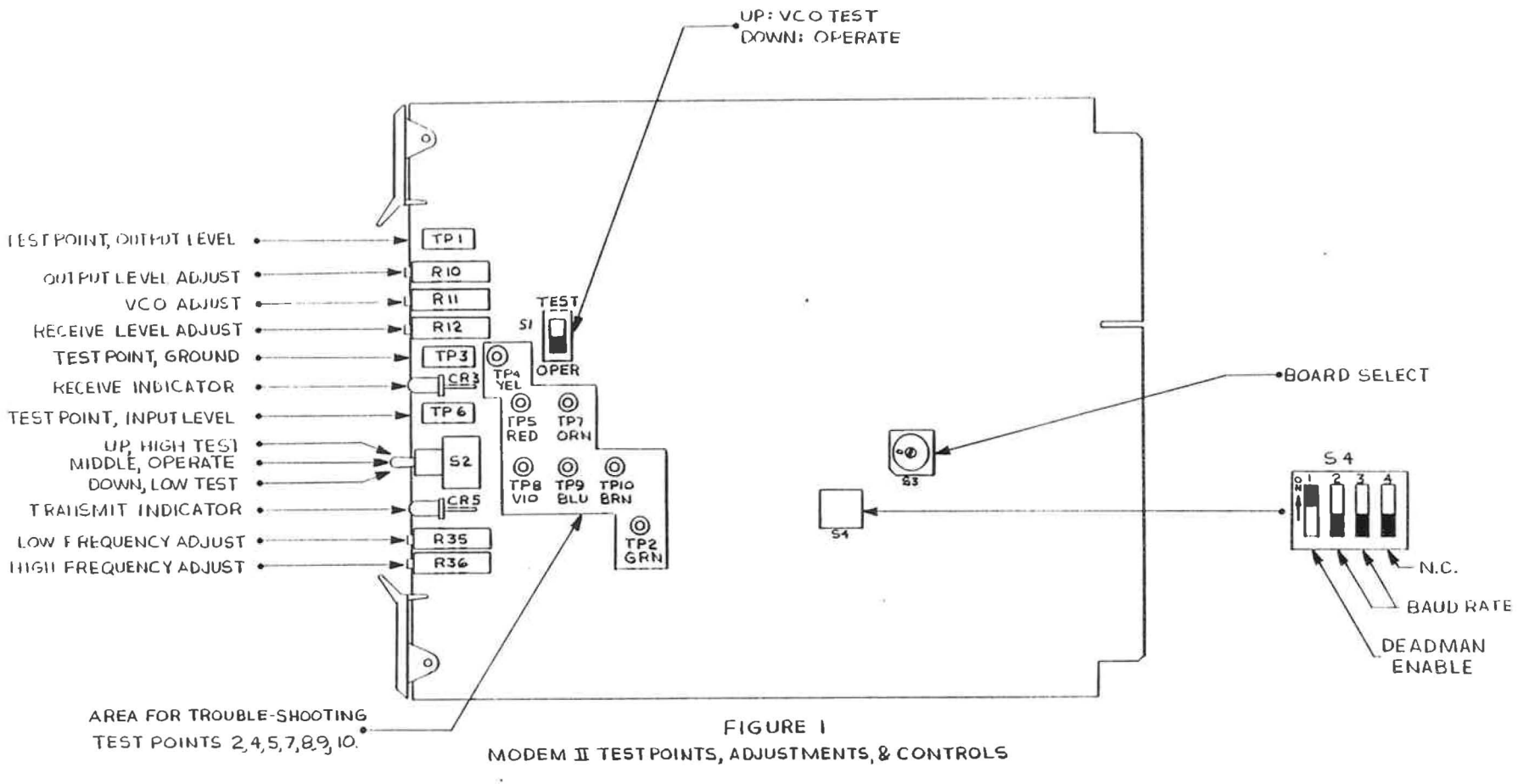


FIGURE 1
MODEM II TEST POINTS, ADJUSTMENTS, & CONTROLS

USED ON: MRC FAMILY

REVISIONS	DATE
MFG'T. APPR.	

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA 93017

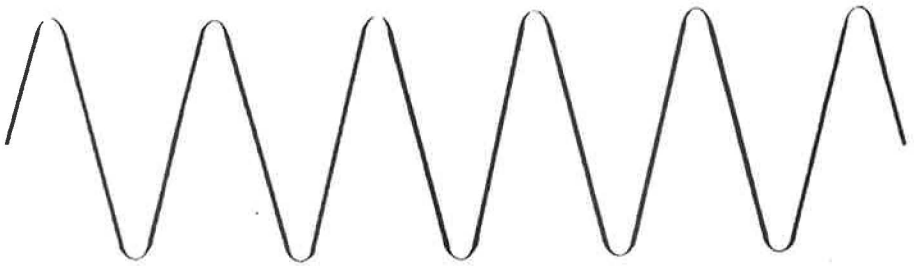
MODEM II
ADJUSTMENTS, ETC.

TOL: FRACT. ± 1/32, .XX ± .030, .XXX ± .010, ∠ ± 1/2°

DWN	CAH	9 MAR 81	SCALE: NONE
CHK	[illegible]	3-12-81	15B1117
ENG	[illegible]	12 Mar 81	

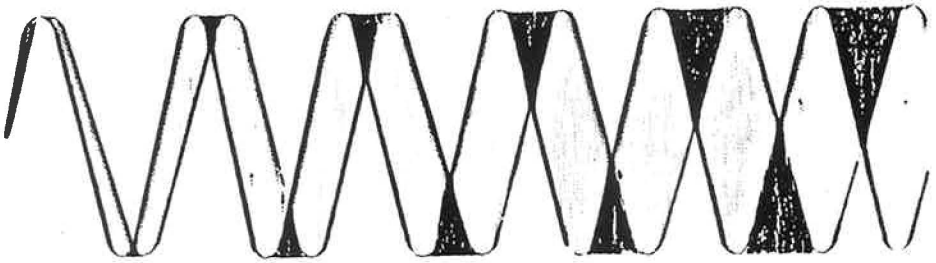
UNMODULATED SUBCARRIER

(A)



SUBCARRIER DEVIATED ± 5% OF CENTER FREQUENCY

(B)



NOTES:

1. USE INTERNALLY - DERIVED POSITIVE - SLOPE TRIGGERED SWEEP.
2. SET SWEEP TIME TO ACHIEVE TRACE "A".
3. SET GENERATOR DEVIATION TO ACHIEVE TRACE "B".

FIRST USED ON: MRC-1

RELEASED 6-7-76

REVISIONS	DATE	MGMT. APPR.

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA 93017

STANDARD SUBCARRIER PATTERN

TOL: FRACT. ± 1/32, .XX ± .030, .XXX ± .010, ∠ ± 1/2°

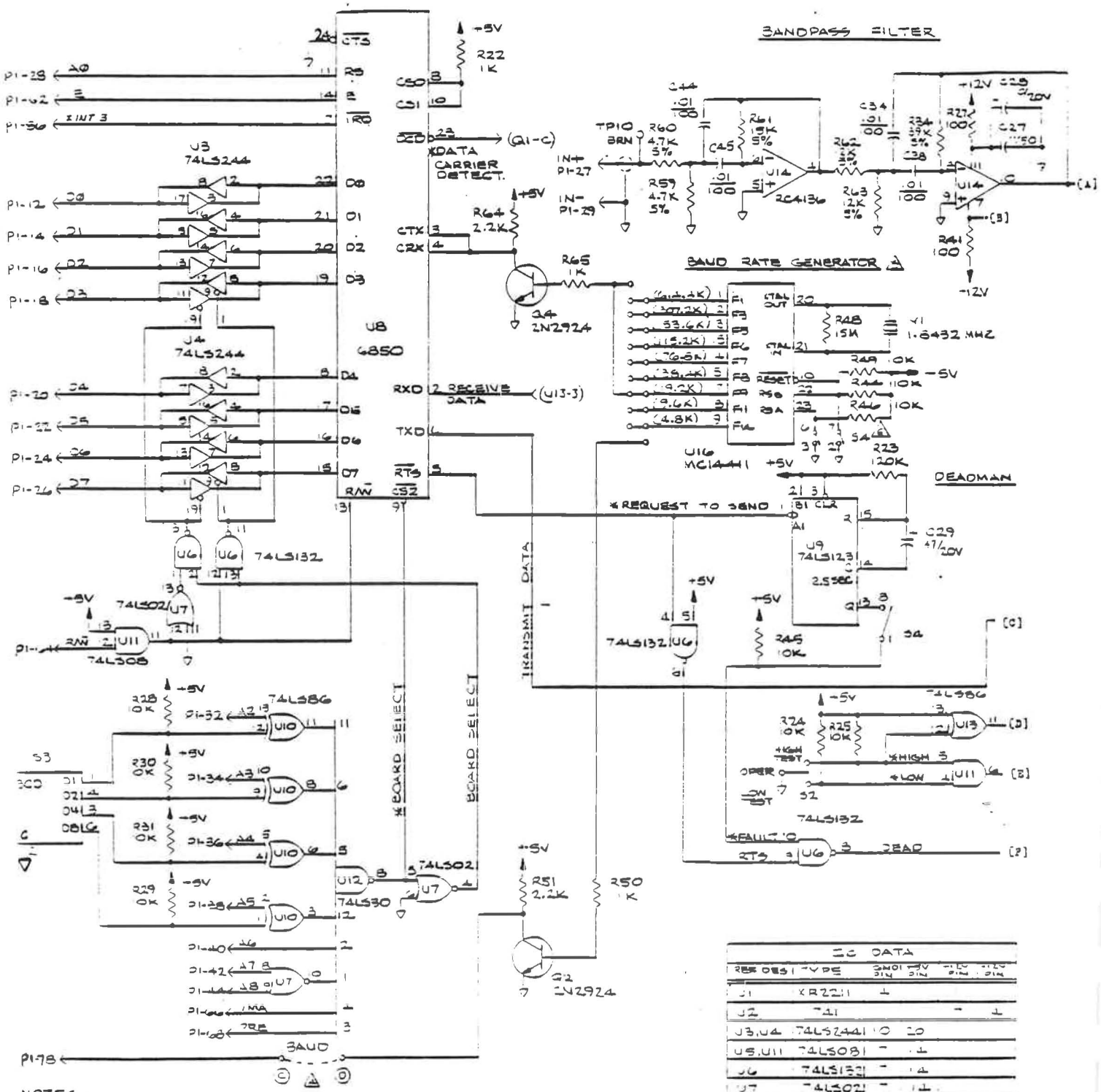
DWN	O.T.W.	6 SEPT 79	SCALE:
CHK		9-7-79	15A1114 A4
ENG			

REVISIONS	DATE	MOSELEY ASSOCIATES, INC.
A1 REVISED NOTE 7	9-12-80	SANTA BARBARA RESEARCH PARK
A REL. TO PROD. ECO 1999, 12-5-80		GOLETA, CALIFORNIA 93117

SCHEMATIC
MODEM II

TOL: FRACT. ± 1/32, XX ± .030, XXX ± .010, ∠ ± 1/2°

DWN	JRM	7-15-80	SCALE:
CHK	[illegible]	9-12-80	9107233 A1
ENG	[illegible]	11-5-80	



NOTES.

1. UNLESS OTHERWISE SPECIFIED, RESISTOR VALUES ARE IN OHMS, 1/4, 10% CAPACITOR VALUES ARE IN MICROFARADS.
2. PC BOARD 51C5909 REV.-11,-21.
3. COMPONENT LAYOUT 2002787 REV. A2.

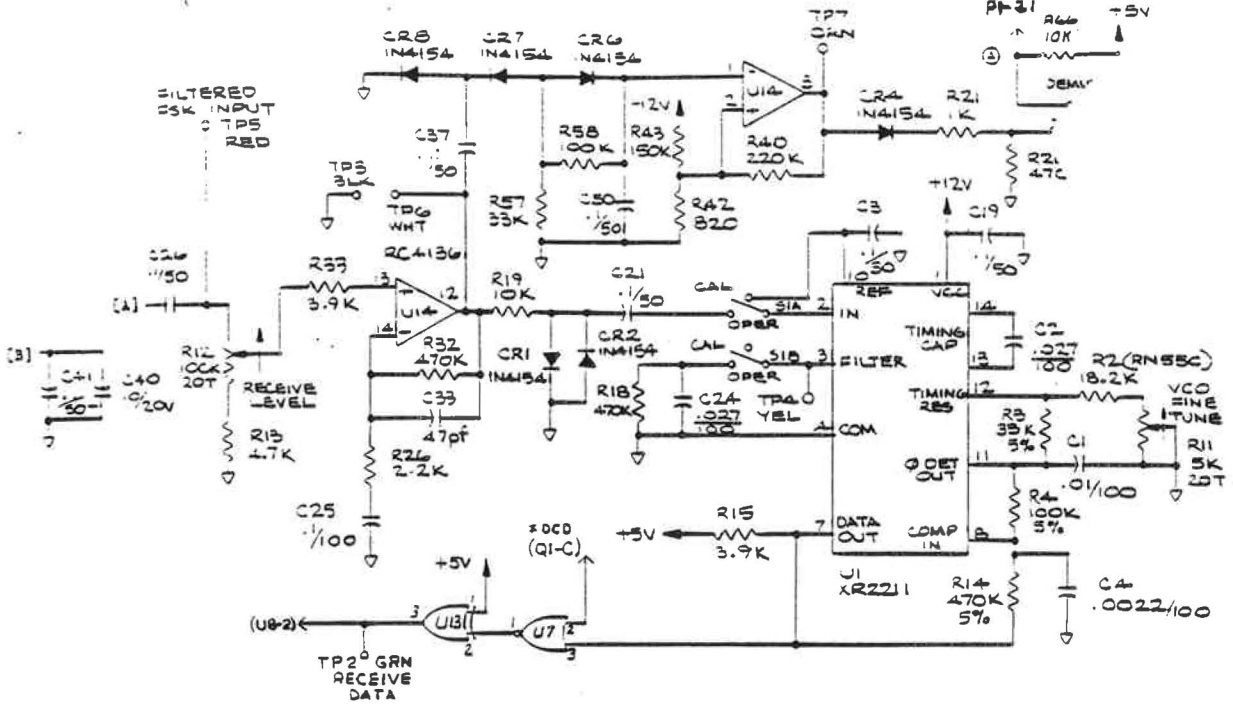
⚠ JUMPER AT [illegible] IS TO BE INSTALLED BY TEST, IF NEEDED

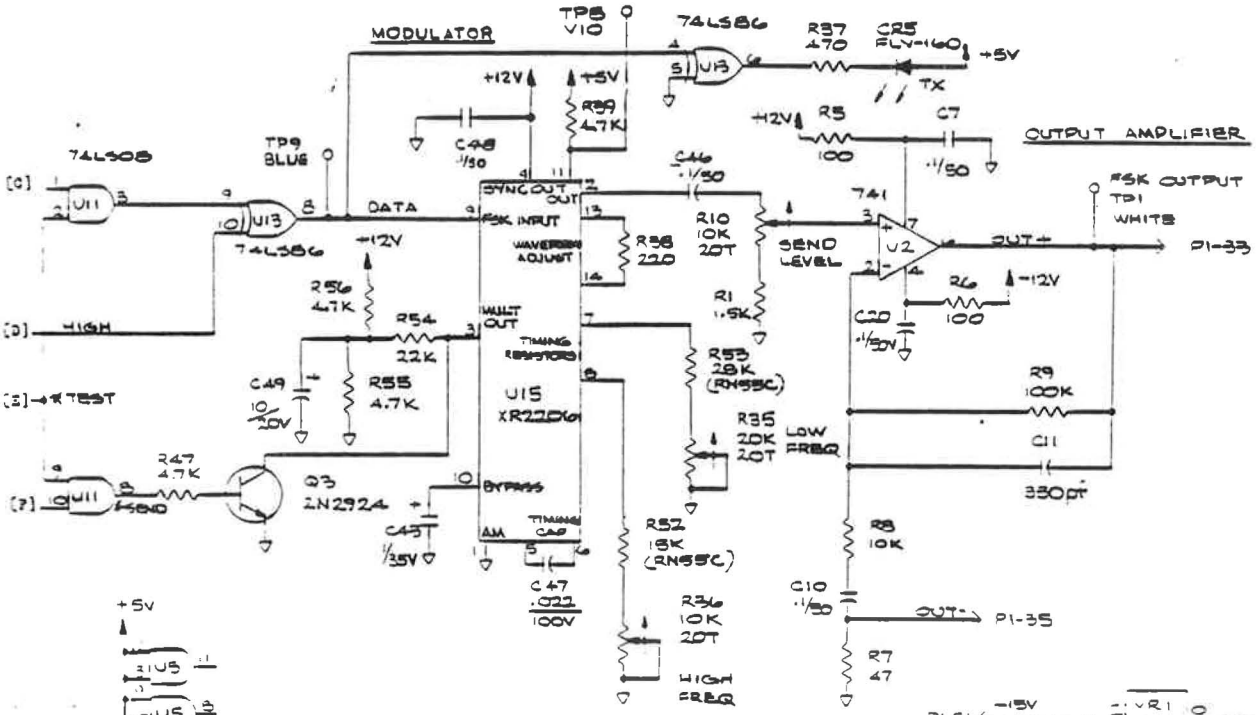
⚠ FOR FREQUENCIES SHOWN, S4-2 AND S4-3 ARE OPEN. FOR OTHER FREQUENCIES CONSULT THE "MOTOROLA CMOS DATA BOOK."

BAUD RATE	S4-2	S4-3
200	OFF	OFF
300	OFF	ON

I/C DATA

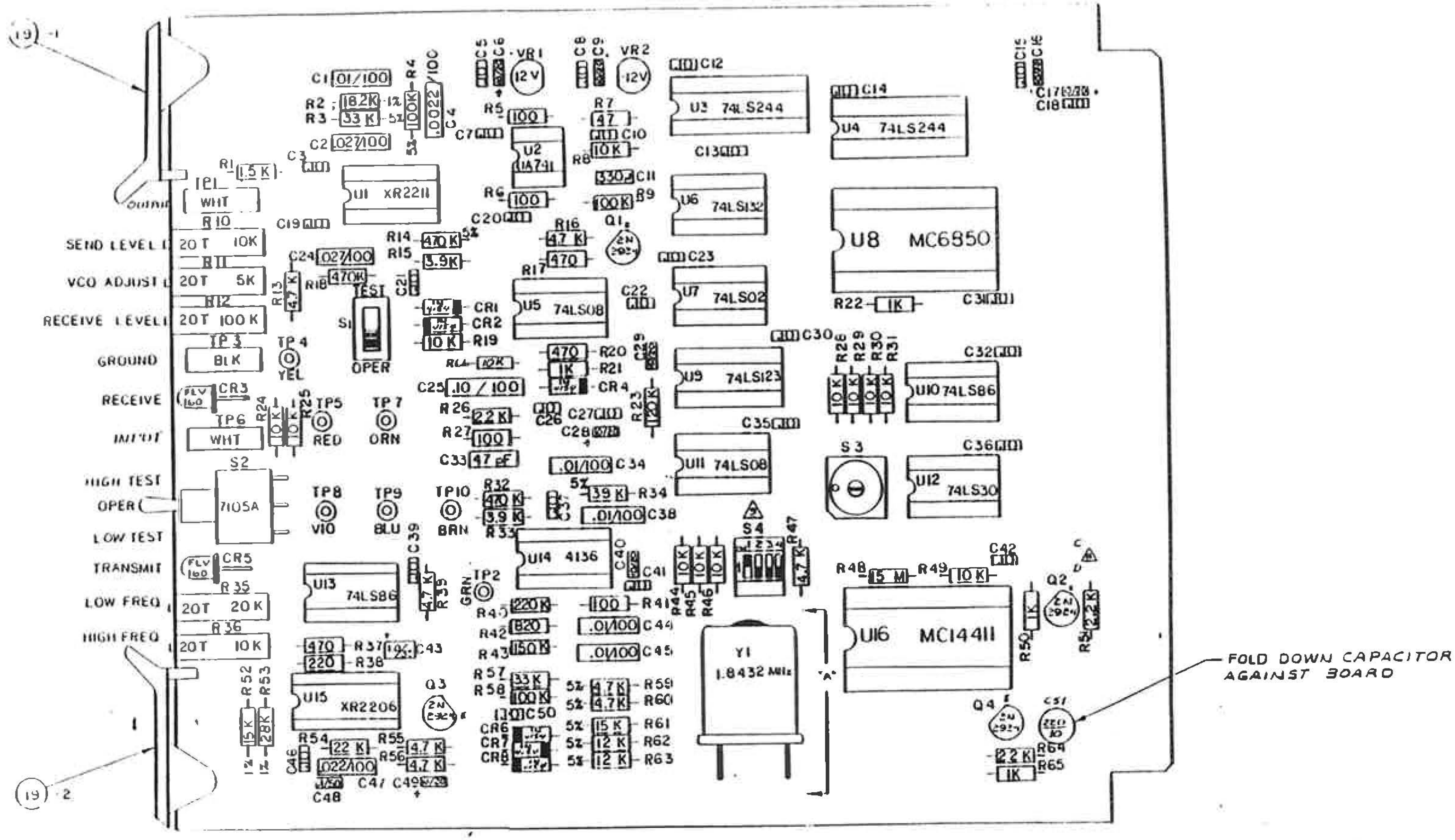
REF DES	TYPE	GND PIN	+5V PIN	-12V PIN	+12V PIN
J1	XR22:1	1			
J2	"	"		"	1
U3,U4	74LS244	10	20		
U5,U11	74LS08	"	14		
U6	74LS132	"	14		
U7	74LS02	"	14		
U8	6850		2		
U9	74LS123	8	16		
U10,U13	74LS86	"	14		
U12	74LS30	"	14		
U14	RC4136			1	"
J15	XR2556	2			1
U16	MC14411	2	24		



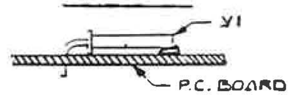


7 BASE ADDRESS: 8040H
CONTROL REGISTER: BASE+0+8CD (S3) x 4
DATA REGISTER: BASE+1+8CD(S3) x 4

MOSELEY ASSOCIATES, INC.
SCHEMATIC
MODEM II
4107232 A1



VIEW "A"



BEND LEADS AND TACK SOLDER TO BOARD.

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTOR VALUES ARE IN OHMS, 1/4 W, 10%;
   ALL CAPACITOR VALUES ARE IN MICROFARADS, 50V
2. P.C. BOARD 51C5809, REV.-11, -21.
3. SCHEMATIC 9107233, REV. A1.

REV	REVISIONS	DATE
A2	CR1, 2, 4, 6-8 WAS 1N4454. PCO 3000	4-30-81
A1	TP1 WAS INPUT, TP6 WAS OUTPUT, ECO 1993	1-21-81
A0	[illegible]	

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA 93017

COMPONENT LAYOUT
MODEM II

TOL: FRACT. ± 1/32, .XX ± .030, .XXX ± .010, ∠ ± 1/2°

DWN	[illegible]	2 SEPT 80	SCALE: 2X
CHK	[illegible]	9-11-80	2002787
ENG	[illegible]	11 SEPT 80	A2

					100
					99
					98
					97
	1		LABEL , MODEM 1081068-16	3430436	96
					95
	4	Q1-Q4	GE 2N2924 NPN	3430027	94
					93
	1	TP8	JOHNSON 105-0862-001	3290095	92
	1	TP9	JOHNSON 105-0860-001	3290087	91
	1	TP2	JOHNSON 105-0854-001	3290079	90
	1	TP4	JOHNSON 105-0857-001	3290061	89
	1	TP7	JOHNSON 105-0856-001	3290053	88
	1	TP5	JOHNSON 105-0852-001	3290046	87
	1	TP10	JOHNSON 105-0859-001	3290038	86
	1	TP3	SMITH 430-103 RT. ANGLE	3290145	85
	2	TP1,6	SMITH 430-101 RT. ANGLE	3290152	84
					83
	1	S2	C&K 7105A TOGGLE SPDT	3160181	82
	1	S1	CHICAGO SW. 23-021-114 DPDT	3190253	81
	1	S4	CTS 206-004 4PST	3190071	80
	1	S8 - YELLOW	SECO 2300576 BCD	3150	79
					78
					77
	2	J8,J16	AMP 640321-1 20 PIN SOCKET	3250077	76

	2	J1,J4	AMP 340484-1 22 PIN SOCKET	3250057	75
	2	J9,J15	AMP 640353-1 18 PIN SOCKET	3250032	74
	9	J5-7,J10-J14	AMP 340357-1 [illegible] PIN SOCKET	3250024	73
	1	J2	AMP 640463-1 24 PIN SOCKET	3250010	72
					71
	1	R48	A.B. 15M 10%	4410650	70
	2	R18,R32	A.B. 470K 10%	4410[illegible]	69
	1	R40	A.B. 250K 10%	4410536	68
	1	R43	A.B. 150K 10%	4410510	67
	1	R23	A.B. 120K 10%	4410502	66
	2	R9,R58	A.B. 100K 10%	4410494	65
	1	R57	A.B. 33K 10%	4410437	64
	1	R54	A.B. 22K 10%	4410411	63
	13	R8,19,24,25,46 [illegible]	A.B. 10K 10%	4410379	62
	6	R13,R14,39, [illegible]	A.B. 4.7K 10%	4410338	61
	2	R15,R33	A.B. 3.9K 10%	4410320	60
	3	R26,R51,R64	A.B. 2.2K 10%	4410288	59
	1	R1	A.B. 1.5K 10%	4410262	58
	4	R21,22,50,65	A.B. 1K 10%	4410247	57
	1	R42	A.B. 820 10%	4410239	56
	3	R17,20,27	A.B. 470 10%	4410205	55
	1	R38	A.B. 330 10%	4410163	54
	4	R5,6,27,41	A.B. 100 10%	4410122	53
	1	R7	A.B. 47 10%	4410080	52
	1	R14	A.B. 470K 5%	4460549	51
	1	R4	A.B. 100K 5%	4460481	50
	1	R34	A.B. 39K 5%	4460476	49
	1	R3	A.B. 33K 5%	4460330	48
	1	R61	A.B. 15K 5%	4460341	47
	2	R62,R63	A.B. 12K 5%	4460325	46
	2	R59,R60	A.B. 4.7K 5%	4460242	45
	1	R53	MEP. ELEC. RN55C 2502F	4510194	44
	1	R2	MEP. ELEC. RN55C 1823F	4510172	43
	1	R52	MEP. ELEC. RN55C 1502F	4510152	42
					41
	1	R12	BOURNS 3006P-1-104	4630328	40
	1	R35	BOURNS 3006P-1-203	4630420	39
	2	R10,R36	BOURNS 3006P-1-103	4630412	38
	1	R11	BOURNS 3006 P-1-502	4630299	37
					36
	1	VR2	MOTOROLA MC79L12 -12V REG.	TO-1 3650140	35
	1	VR1	MOTOROLA MC78L12 12V REG.	TO-1 3650124	34
	1	U2	T.I. μA741CP OP-AMP	DIP 3660008	33
	1	U15	EXAR XR2206CP FUNCTION GENERATOR	DIP 3730819	32
	1	U9	T.I. SN74LS123N DUAL ONE-SHOT	DIP 3660769	31
	1	U16	MOTOROLA MC14411P BIT RATE GEN.	DIP 3680212	30
	1	U12	T.I. SN74LS20N 4-INPUT NAND	DIP 3660735	29
	2	U10,U13	T.I. SN74LS86N QUAD EX-OR	DIP 3660743	28
	2	U5,U11	T.I. SN74LS03N QUAD 2-INP. NAND	DIP 3660695	27
	1	U7	T.I. SN74LS02N QUAD NOR	DIP 3660677	26
	1	U6	T.I. SN74LS132N QUAD SCHMITT NAND	DIP 3660776	25
	1	U1	EXAR XR2211CP FSK DEMODULATOR	DIP 3730327	24
	1	U14	T.I. RC4136N QUAD 741 OP-AMP	DIP 3730462	23
	1	U8	MOTA. MC6850P ACIA	DIP 3710043	22
	2	U3,U4	T.I. SN74LS240N BUS TRANSCEIVER	DIP 3660859	21
					20
	1	EJECTOR KIT	VERO, 612409-1/-2		1250075	19
					18
	2	CR3,CR5	FAIRCHILD FLV160 L.E.D.	3390127	17
	6	CR1,2,4 CR6-8	GE 1N4154 SMALL SIGNAL	3300145	16
					15
	1	Y1	CRYSTAL, 1.8432 MHz	3040073	3340726	14
	1	C31	<220 EIO 220 /10		4220186	13
	1	C6,10,17,29, [illegible]	SPRAG. 1960106X0025KAT 10/20		4250073	12
	1	C43	SPRAGUE 1960105X0025HA1		4250035	11
	[illegible]	[illegible]	C.R.L. CV20C104MM		10
	1	C35	SEC. 22UB104H C.1/100		4250486	9
	2	C3,C34	SEC. 22UB273H C.027/100		4250312	8
	1	C47	SEC. 22UB223H C.022/100		4250336	7
	5	C4,24,38,44,[illegible]	SEC. 22UB1C3H C.1/100		425017	6
	1	C40	SEC. 22UB223H C.022/100		4250349	5
	1	C21	CED IND. CM-15-331J 330pF		4210415	4
	1	C33	SEC. NO. CM-15-470J 47pF		4210187	3
	1	C39	SPRAGUE 1960476X0020 D64 47μF/20		4290137	2
	1	P.C. BOARD	MAI 81C9003 REV.-11-21		3472420	
ITEM	QTY	REF DES.	DESCRIPTION		STOCK NO.	ITEM

MOSELEY ASSOCIATES, INC.

COMPONENT LAYOUT

MODEM II

2002787 AZ

MODEM TELCO INTERFACE

Schematic 91A7147
Assembly 20B2716
PC Board 51B5856

I. PURPOSE

This interface card interconnects the modem with either a 2-wire or 4-wire dedicated circuitry telephone line. Telephone line interconnections are balanced, isolated, fused and filtered.

II. SPECIFICATIONS

Output Distortion	1.5% or less
Input/Output Impedance	300 ohms or 600 ohms strappable by user

III. THEORY OF OPERATION

Telephone line inputs are filtered to reduce RF interference. Each input line is individually fused, using an AGC 1/4-amp fuse. Transformers T1 and T2 are 600-ohm to 600-ohm matching transformers. Resistors R1, R2, R4 and R5 are used to convert 600 ohms to 300 ohms for use in the 2-wire mode. Resistors R3 and R6 are used in the 4-wire mode to make the phone line connections approximately 600 ohms. Diodes D1 through D4 are used to protect the transformers and modem board from large transients on the telephone line.

Two interconnection schemes are possible using this board. The 2-wire scheme uses a single pair of wires for communi-

cating in both directions. The 4-wire system uses two pairs of wires separating both telemetry and control signals. The connections necessary for 2-wire interconnections are shown in Fig. 1. Figure 2 illustrates 4-wire connections. When interconnecting a Control Terminal with Remote Terminals, no special line polarity must be observed as each input is a balanced 300 ohms or 600 ohms.

A Bell 3002, unconditioned data circuit is specified. The use of long (over 1000 ft.) DC continuous circuits is not recommended as their AC frequency response is not guaranteed, and induced currents may prove troublesome.

IV. TROUBLESHOOTING

1. Check fuses and fuse clips for continuity.
2. After lightning damage:
   a. Check inductors for open circuits.
   b. Diodes D1 through D4 may be shorted.
   c. Capacitors C1 through C8 may be shorted.
   d. Check transformer continuity.

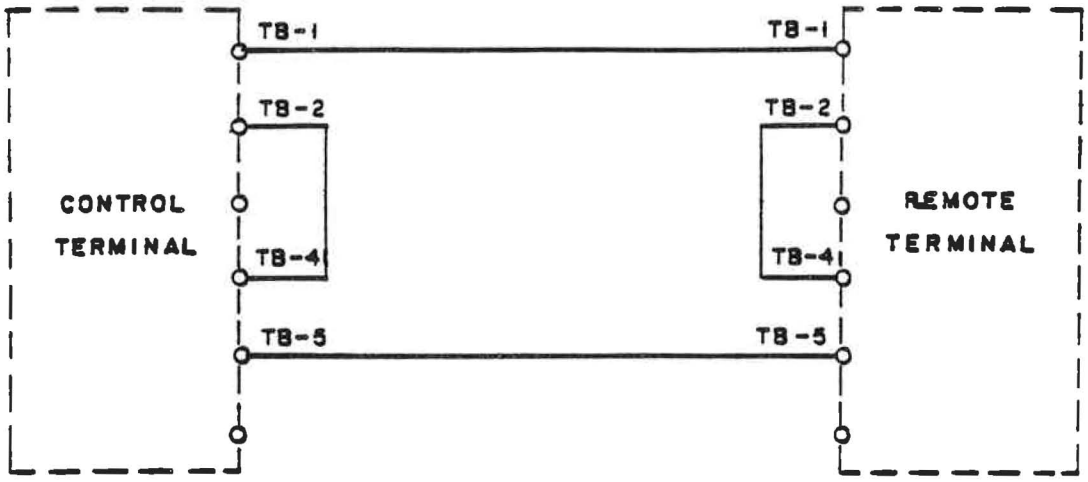


FIGURE 1
TWO-WIRE INTERCONNECTIONS

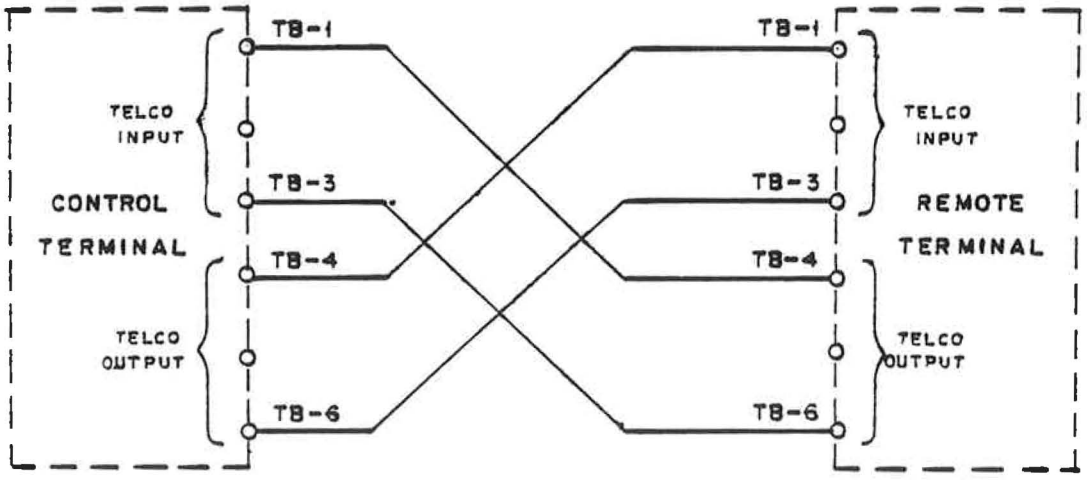
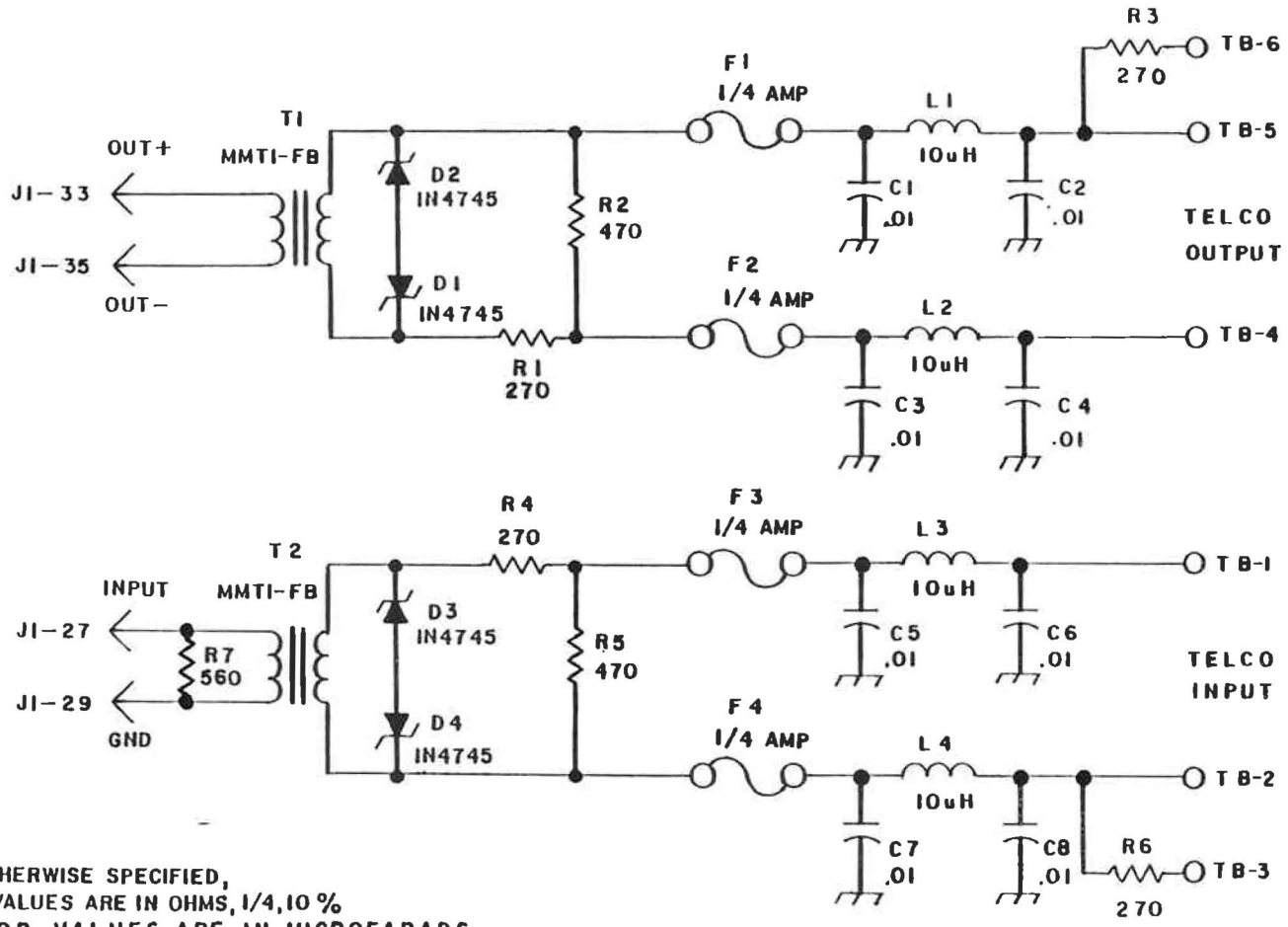


FIGURE 2
FOUR-WIRE INTERCONNECTIONS



NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTOR VALUES ARE IN OHMS, 1/4, 10 % CAPACITOR VALUES ARE IN MICROFARADS.
2. FOR 2 WIRE MODE INSTALL PHONE LINE ACROSS TERMINALS TB-1 AND TB-4 INSTALL JUMPER BETWEEN TB-2 AND TB-5.
3. FOR 4 WIRE MODE USE TERMINALS TB-4 AND TB-6 FOR OUTPUT. USE TERMINALS TB-1 AND TB-3 FOR INPUT.
4. ⏚ IS DIRECT CHASSIS GROUND.
5. P.C. BOARD 51B5856
6. COMPONENT LAYOUT 20B2716.

FIRST USED ON MRC-1

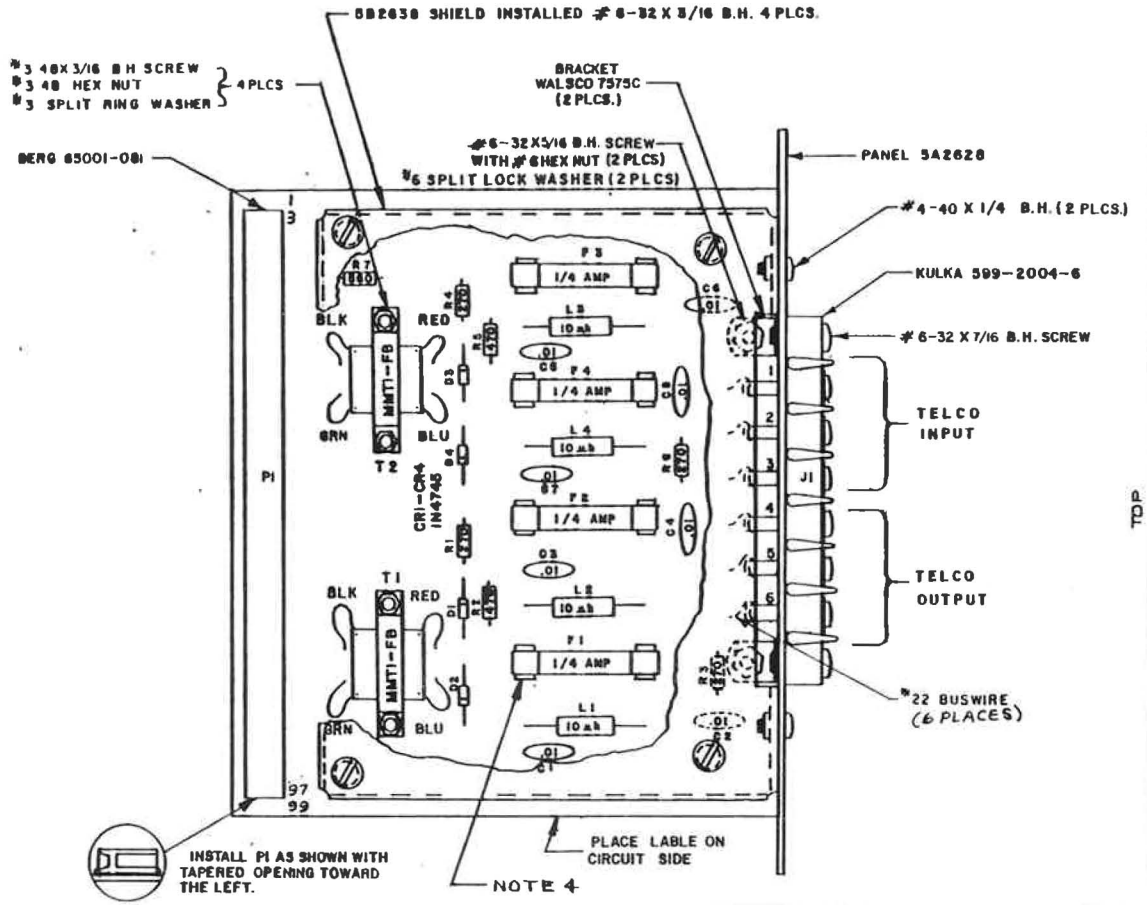
REVISIONS	DATE	MGMT. APPR.
A RELEASED FOR PRODUCTION. 12APR79 F.X.Y.		

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA 93017

SCHEMATIC
MRC-1 MODEM TELCO INTERFACE

TOL: FRACT. ± 1/32, .XX ± .030, .XXX ± .010, ∠ ± 1/2°

DWN	A.J.B.	9 JAN 79	SCALE:
CHK	F X Y	24 JAN 79	91A7147 A
ENG	[illegible]	25 APR 79	



NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTOR VALUES ARE IN OHMS, 1/4, 10%
2. P.C. BOARD 5185856-02
3. SCHEMATIC 91A7147
4. SOLDER FUSE CLIP EYELETS TO CIRCUIT SIDE OF BOARD.

REVISIONS	DATE	MGMT. APPR.
C2 ADD NOTE 4 PER 10B1825 WPS 31MAR 80		
C1 ADD LABEL 10A1069-2 PER ECO 1686 WPS 25APR 80		
B1 BERG 65001-081 WAS BERG 65001-083. ECO 1362 WPS 5 SEPT 79		
A1 CHANGES AS PER P.C.O. 1321. 10AUG 79. D.T.W.		
A RELEASED FOR PRODUCTION. ZEPHYR'S P.O.#		

ADD PARTS LABLE ON BASIS OF P.C.O. 1886 AJB. ALSO,

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SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA 93017

COMPONENT LAYOUT
MRC-1 MODEM TELCO INTERFACE

TOL: FRACT. ± 1/32, .XX ± .030, .XXX ± .010, ∠ ± 1/2°

DWN	A J.B.	2 JAN 79	SCALE: 1:1
CHK	F.X.Y	24 APR 79	20B2716 C2
ENG	W.L.L.	25 APR 79	

TELCO IN/SUBCARRIER OUT

Schematic 91B7144
Component Layout 20A2737
PC Board 51B5865

I. PURPOSE

This board transmits data via an FM subcarrier and interfaces the modem demodulator with the telephone line for received data. This board is the companion board for Moseley Telco Out/Subcarrier In (20B2736). Operation in several standard subcarrier bands is possible by specifying different frequency selective components.

II. DESCRIPTION

Incoming data on the telephone is filtered by L1 and L2 to reduce radio frequency interference. Fuses F1 and F2 are used for protection from large surges on the phone line. Resistors R13, R14, and R15 form a 600 ohm impedance matching network between the phone line and the transformer. T1 is a 600 ohm to 600 ohm impedance matching transformer.

An XR-2206 function generator (IC U1) is used to generate an FM signal from the frequency shift keyed output of the standard modem board. The frequency of oscillation is controlled by applying a control voltage to the activated timing pin, (Pin 7). Resistors R8, R9, R10, and R20 form a voltage divider network used to adjust the frequency control voltage. Timing capacitor, C6 is also used for frequency control. Its value is dependent on which subcarrier band is used. Capacitor C5 is a bypass capacitor

required by the IC. Resistors R6 and R7 are used to reduce the total harmonic distortion. THD can be reduced to 1/2% by trimming, or in the worst case, approximately 2.5%. The DC output level is adjusted by applying a voltage bias to Pin 3, using R5.

III. ADJUSTMENT

a. Subcarrier Generator

1. Remove modulation applied to subcarrier generator using the send level pot on the modem (R50).

2. Connect a frequency counter to the "GEN OUT" BNC. Adjust subcarrier frequency using pots R19 and R20. R19 is a course frequency adjustment. R20 is a fine frequency adjustment. Both pots are accessible from the rear panel and are labelled "COARSE" and "FINE".

3. Disconnect the frequency counter and connect a distortion analyzer to the generator output BNC. Adjust distortion pot R6 for minimum distortion. Using this control approximately 1/2% distortion is obtainable. If no distortion analyzer is available, no adjustment on this pot is required. The worst case distortion is approximately 2.5% which is quite acceptable in most applications.

4. Disconnect the analyzer and attach an oscilloscope to the generator output. To understand this adjustment, refer to print number 15A1114 (See modem section) for representative waveforms. Adjust the oscilloscope to display about 6 periods of the unmodulated subcarrier as shown in (A). Using the modem send level pot, increase subcarrier modulation until the fifth crossover occurs midway as shown in (B).

5. Adjust the output level to 2.5 volts peak-to-peak using R14. This pot is labelled "OUT" and is accessible through the rear panel.

IV. TROUBLESHOOTING

a. Verify that +12 volts DC is present on Pin 4 of IC U1.

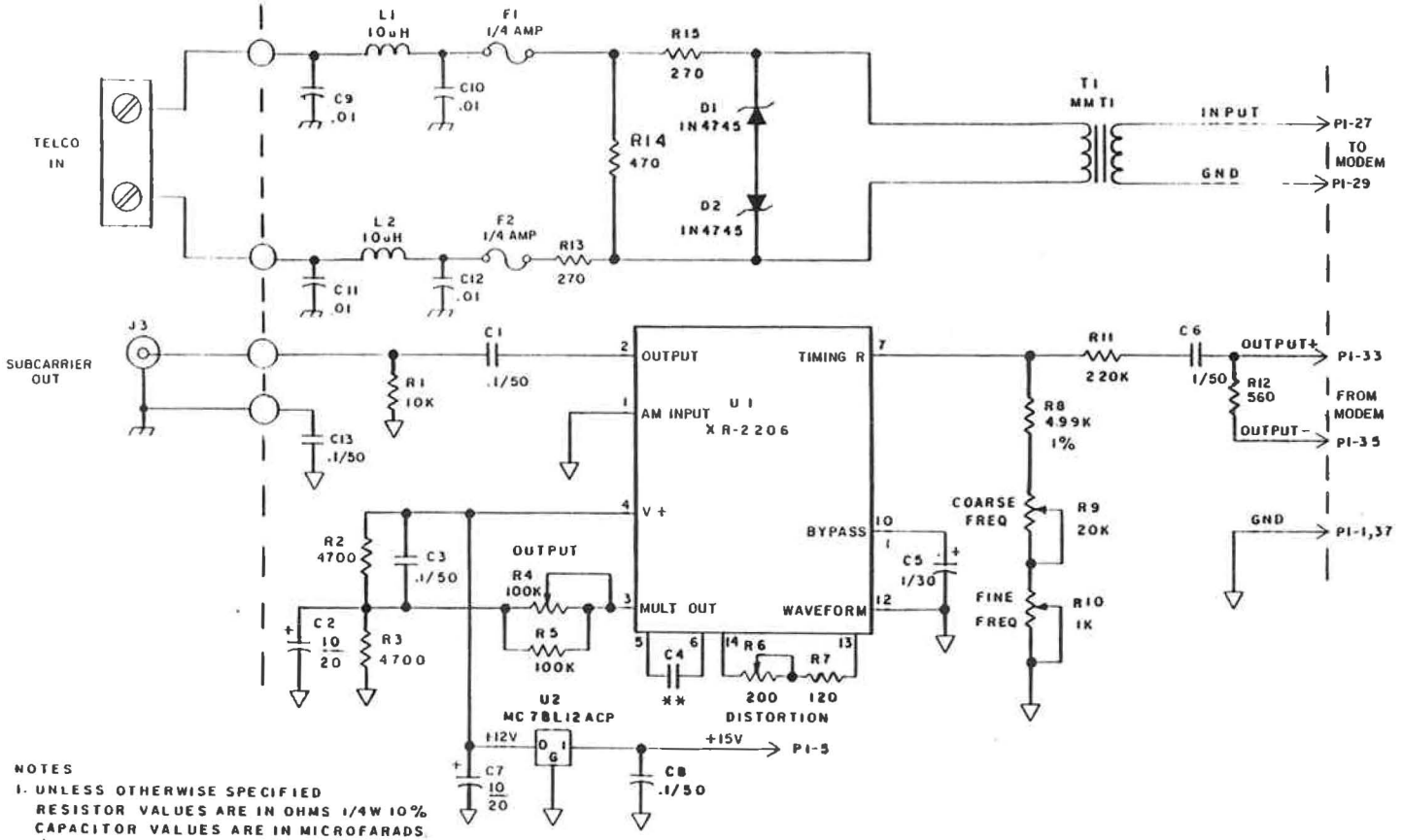
b. Modulator

1. Verify that modem is generating a FSK signal which may be observed at Pin 7 of the XR2206 function generator (IC U1).

2. If no output is observed, check on chip voltages and grounds. If the IC is replaced, verify proper adjustment by performing the subcarrier adjustment procedure described previously.

3. Note the modem card must be properly adjusted and working correctly for the subcarrier board to function. Refer to the modem section of this manual for troubleshooting details.

9187144 A2



**	FREQ	C4
ITEM 1	20 KHZ	2530 pf
ITEM 2	26 KHZ	1930 pf
ITEM 3	39 KHZ	1300 pf
ITEM 4	67 KHZ	750 pf
ITEM 5	110 KHZ	560 pf
ITEM 6	200 KHZ	470 pf

NOTES

1. UNLESS OTHERWISE SPECIFIED RESISTOR VALUES ARE IN OHMS 1/4W 10% CAPACITOR VALUES ARE IN MICROFARADS.
2. ▽ IS GROUND ON CPU BUS.
   ⏚ IS DIRECT CHASSIS GROUND.
3. P.C. BOARD 51B5865-02
4. COMPONENT LAYOUT 20A2737 C3

REVISIONS	DESCRIPTION	DATE	MGMT. APPR.
A2	PARTS LIST CHANGE PER ECO 1092 9-22-80 W.K.		
A1	ADDED U2. INFORMATION. PCD 1847. 1 FEB. 80 BWF		
A	RELEASED FOR PRODUCTION F.X.Y. 30APR79		

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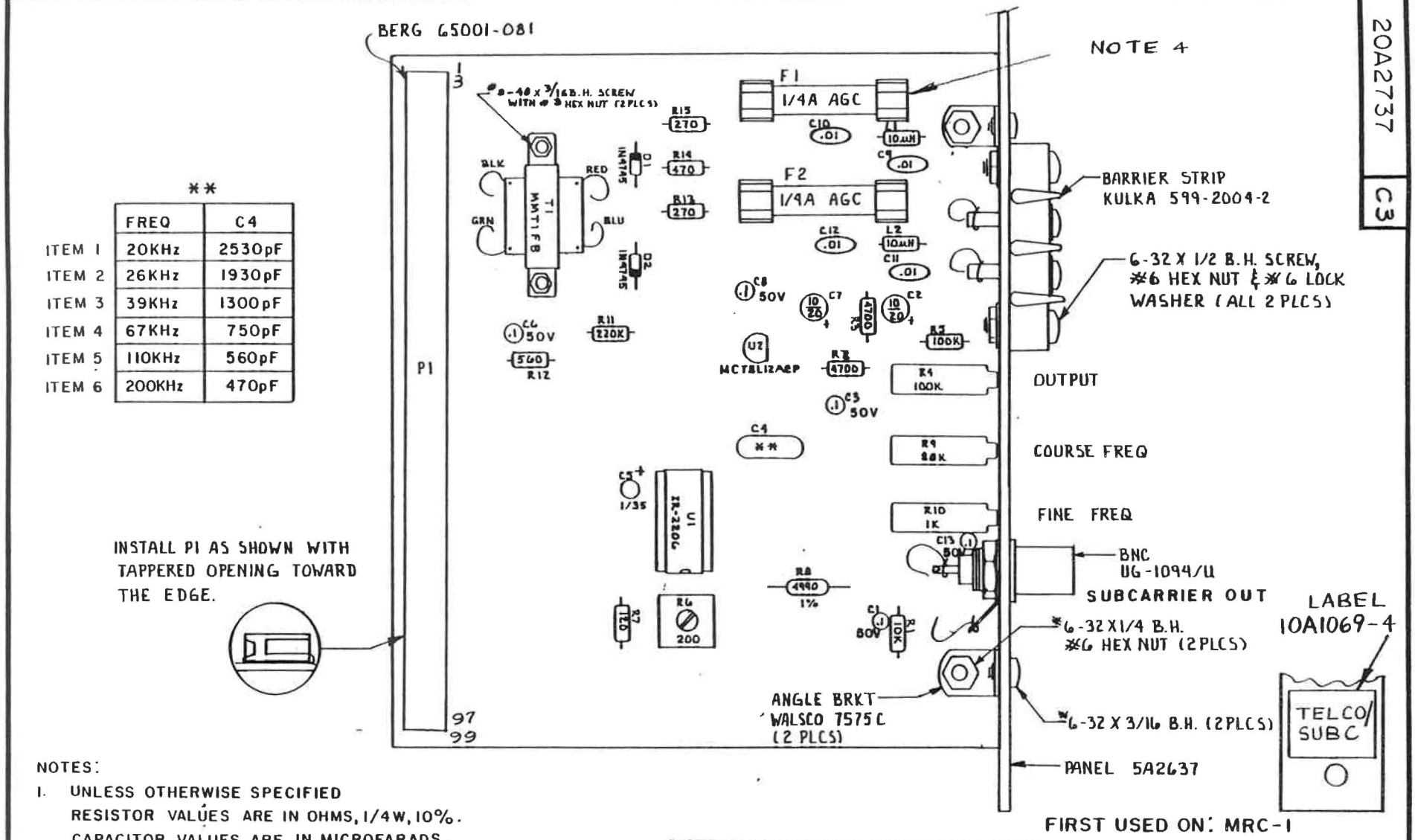
SCHEMATIC
TELCO IN / SUBCARRIER OUT

TOL: FRACT. ± 1/32, .XX ± .030, .XXX ± .010, ∠ ± 1/2°

DWN	L.I.	28DEC78	SCALE: NONE
CHK	F.X.Y.	26APR79	9187144 A2
ENG	W.H.	30 APR 79	

PRINTED ON DIETERICH POST CLEANPRINT 1010-8



**

	FREQ	C4
ITEM 1	20KHz	2530pF
ITEM 2	26KHz	1930pF
ITEM 3	39KHz	1300pF
ITEM 4	67KHz	750pF
ITEM 5	110KHz	560pF
ITEM 6	200KHz	470pF

NOTES:

1. UNLESS OTHERWISE SPECIFIED RESISTOR VALUES ARE IN OHMS, 1/4W, 10%. CAPACITOR VALUES ARE IN MICROFARADS.
2. P.C. BOARD 5IB5865-02.
3. SCHEMATIC 9IB7144. A2
4. SOLDER FUSE CLIP EYELETS TO CIRCUIT SIDE OF BOARD.

REVISIONS	DATE	MGMT. APPR.
C3 PARTS LIST CHANGE PCO1892, 9-22,80 ABT		
C2 ADD NOTE 4 PCO1823 WPG 31 JUL 80		
C1 ADD LABEL 10A1069-4 ECO1696 WPG 25AUG80		
B1 ADDED "ACP" TO U2. PCO 1567. 31 JAN 80 BWF		
B0 BERG 65001-081 WAS 65001-085. ECO1362 4SEPT79 D.T.W.		
A RELEASED FOR PRODUCTION. 30 APR 79 F.X.Y.		

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COMPONENT LAYOUT
TELCO IN-SUBCARRIER OUT INTERFACE

TOL: FRACT. ± 1/32, .XX ± .030, .XXX ± .010, ∠ ± 1/2°

DWN	JAM	9APR79	SCALE: FULL
CHK	FXY	26APR79	
ENG	WLL	30 APR 79	20A2737 C3

FIRST USED ON: MRC-1

20A2737 C3

TELCO OUT/SUBCARRIER IN

Schematic 91C7160
Component Layout 20B2736
PC Board 51A5870

I. PURPOSE

This board interconnects transmitted signals from the modem with a dedicated telephone line, and demodulates FM subcarrier data transmissions to provide received data to the modem. This board is the companion board to the Telco In/Subcarrier Out assembly (20A2737). Operation in several different standard subcarrier bands is possible by selection of component values.

II. DESCRIPTION

The XR2211 is a phase-locked loop used to demodulate the incoming FM subcarrier. The input filter connected to Pin 2 is a telemetry extraction bandpass filter and is used to reject frequencies other than the telemetry subcarrier. The components used in the input filter are frequency dependent and are specified according to the subcarrier band being used. Recommended signal input at Pin 2 is from 10 mV rms to 3 mV rms. The operating frequency is determined by C5, R5 and R6. Resistor R3 and Capacitor C9 form a lock detect filter to eliminate chatter at the lock detect output (Pin 5). Capacitor C8 is used as a bypass capacitor for an internal voltage reference. The demodulated output is taken from the loop phase detector (Pin 11), through a post detection filter made up of R7 and C12, and an external buffer amplifier. This buffer amplifier is necessary because of the high impedance output at Pin 11. A non-inverting unity gain 741 op amp is used as a buffer.

III. ADJUSTMENT

1. Telemetry Extraction Filter Adjustment

   Apply a modulated subcarrier signal to the input. Adjust inductors L1 and L2 for maximum amplitude and minimum AM. The filter output should be similar in appearance to the subcarrier generator output.

2. FM Demodulator Frequency Adjustment

   Apply a modulated subcarrier to the input. Adjust R5 for the cleanest FSK output. Note that some residual high frequency subcarrier may be superimposed on the FSK signal, this is quite normal.

IV. TROUBLESHOOTING

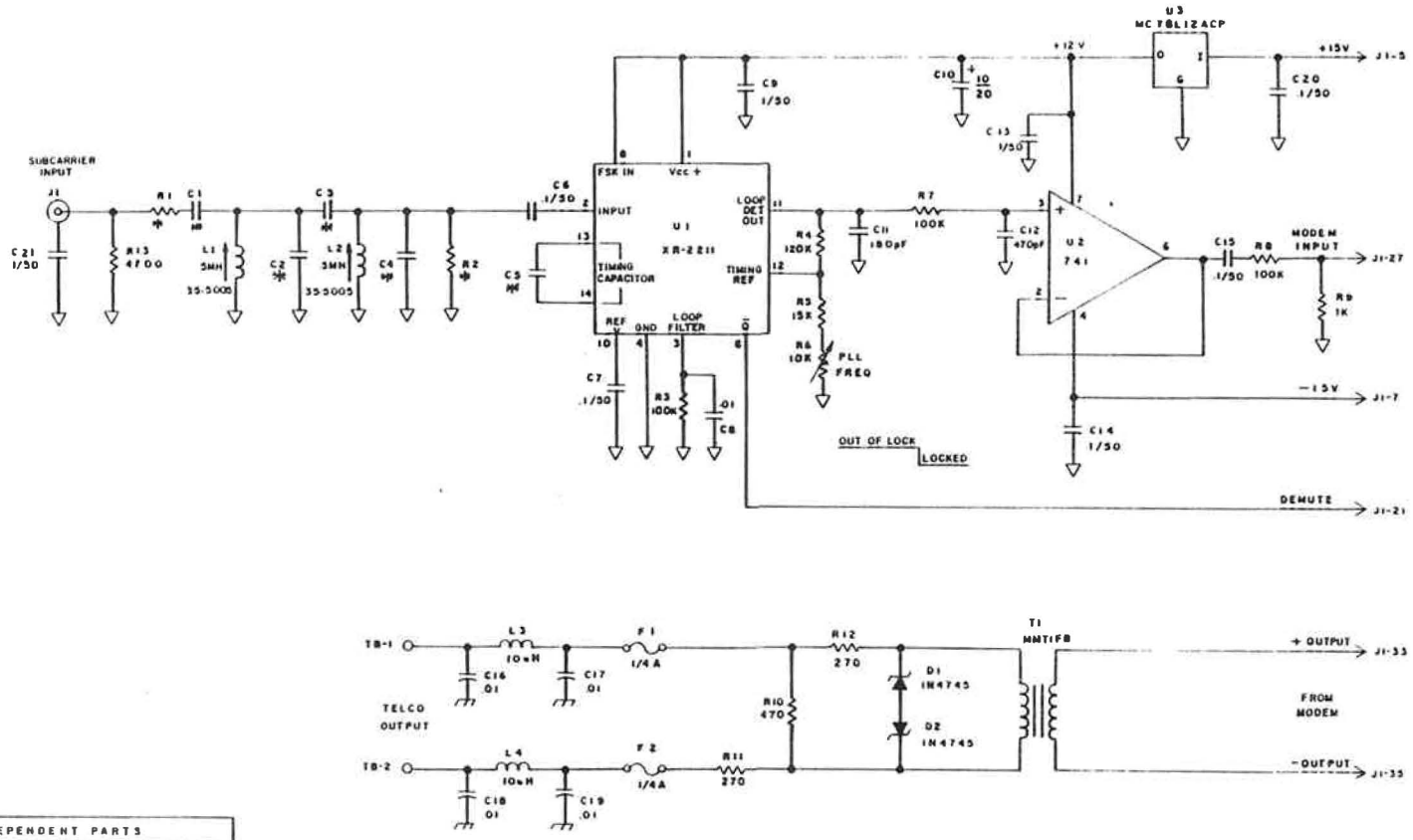
a. Verify correct power supply voltages are present on the board (+5, +12, and -15 volts).

b. Using an oscilloscope, observe the extraction filter output at IC U1, Pin 2. This signal should appear much like the subcarrier generator output. If it is distorted, check input filter for proper tuning or defective components.

c. Check demodulator frequency as described in adjustment section.

d. Check operation of 741 Buffer Amp.

e. Check operation of modem board. Refer to modem section of manual.



* FREQ DEPENDENT PARTS							
	R1	R2	C1	C2	C3	C4	C5
20KHZ	470	1500	0131	.111	0175	.111	2550pF
26KHZ	470	1800	008	068	01	068	1950pF
39KHZ	820	2700	5600pF	.031	4700pF	031	1300pF
67KHZ	1500	4700	0012	01	0016	01	750pF
110KHZ	2200	6800	470pF	3600pF	620pF	3600pF	470pF
200KHZ	3900	15K	330pF	1110pF	180pF	1110pF	270

NOTES:

1 UNLESS OTHERWISE SPECIFIED
RESISTOR VALUES ARE IN OHMS 1/4W 10%
CAPACITOR VALUES ARE IN MICROFARADS

2 P C BOARD 51A5870-01

3 COMPONENT LAYOUT 20B2756

FIRST USED ON MRC-1

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA 93117

SCHEMATIC
TELCO OUT/SUBCARRIER IN

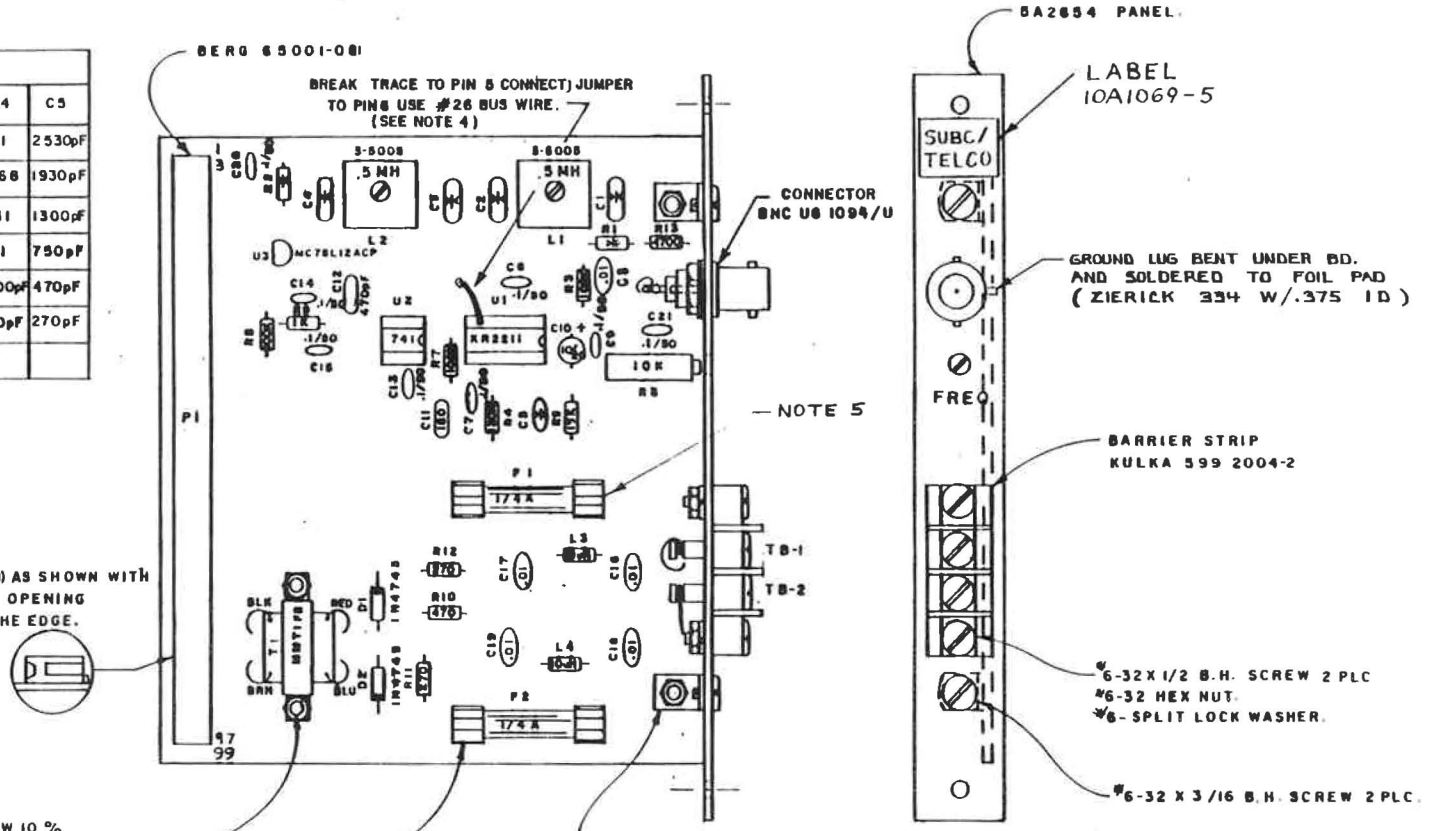
DWN L. I. 9MAR79 SCALE: NONE

91C7160 B1

91C7160 B1

20B2736 D3

* FREQ DEPENDENT PARTS							
	R1	R2	C1	C2	C3	C4	C5
ITEM 1	20KHZ 470	1500	.0131	.111	.0175	.111	2530pF
ITEM 2	26KHZ 470	1800	.008	.068	.01	.068	1930pF
ITEM 3	39KHZ 820	2700	3600pF	.031	4700pF	.031	1300pF
ITEM 4	67KHZ 1500	4700	1200pF	.01	.0016	.01	750pF
ITEM 5	110KHZ 2200	6800	470pF	3600pF	620pF	3600pF	470pF
ITEM 6	200KHZ 3900	15K	130pF	1110pF	180pF	1110pF	270pF



NOTES:

1. UNLESS OTHERWISE SPECIFIED
   RESISTOR VALUES ARE IN OHMS 1/4 W 10 %
   CAPACITOR VALUES ARE IN MICROFARADS
2. P. C. BOARD 51A5870-01
3. SCHEMATIC 91C7160
4. BREAK TRACE AND CONNECT JUMPER AS SHOWN.
5. SOLDER FUSE CLIP EYELETS TO CIRCUIT SIDE OF BOARD.

FIRST USED ON MRC-I

D3	ADD NOTE 5 PCO 1823 WPS 31JUL80		
D2	ADD LABEL 10A1069-5 ECO 1646 WPS 12APR80		
C2	ARTWORK CHANGE 04. PCO 1533 RFEBBD D.T.W.		
C1	ADDED U3 PER MANUFACTURER. PCO 1687. 31 JAN 80 BWF		
C0	ECO 1488: CHANGE ADD LABEL, C13, C11 & T1 VALUES. C13, C11 & T1 HANDPARE. 8 DEC 79 BWF		
B0	BERG 65001-081 WAS 65001-085. ARTWORK REV 02. ECO 1362 RELEASED FOR PRODUCTION 4 MAY 79 D.T.W.		
A1	RELEASED FOR PRODUCTION A.J.B.		
REVISIONS		DATE	
DRAFT. APPR.			

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA 93017

COMPONENT LAYOUT TELCO OUT SUBCARRIER IN

TOL: FRACT. ± 1/32, .XX ± .030, .XXX ± .010, ∠ ± 1/2°

DWN	L.I.	12APRIL79	SCALE: FULL
CHK			20B2736 D3
ENG			

SUBCARRIER INTERFACE

Schematic 91C7156
Parts Layout 20B2719
PC Board 51B5858

I. PURPOSE

This board, when used with the modem board (20B2732) generates and demodulates FM subcarrier data transmissions.

II. DESCRIPTION

An XR-2206 function generator (IC U3) is used to generate an FM signal from the frequency shift keyed output of the standard modem board. The frequency of oscillation is controlled by applying a control voltage to the activated timing pin, (Pin 7). Resistors R17, R18, R19 and R20 form a voltage divider network used to adjust the frequency control voltage. Timing capacitor, C6, is also used for frequency control. Its value is dependent on which subcarrier band is used. Capacitor, C20 is a bypass capacitor required by the IC. Resistors R15 and R16 are used to reduce the total harmonic distortion. This can be reduced to 1/2% by trimming, or in the worst case, approximately 2.5%. The DC output level is adjusted by applying a voltage bias to Pin 3, using R14. The XR2211 is a phase-locked loop used to demodulate the incoming FM subcarrier. The input filter connected to Pin 2 is a telemetry extraction bandpass filter and is used to reject frequencies other than the telemetry subcarrier. The components used in the input filter are frequency dependent and are specified according to the

subcarrier band being used. Recommended signal input at Pin 2 is from 10 mV rms to 3 mV rms. The operating frequency is determined by C5, R5 and R6. Resistor R3 and Capacitor C9 form a lock detect filter to eliminate chatter at the lock detect output (Pin 5). Capacitor C8 is used as a bypass capacitor for an internal voltage reference. The demodulated output is taken from the loop phase detector (Pin 11), through a post detection filter made up of R7 and C12, and an external buffer amplifier. This buffer amplifier is necessary because of the high impedance output at Pin 11. A non-inverting unity gain 741 op amp is used as a buffer.

III. ADJUSTMENT

a. Subcarrier Generator

1) Remove modulation applied to subcarrier generator using the send level pot on the modem (R50).

2) Connect a frequency counter to the "GEN OUT" BNC. Adjust subcarrier frequency adjustment. R20 is a fine frequency adjustment. Both pots are accessible from the rear panel and are labeled "COARSE" and "FINE".

3) Disconnect the frequency counter and connect a distortion analyzer to the generator output BNC. Adjust distortion pot R6 for minimum distortion. Using this control approximately 1/2% distortion is obtainable. If no distortion analyzer is available no adjustment on this pot is required. The worst case distortion is approximately 2.5% which is quite acceptable in most applications.

4) Disconnect the analyzer and attach an oscilloscope to the generator output. To understand this adjustment, refer to print number 15A1114 (See modem section) for representative waveforms. Adjust the oscilloscope to display about 6 periods of the unmodulated subcarrier as shown in (A). Using the modem send level pot, increase subcarrier modulation until the fifth crossover occurs midway as shown in (B).

5) Adjust the output level to 2.5 volts peak-to peak using R14. This pot is labelled "OUT" and is accessible through the rear panel.

b. Subcarrier Demodulator

1) Telemetry Extraction Filter Adjustment

Apply a modulated subcarrier signal to the input. Adjust inductors L1 and L2 for maximum amplitude and minimum AM. The filter output should be similar in appearance to the subcarrier generator output.

2) FM Demodulator Frequency Adjustment

Apply a modulated subcarrier to the input. Adjust R5 for the cleanest FSK output. Note that some residual high frequency subcarrier may be superimposed on the FSK signal, this is quite normal.

IV. TROUBLESHOOTING

a. Verify correct power supply voltages are present on the board (+5, +12, and -15 volts).

b. Modulator

1) Verify that modem is generating a FSK signal which may be observed at Pin 7 of the XR2206 function generator (ICU3).

2) If no output is observed, check on chip voltages and grounds. If the IC is replaced, verify proper adjustment by performing the subcarrier adjustment procedure described previously.

3) Note the modem card must be properly adjusted and working correctly for the subcarrier board to function. Refer to the modem section of this manual for troubleshooting details.

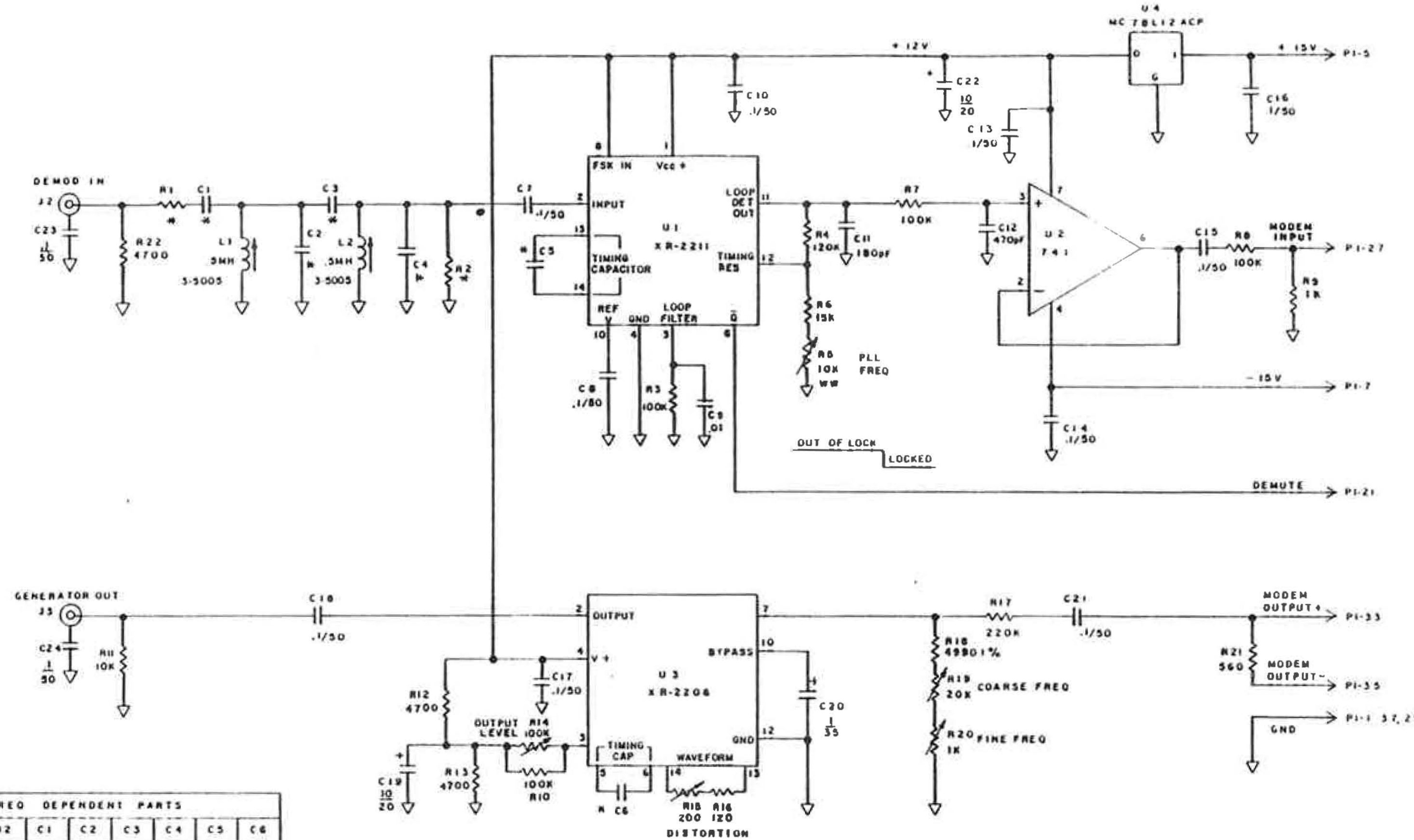
c. Subcarrier Demodulator

1) Using an oscilloscope, observe the extraction filter output at IC U1, Pin 2. This signal should appear much like the subcarrier generator output. If it is distorted, check input filter for proper tuning or defective components.

2) Check demodulator frequency as described in adjustment section.

3) Check operation of 741 Buffer Amp.

4) Check operation of modem board. Refer to modem section of manual.



✱ FREQ DEPENDENT PARTS								
	R1	R2	C1	C2	C3	C4	C5	C6
20KHZ	470	1500	.0131	.111	.0175	.111	2530pF	2530pF
26KHZ	470	1800	.008	.068	.01	.068	1930pF	1930pF
39KHZ	820	2700	3600pF	.031	4700pF	.031	1300pF	1300pF
67KHZ	1500	4700	1200pF	.01	.0016	.01	750pF	750pF
110KHZ	2200	6800	470pF	3600pF	620pF	3600pF	470pF	560pF
200KHZ	3900	15K	130pF	1110pF	180pF	1110pF	270pF	470pF

NOTES

1. UNLESS OTHERWISE SPECIFIED
   RESISTOR VALUES ARE IN OHMS 1/4W 10%
   CAPACITOR VALUES ARE IN MICROFARADS
2. P C BOARD 5185858
3. COMPONENT LAYOUT 2082719

FIRST USED ON MRC-1

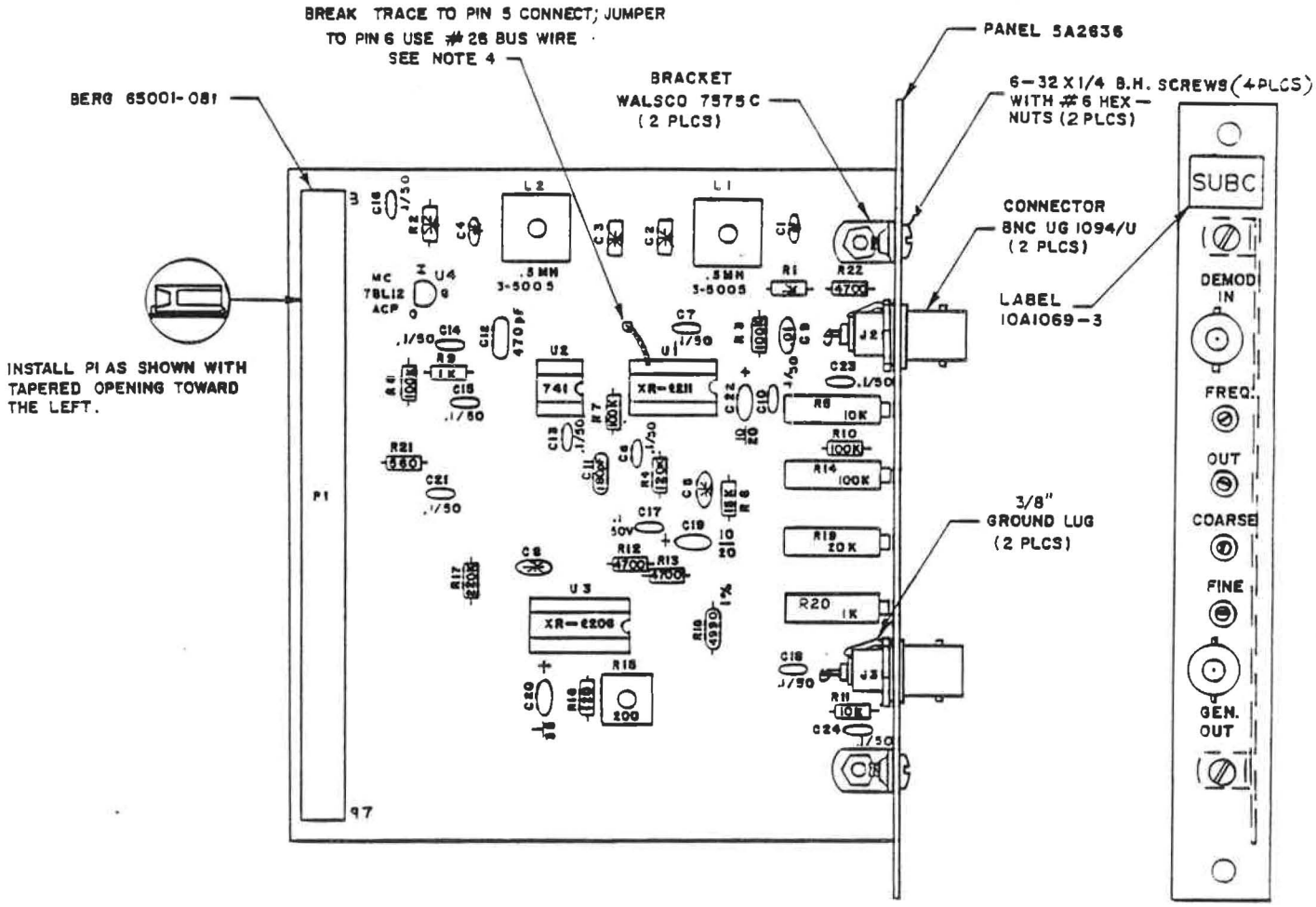
MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA

SCHEMATIC
SUBCARRIER INTERFACE

SCALE: NONE

91C7156 B1

9 1C7156 B1



FREQ. DEPENDENT PARTS *										
	INPUT								OUTPUT	
ITEM		R1	R2	C1	C2	C3	C4	C5	C6	ITEM
1	20 KHz	470	1500	.0131	.111	.0175	.111	2530 pf	2530pf	A
2	26 KHz	470	1800	.008	.068	.01	.068	1930pf	1930pf	B
3	39 KHz	820	2700	3600pf	.031	4700pf	.031pf	1300pf	1300pf	C
4	67 KHz	1500	4700	1200pf	.01	.0016	.01	750pf	750pf	D
5	110KHz	2200	6800	470pf	3600pf	620pf	3600pf	470pf	560pf	E
6	200KHz	3900	15 K	130pf	1110pf	180pf	1110pf	270pf	470pf	F

FIRST USED ON MRC-1

REVISIONS	DATE	MGMT. APPR.
E1 CORRECT FREQ CHART ECO 3016 15 MAY 81 AJB		
D1 ADD "INPUT" TO TABLE "OUTPUT" ITEM ECO 1713 WR6 28 MAY 80		
C1 CHG. J1-21 TO U1 PIN 4 NOTES 5 & 9 ECO 1720 ADD LABEL 10A1069-3 ECO 1690 WR6 25 APR 80		
B1 ADDED BIT INFORMATION PER ECO 1567 B.W.F.	1 FEB 80	
B0 BERG 65001-081 WAS 65001-085 ARI WORST KEY 02 ECO 1582 12 SEP 79 DFH		
A RELEASED FOR PRODUCTION	4 MAY 79	A.J.B.

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA 93017

COMPONENT LAYOUT
SUBCARRIER INTERFACE

TOL: FRACT. = 1/32. XX = .030. XXX = .010. ∠ = 1/2°
DWN A. J. B. 23 APR 79 SCALE: FULL
CHK
ENG 15 MAY 79

2082719 E1

ANALOG II INPUT BOARD

Schematic 91D7238
Assembly 20D2794
PC Board 51C5910

I. PURPOSE

This board is used to measure 16 differential analog inputs and convert these input voltages to digital signals suitable for use by the central microprocessor.

II. SPECIFICATIONS

DC input resistance is 500kΩ. However, it is recommended that the output impedance of the circuit driving the card not exceed 10kΩ at .25 Hz, increasing to 25kΩ at 4 Hz. Normal mode rejection at 60 Hz is 35 dB with a common mode rejection (within input voltage range) of at least 60 dB. For best overall accuracy, the normal mode input should be close to +3V, with maximum inputs not exceeding ±5V.

Measurement accuracy is 0.1% ±1 bit. The maximum input voltage from either input to ground is ±5V. Exceeding this voltage will cause improper operation of the board for the duration of the over-voltage condition. If either input voltage exceeds ±40V, permanent damage to the A/D IC may result.

III. ELECTRICAL ADJUSTMENTS

Board addressing is accomplished using BCD switch S1.

Up to 16 different A/D channels per board can be accessed, with the lowest 16 data channels on Board Ø, the next 16 data channels on Board 1, and so on. Switch programming positions are shown in Section 7.3. S1 is normally programmed at the factory and will not normally require changing. If a defective board is replaced, be sure that the address switches are set to the proper position.

Two A/D conversion rates may be selected using a jumper near IC U6. Normally a trace exits (on the backside of the board) between Point C and Point F causing a conversion time of 15 ms. Increased 60 Hz rejection can be obtained by cutting the trace between C and F and installing a jumper between Points C and S. This will double the conversion time and reduce the update time by half. A 30 ms rate will sample the input for almost an entire power line cycle, allowing most of the 60 Hz signal to average out.

IV. THEORY OF OPERATION

The A/D board is selected by the microprocessor when pin 22 of the MC6821 PIA (IC U2) is pulled to a high state. Switch S1 and a 74LS86 exclusive or gate (IC U11) form a programmable inverter for board address selection. The 74LS30 NAND gate (IC U12) determines the ultimate address location by NAND'ing the outputs of IC U11 with PRE (I/O Select), and address lines A6, *A7, and A8. The A/D board requires four (4) adjacent address locations in the range from 8140 to 817F, with the exact address location programmed by swith S1.

When the address lines match the address programmed by S1, pin 8 of IC U12 will go to a low state. Part of IC U14 is

used to invert the output of U12 to form an active high board select signal which is fed to the chip select on IC U2 and the bus buffer selector IC U10. When the CPU requests data from the A/D PIA, the read/write line will go high, causing pin 11 of IC U10 to go low, enabling the bus drivers in the read data direction. When the CPU writes data to the A/D PIA, the read/write line will be low making pin 8 of IC U10 low, enabling the bus drivers in the write direction.

PIA lines PAØ through PA7 are used to read in the eight least significant digits of the A/D output. The four most significant bits plus an over-range bit are read in on PBØ through PB4. These same lines double as outputs to select 1 of 20 analog inputs. PBØ and PB1 select 1 of 4 multiplexer inputs, while bits PB2 through PB4 select 1 of 5 multiplexers using a 74LS138 decimal decoder (IC U13).

The ADB 1200 (IC U3) is the digital controller for the LF 13300 analog building block (IC U4). Together, they form an integrating 12-bit A/D converter. The ABD1200 provides the control signals plus autozeroing, polarity indication, over-range indication, and continuous conversion capability. The ADB 1200 supplies 4 control signals to the LF13300 and requires one from the LF13300.

The conversion cycle is divided into five distinct cycles. They are:

Phase I - Offset Correction
Phase II - Polarity Detect
Phase III - Initialization
Phase IV - Ramp Unknown
Phase V - Ramp Reference

A timing diagram illustrating these phases is shown in Fig. 1. When the conversion jumper is connected from C to F, the clock period (1/f) is 2 μs. When the jumper is connected from C to S, the clock period is 4 μs.

Phase I - Offset Correction (256 Clock Periods)

This phase is initiated by taking the Start Conversion (SC) and the Output Enable (*OE) lines high. At this time, Offset Correct (OC) will be Logic 1. The LF13000 requires this phase to correct any intrinsic offset voltage errors prior to the polarity detect phase.

PHASE II - Polarity Detect (256 Clock Periods)

This phase is used to determine the polarity of the analog input. At the midpoint of this phase, COMP from the LF13300 is examined for polarity. If COMP is high, the input voltage is positive. If COMP is low, the input voltage is negative. The Polarity Detect signal (PD/RU+) will be high during this entire phase. The above operation is also necessary to determine which integrator input (positive or negative) of the LF13300 should be used for proper A/D conversion.

PHASE III - Initialization (256 Clock Periods)

This phase is identical to Phase I and is used by the LF13300 to eliminate any offsets induced as a result of the polarity detect phase. Offset Correct (OC) will be high during this phase.

Phase IV - Ramp Unknown (4096 Clock Periods)

The unknown input voltage is integrated for a fixed time,

4096 clock periods, during this phase. The result of the Phase II Polarity Detect cycle determines whether PD/RU+ or RU- will be high. If Phase II indicates a positive input, the PD/RY+ signal will be high. If Phase II indicated a negative input, Ramp Negative (RU-) will be high. These two signals will never be high simultaneously.

Phase IV - Ramp Reference

This phase is a variable length phase depending on the magnitude of the analog input voltage. During this time, Ramp Reference (RR) will be high. When COMP goes low, or when the internal counter reaches 100% of full scale (8192 clock periods), the Ramp Reference (RR) signal goes to the low state, the counter output is loaded into the output register, and the End of Conversion (EOC) signal goes high. The polarity bit will reflect whatever value was determined during Phase II. The output register will hold the data until a new conversion is completed and new data is loaded into the register. The Output Enable (*OE) line must be low and SC must be high to enable the outputs.

The differential amplifier consisting of the LM 308A (IC U9), TL072 (IC U15), and associated components converts the input samples to a single-ended signal suitable for the A/D converter. The gain of the amplifier is fixed at 2.00 by resistors R7, 8, 14, and 15.

An LM329BZ precision reference (IC U8) provides 6.95V to the A/D converter.

Five MC14052 four-channel differential analog multiplexers (U1 through U5) are used to select 1 of 20 analog input channels. Only 16 input channels are available externally to the user; the remaining 4 channels are used for automatic compensation to maintain long-term accuracy. Input Channel 17 is referenced to ground and is used to measure the offset voltage of the amplifier and A/D converter. Input Channels 18 and 19 monitor the voltage generated by U8. Channel 20 monitors the +5V supply.

V. TROUBLESHOOTING

A. Verify that the A/D board and the interface card are plugged into the corresponding slots.

B. Verify proper switch position by checking the board address strobe.

C. Check power supply voltages on this card.

D. Using the technical description and Fig. 1, observe the waveforms of the LF13300 digital portion of the A/D converter.

E. Check analog switch addressing. Under normal operations, the system will be scanning all 20 channels.

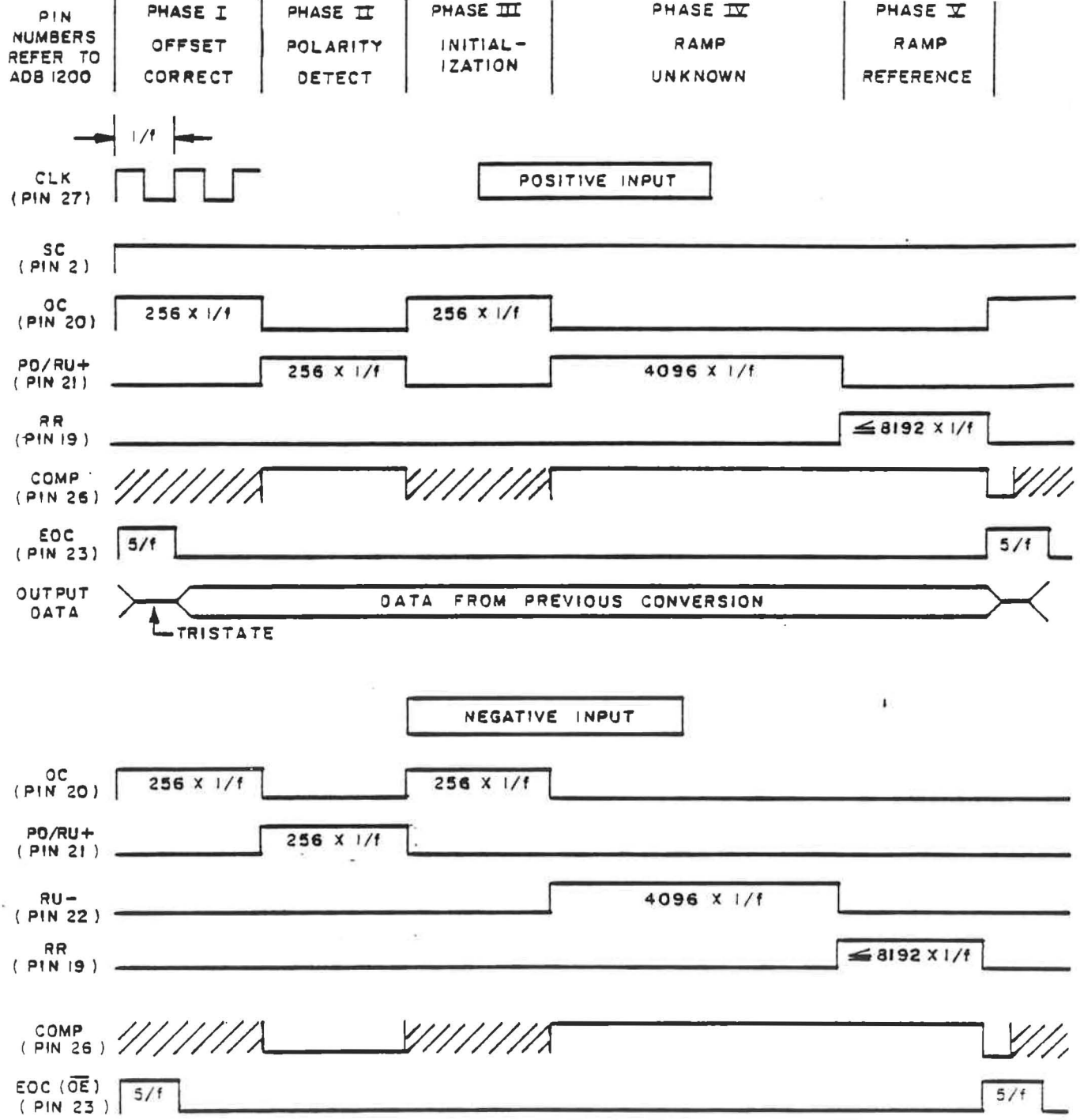
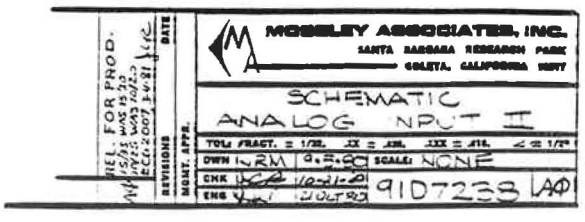
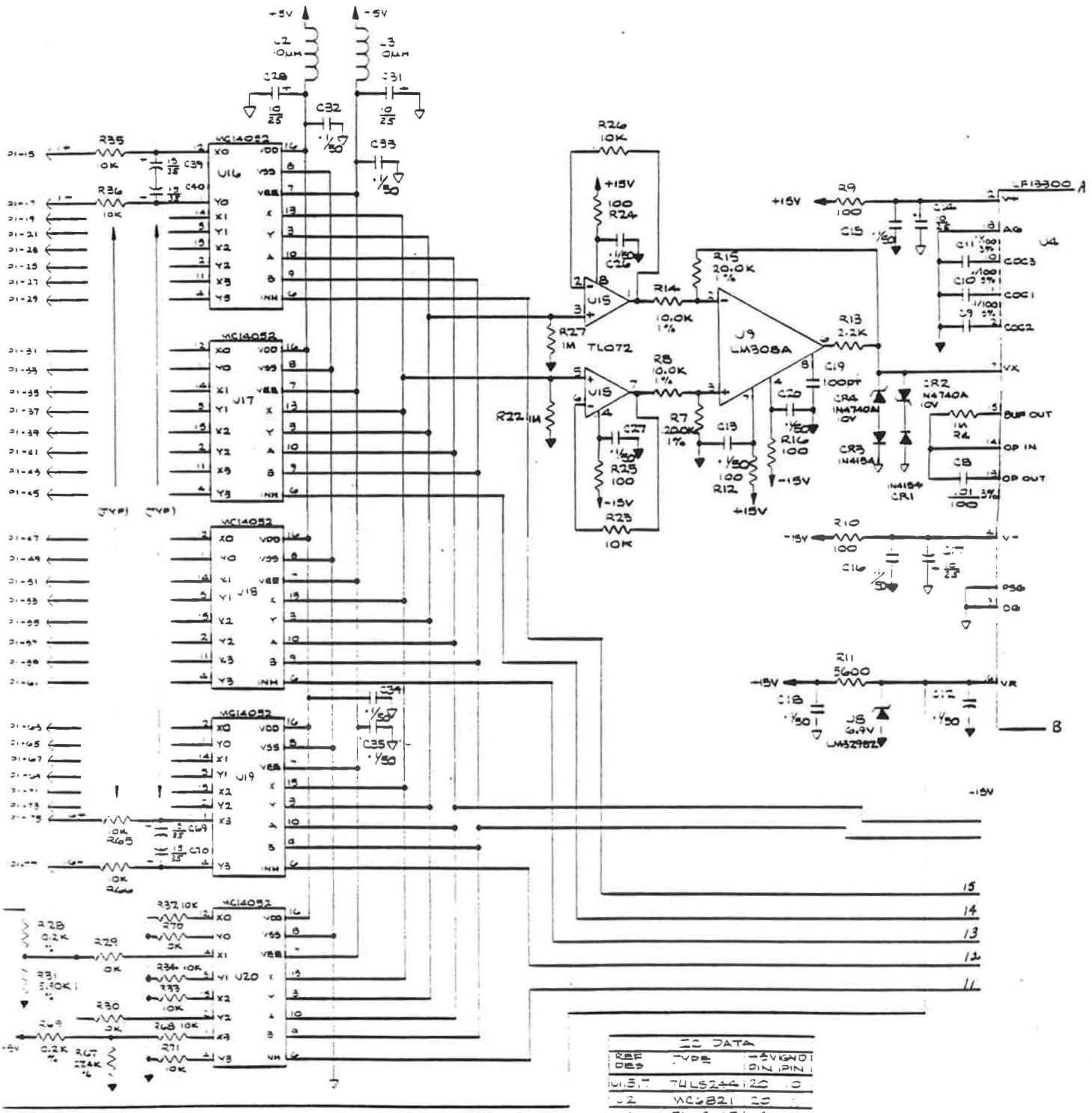


FIGURE 1
ADB1200-LF13300 TIMING DIAGRAM

USED ON: MRC FAMILY

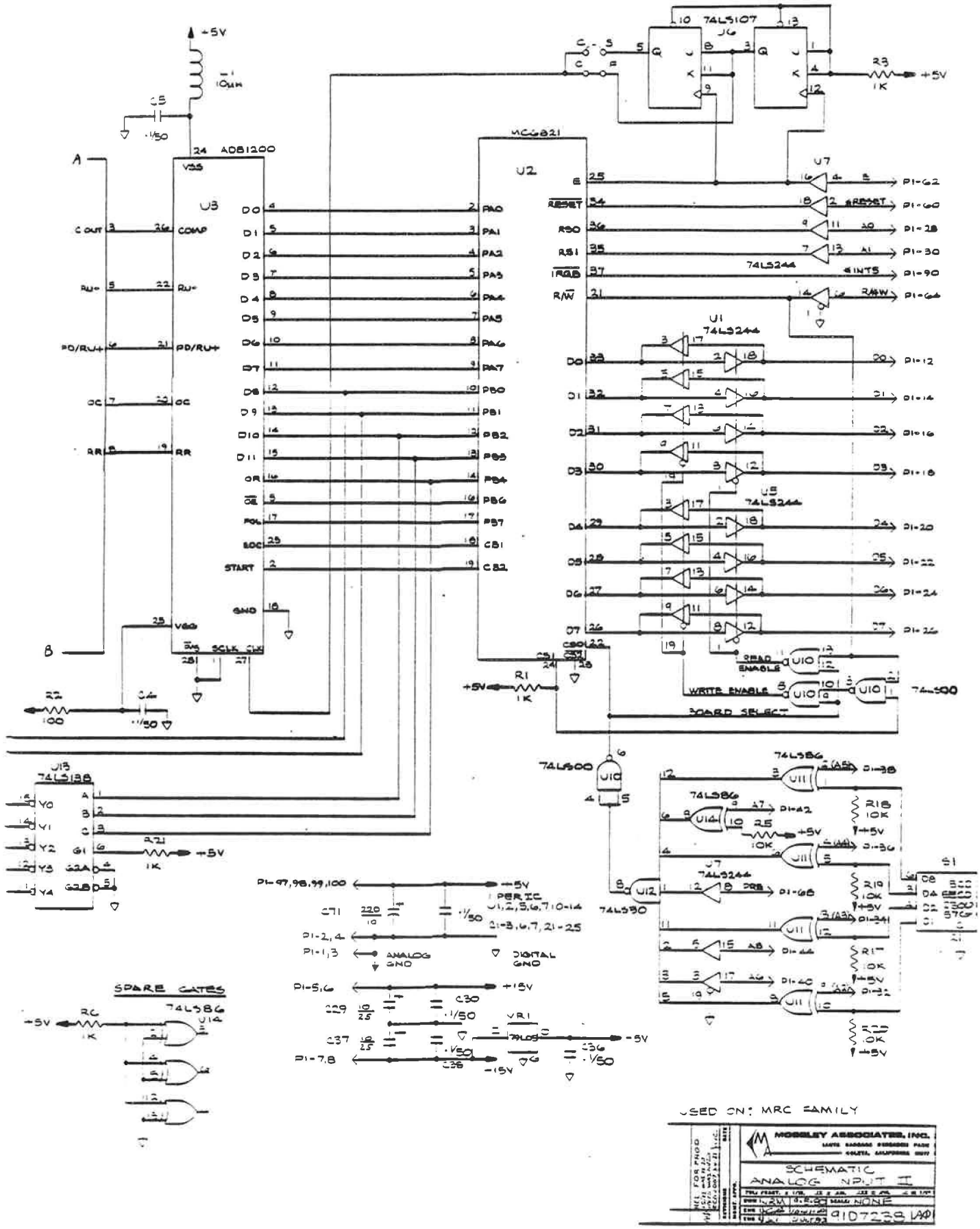


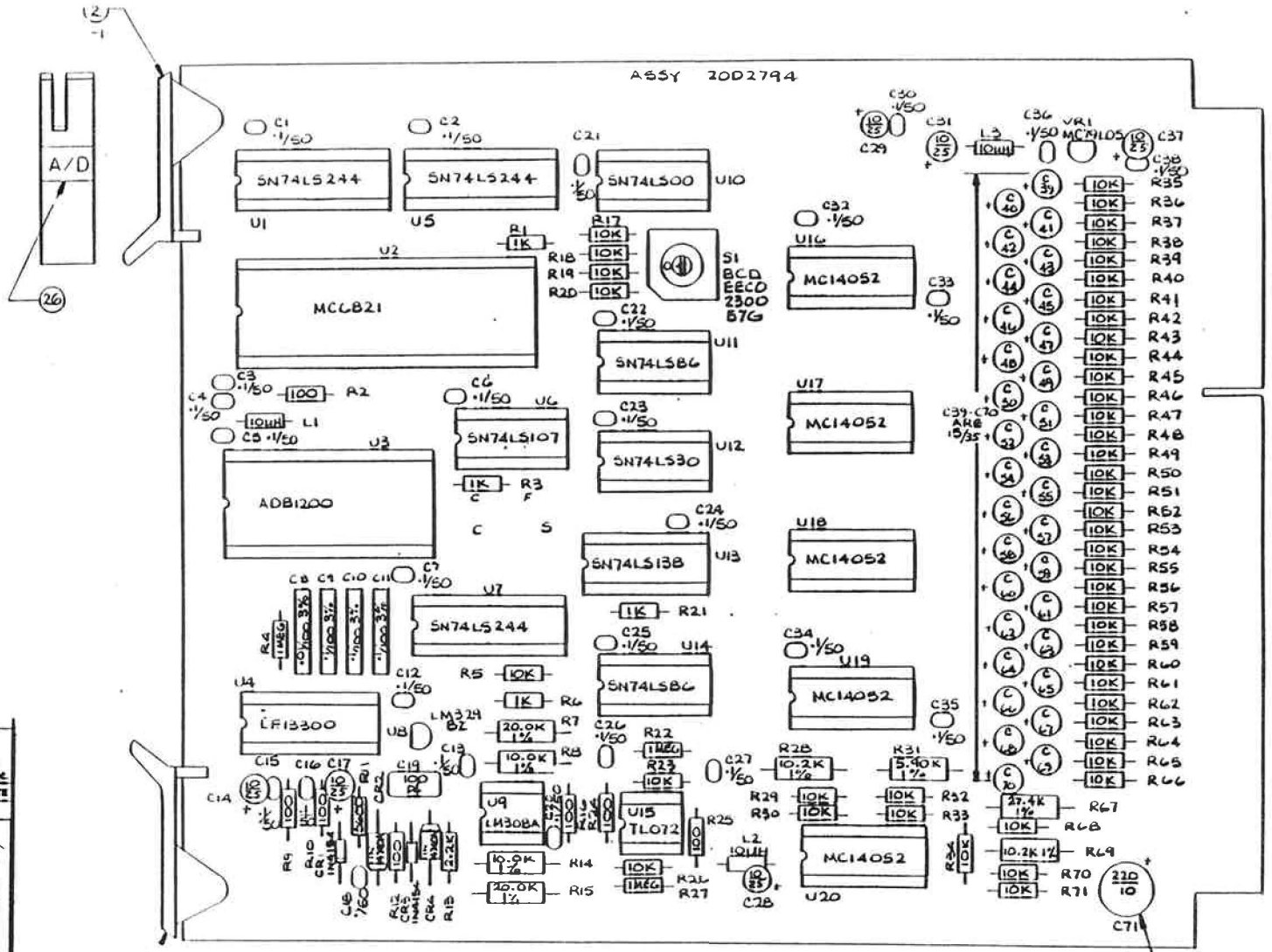


I/O DATA			
REF DES	TYPE	+5V PIN	GND PIN
U1,3,7	74LS244	20	10
U2	MC6821	35	
U6	74LS107	4	11
U10	74LS00	4	11
U11,12	74LS86	4	11
U13	74LS30	4	11
U14	74LS138	16	8

NOTES:

1. UNLESS OTHERWISE SPECIFIED
   RESISTOR VALUES ARE IN OHMS, 1/4W, 10%
   CAPACITOR VALUES ARE IN MICROFARADS.
2. P.C. BOARD 51C5910. REV. -11, -21.
3. COMPONENT LAYOUT 2002794. REV. A0
4. BASE ADDRESS = $814Ø
   DATA REGISTER A = BASE + BCD +Ø
   CONTROL REGISTER B = BASE + BCD +1
   DATA REGISTER B = BASE + BCD +2
   CONTROL REGISTER B = BASE + BCD +3


+5V
L1
10uH
C5
.1/50
24 ADB1200
VSS
U3
A
B
DO
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
OR
OE
POL
EOC
START
GND
VDD
COUT
COMP
RU+
PD/RU+
OC
RR
SCLK
DIN
22
100
C4
.1/50
MC6821
U2
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
CB1
CB2
E
RESET
R/S0
R/S1
R/WB
R/W
CS0
CS1
CS2
R1
1K
74LS107
U6
R3
1K
U7
74LS244
P1-62
P1-60
P1-28
P1-30
P1-90
P1-64
INTS
U1
74LS244
U5
74LS244
D0
D1
D2
D3
D4
D5
D6
D7
P1-12
P1-14
P1-16
P1-18
P1-20
P1-22
P1-24
P1-26
READ ENABLE
WRITE ENABLE
BOARD SELECT
74LS00
U10
74LS86
U11
U14
R18
10K
R19
10K
R17
10K
R20
10K
+5V
P1-38
P1-42
P1-36
P1-66
P1-44
P1-40
P1-34
U7
74LS244
U12
74LS30
U13
74LS138
Y0
Y1
Y2
Y3
Y4
G1
G2A
G2B
A
B
C
R21
1K
P1-97,98,99,100
PERIC
U1,2,5,6,7,10-14
21-23,6,7,21-25
C71
220/10
.1/50
P1-2,4
P1-1,3
ANALOG GND
DIGITAL GND
P1-5,6
+15V
C29
10/25
.1/50
C30
C37
10/25
.1/50
C36
.1/50
-15V
P1-7,8
VR1
ANALOG
-5V
SPARE GATES
74LS86
U14
R6
1K
S1
USED ON: MRC FAMILY
MOSELEY ASSOCIATES, INC.
SCHEMATIC
ANALOG INPUT II
SIZE A
NONE
9107239 LAD



REL FOR PROD. 10/25 WAS 10/30 15/39 WAS 15/30 ECO 2007 2-4-81

REVISIONS	DATE
MGMT. APPR.	

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA 93017

COMPONENT LAYOUT
ANALOG INPUT II

TOLL FRACT. ± 1/32 | .XX ± .01 | .XXX ± .005 | ∠ ± 1/2°

DWN | CHK | ENG | MFG | QA

SCALE: NONE

20D2794 | A0

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 10%;
   ALL CAPACITOR VALUES ARE IN MICROFARADS.
2. PC. BOARD 51C5910 REV-11, -21.
3. SCHEMATIC 91D7238 REV. A0
4. I.C. SOCKETS INSTALLED AT EACH I.C. POSITION.
5. S1, U8 AND VR1 INSTALLED WITHOUT SOCKETS.

QTY	DESCRIPTION	REF DES	STOCK NO.	ITEM NO
1	VOLTAGE REG - 5V MOTOROLA MC7905	VR1	3650132	51
2	DIODE GE IN4154 SMALL SIGNAL	CR1,3	3600145	50
2	DIODE SCHAUR IN4740A ZENER	CR2,4	3600202	49
3	INDUCTOR MILLER 9230-44 10UH	L1-3	4020244	48
				47
1	CAPACITOR ARCO OMS-10U 100P6 MICA DIP	C19	4200069	46
3	" SEI 22UB104H 1/100 3% POLY. CAP	C9,10,11	4250486	45
1	" SEI 22UB103H .01/100 3% POLY CAP	C8	4250171	44
32	" SPRAGUE 196D156X9035PB4 15/35 EPOXY DIP	C39-70	4280087	43
1	" KEMET K220E10 220/10 EPOXY DIP	C71	4280186	42
6	" SPRAGUE 196D106X0025KA1T 10/25 EPOXY DIP	C14,17,28,29, 31,37	4280079	41
27	" CAL CY220C104M 1/50 CERAMIC	C1-7,12,13,15,16,18 20-27,30,32-36,38	4310207	40
				39
1	RESISTOR KEPCO RNC0 D27432F 27.4K METAL FILM 1/4W 1%	R67	4520227	38
2	" " D20025F 20.0K 1/4W 1%	R7,15	4520219	37
2	" " D10225F 10.2K 1/4W 1%	R28,69	4520201	36
2	" " D10025F 10.0K 1/4W 1%	R8,14	4520094	35
1	" " D5901F 5.90K 1/4W 1%	R31	4520193	34
3	" ALLEN BRADLEY 1 MEG 1/4W 10% CARB	R4,22,27	4410601	33
1	" " 2.2K " " "	R13	4410288	32
47	" " 10K " " "	R5,17-20,23,24,26, 29,30,32-44,46,3211	4410379	31
4	" " 1K " " "	R1,3,6,21	4410247	30
1	" " 5600Ω " " "	R11	4410346	29
7	" " 100Ω " " "	R9,9,10,12,16, 24,25	4410122	28
				27
1	LABEL A/D MAI 10A1068-10		3430378	26
2	SOCKET, IC 8 PIN AMP 640463-1	U9,15	3250016	25
5	" " 14 PIN AMP 640357-1	U6,10,11,12,14	3250024	24
6	" " 16 PIN AMP 640558-1	U13,U16-U20	3250032	23
1	" " 18 PIN AMP 640559-1	U4	3250040	22
3	" " 20 PIN AMP 640464-1	U1,5,7	3250057	21
1	" " 28 PIN AMP 640362-1	U3	3250081	20
1	" " 40 PIN AMP 640579-1	U2	3250099	19
				18
1	DIP SWITCH BCD EECD2300576	S1 YEL	3150117	17
				16
5	IC MOTOROLA ANALOG MULTIPLEXER MC14052	U16-U20	3680220	15
1	" T.I. DUAL OP-AMP TL072	U15	3730876	14
1	" T.I. 1 OF 8 DECODER SN74LS138	U13	3660742	13
1	" T.I. 8-INPUT NAND SN74LS30	U12	3660735	12
2	" T.I. QUAD X OR SN74LS86	U11,U14	3660743	11
1	" T.I. QUAD NAND SN74LS00	U10	3660669	10
1	" NAT. OP-AMP LM-308A	U9	3730157	9
1	" NAT. RGLTR 6.9V LM329BZ	U8	3650066	8
1	" T.I. DUAL J-K F.F SN74LS107	U6	3660750	7
1	" NAT. A/D LF13300	U4	3730132	6
1	" NAT. CONTROLLER ADB1200	U3	3730595	5
1	" MOT. PIA MC6821	U2	3710027	4
3	" T.I. QUAD BUS TRANSCEIVER SN74LS244	U1,5,7	3660859	3
1	EJECTOR PINS VERO S12409/1 S12409/2		1250075	2
1	PC BOARD ANALOG INPUT II	SIC5910 REV-10,-20	3472438	1

REL FOR PROD.

MOSELEY ASSOCIATES, INC.

COMPONENT LAYOUT

ANALOG INPUT II

SIZE: D | DWG NO: 20D2794 | REV: AD

STATUS INPUT, TTL II

Schematic 91C7237
Assembly 20D2798
PC Board 51C5912

I. PURPOSE

This unit is used to interface the remote control system with 16 TTL inputs. The inputs can be used separately as status or as a single 16-bit word.

II. SPECIFICATIONS

Inputs are TTL active low. Input voltage should be restricted from Ø to +5 volts, or board damage may result.

III. BOARD ADDRESS SPECIFICATION

Switch S1 is used to assign a board address from Ø to 15. Board Ø will output Channels 1 through 16; Board 1 will output Channels 16 through 32, etc. Programming of S1 is shown in Fig. 1. If replacement boards are installed for any reason, be sure the board is switched correctly.

IV. THEORY OF OPERATION

IC U6, in conjunction with swith S1, is a programmable inverter for address selection. IC U5 ANDS the outputs of U6 with PRE (I/O Select), A6, A7 and *A8 to form the board address. When switch S1 is set to "0", the board is addressed in its lowest address range 8ØCØ to 8ØC3.

When switch S1 is set to "F", the board is addressed from 8ØFC to 8ØFF.

When the correct address is decoded, pin 8 of IC U5 goes to a low state, enabling decoder IC U4. U1 and U2 are tri-state buffers used to gate 8 bits of status information onto the data bus. U3 provides a unique board ID pattern on the data bus when selected.

When address line AØ and A1 are both low and IC U4 is enabled, status bits 1 through 8 are gated onto the data bus. When AØ is high and A1 is low, status bits 9 through 16 are gated onto the bus. When AØ is low and A1 is high, the unique board ID is gated onto the bus.

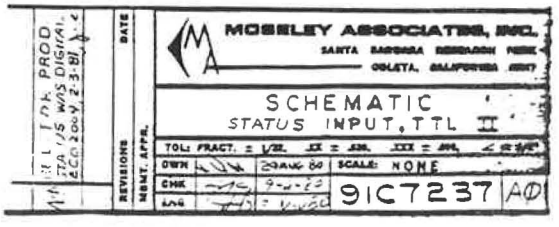
V. TROUBLESHOOTING

Check for periodic low pulses on IC U5 pin 8, indicating the CPU is attempting to read data from this card. Low-going pulses should also be observed on pins 1 and 19 of IC's U1 and U2. Upon power-up of the unit, at least one status input should be low or the CPU will not recognize the existence of the board (MRC-1 only).

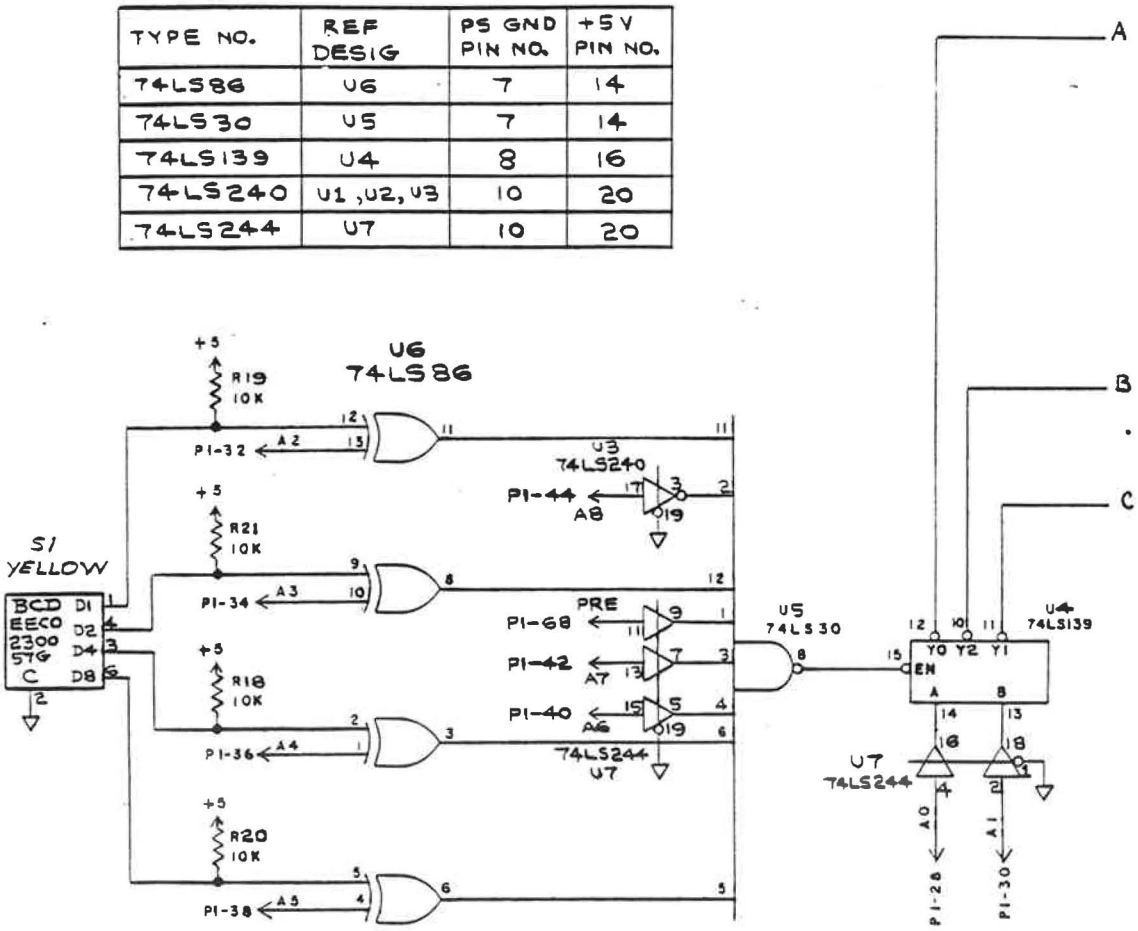
Address	Channels
0	1-16
1	17-32
2	33-48
3	49-64
4	65-80
5	81-96
6	97-112
7	113-128
8	129-144
9	145-160
A	161-176
B	177-192
C	193-208
D	209-224
E	225-240
F	241-256

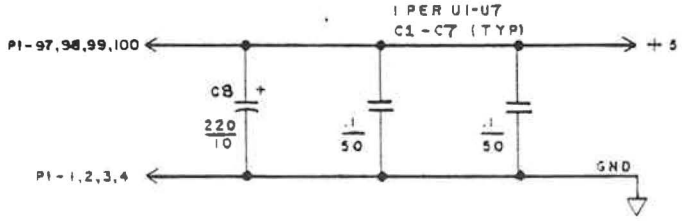
FIGURE 1

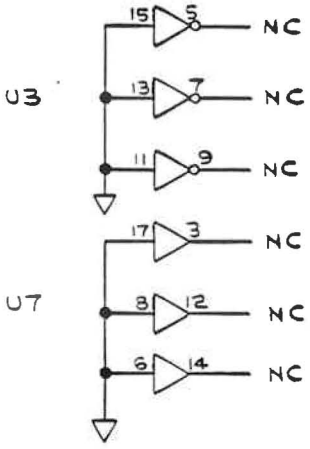
S1 PROGRAMMING


MOSELEY ASSOCIATES, INC.
SCHEMATIC
STATUS INPUT, TTL II
SCALE: NONE
9IC7237
A0

TYPE NO.	REF DESIG	PS GND PIN NO.	+5V PIN NO.
74LS86	U6	7	14
74LS30	U5	7	14
74LS139	U4	8	16
74LS240	U1, U2, U3	10	20
74LS244	U7	10	20

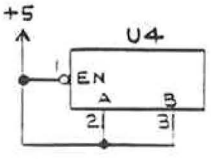




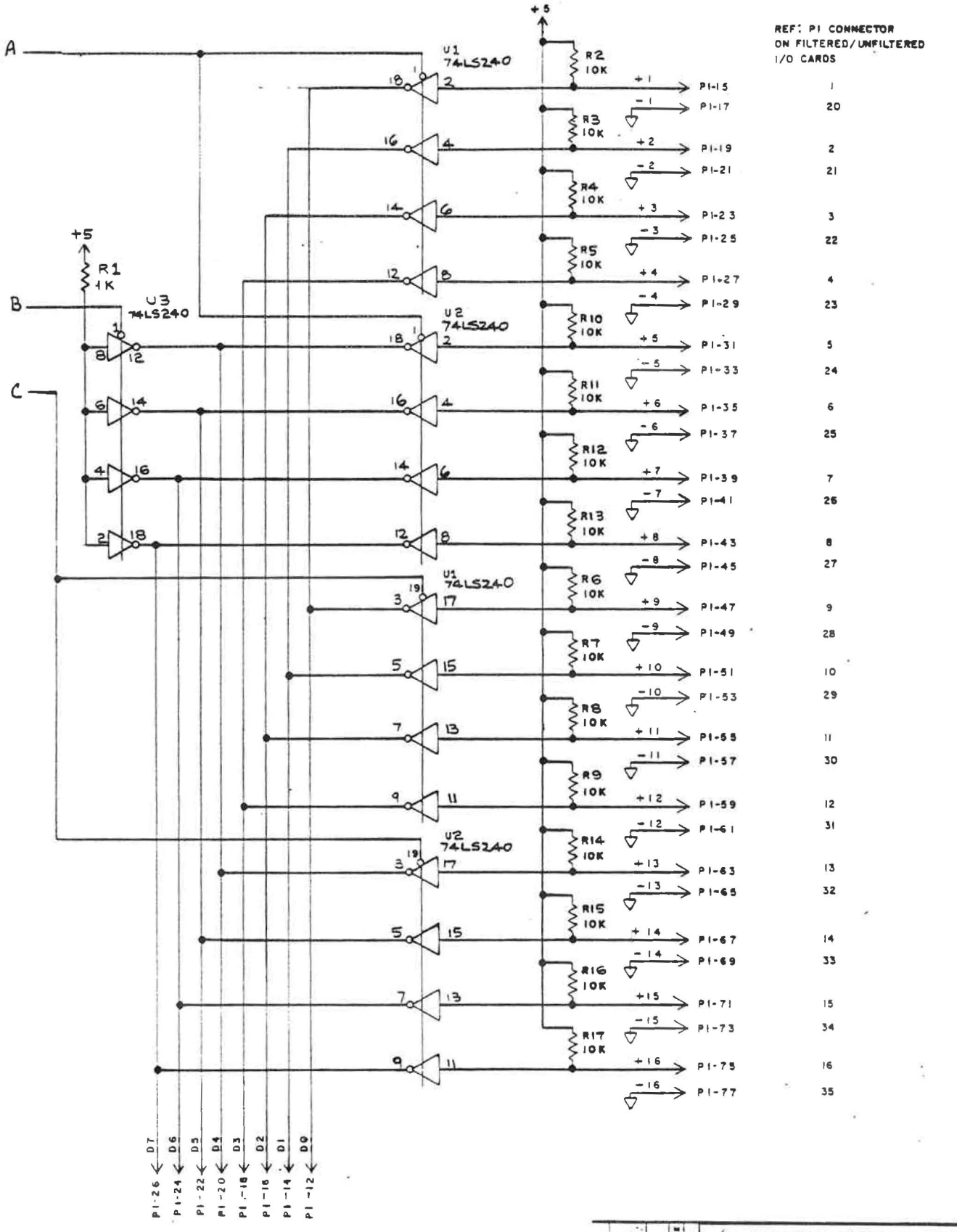


NOTES:

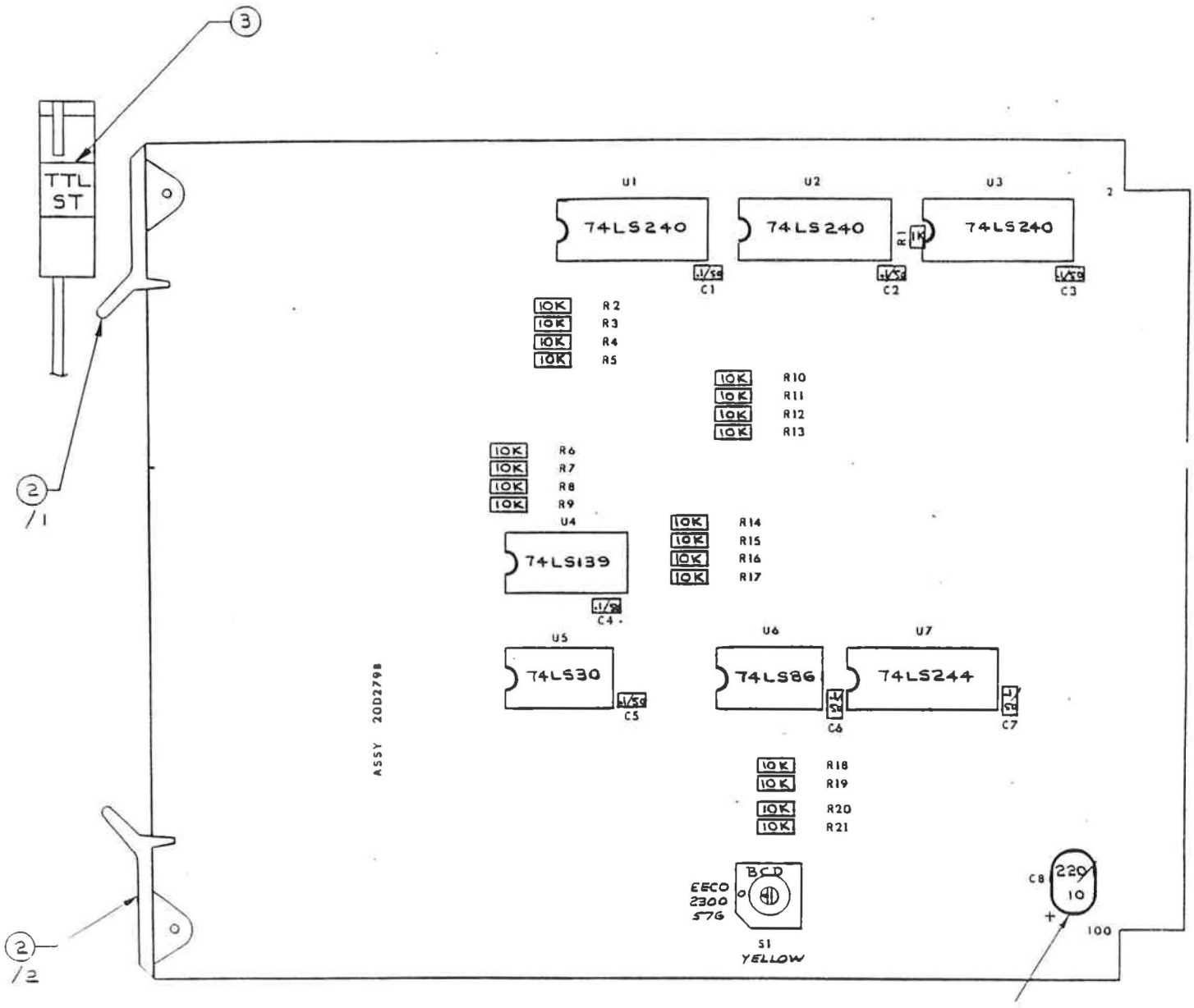
1. UNLESS OTHERWISE SPECIFIED
   RESISTOR VALUES ARE IN OHMS 1/4W 10%
   CAPACITOR VALUES ARE IN MICROFARDS.
2. P C. BOARD 51C5912 REV. -10, -21
3. COMPONENT LAYOUT 2002798 REV. AØ.



Continued on next page



REVISIONS	DATE	MOSELEY ASSOCIATES, INC.	
		SANTA BARBARA RESEARCH PARK	
		GOLETA, CALIFORNIA 93017	
		SCHEMATIC	
		STATUS INPUT, TTL	
		TOL: FRACT. ± 1/32 .XX ± .030 .XXX ± .010 ∠ ± 1/2°	
		DWN	SCALE: NONE
		CHK	91C7237 AD



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   RESISTOR VALUES ARE IN OHMS 1/4W ±5%
   CAPACITOR VALUES ARE IN MICROFARADS
2. I C SOCKETS TO BE INSTALLED AT EACH I C LOCATION
3. SWITCH S1 TO BE INSTALLED WITHOUT A SOCKET
4. P C BOARD 51C5912 REV. -10, -21
5. SCHEMATIC 91C7237 REV.

RELEASED FOR PROD
STATUS MASDIGITAL
EC0209, 2-3-81

REVISIONS	MGMT. APPR.	DATE

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA 93017

COMPONENT LAYOUT—
STATUS INPUT, TTL II

TOL: FRACT ± 1/32, XX ± .030, XXX ± .010, ∠ ± 1/2°

DWN		4 NOV 80
CHK		11-11-80
ENG		4 Nov 81

SCALE:

20D2798 | A

16	CAPACITOR, 220 µf 10V	C8	4280186	1
15	" , .1 µf 50V	C1-C7	4310207	7
14	RESISTOR, 10K 1/4W 10%	R2-R21	4410379	20
13	" , 1K 1/4W 10%	R1	4410247	1
12	SWITCH , BCD, EECO 2300576	S1 YELLOW	3150117	1
11	SOCKET, I.C., 14 PIN	U5, U6	3250024	2
10	" " 16 PIN	U4	3250032	1
9	" " 20 PIN	U1, U2, U3, U7	3250057	4
8	I.C. SN74LS244	U7	3660859	1
7	" SN74LS240	U1, U2, U3	3660974	3
6	" SN74LS139	U4	3660800	1
5	" SN74LS 86	U6	3660743	1
4	" SN 74LS30	U5	3660735	1
3	LABEL , 10A1067-7		3430345	1
2	EJECTOR PAIR, C12409/1,/2		1250075	1
1	P C BOARD 51C5912-10,-21		3472446	1
ITEM NO.	DESCRIPTION	REF DESIG	STOCK NO.	QTY

RELEASED FOR PROD STATUS WAS DIGITAL ECO 2007, 2-3-81 JC

REVISIONS | MGMT. APPR | DATE

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA 93017

COMPONENT LAYOUT-
STATUS INPUT, TTL II

TOL: FRACT. ± 1/32, .XX ± .030, .XXX ± .010, ∠ ± 1/2°

DWN: JH 4 NOV 80 SCALE:
CHK: CJC 11-11-80
ENG: [illegible] 14 Nov 80

20D2798 | AØ

STATUS INPUT, OPTO II

Schematic 91C7236
Assembly 20D2795
PC Board 51C5911

I. PURPOSE

This unit is used to bring 16 on/off inputs into the CPU. It can be used for individual bits (status) or as a 16-bit word. Optical isolators are used for maximum noise rejection.

II. SPECIFICATIONS

The input requires between 5 mA and 30 mA of current (user supplied) to drive the optical isolator. The unit is shipped with 1800 ohm current-limiting resistors. These are suitable for input voltages from 10V to 48V. For lower voltages, the resistors will have to be changed to 560 ohms. This will allow operation from input voltages from 3V to 15V. The maximum voltage from any input to ground should not exceed $\pm$50 VDC. Exceeding this voltage may cause damage to the board.

III. ELECTRICAL ADJUSTMENTS

Switch S1 is used to assign a board address from 0 to 15. Board 0 will output Channels 1 through 16; Board 1 will output Channels 17 through 32, etc. Programming of S1 is given in Fig. 1. S1 is programmed at the factory and will normally only be reset if a defective board is replaced. In this case, the switch on the new board should be set to the same position as the board it is replacing.

IV. THEORY OF OPERATION

IC U1, in conjunction with S1, is used as a programmable inverter for address selection. IC U2 ANDS the output of U1 along with PRE (I/O Select), A6, A7, and *A8 to form the address at which the board will operate.

With switch S1 set to "0", the address for the board will begin at 80C0 and end at 80C3 as each card uses four addresses. If switch S1 is set to "F", the address for the board will begin at 80FC and end at 80FF.

The output of U2 is used to enable 1 of 4 decoder U3, with only the first three outputs being used. The outputs of U3 are active low enables for tri-state buffers U4, U5 and U22.

U4A-D and U5A-E are used to bring the first eight channels onto the data bus, while U4E-H and U5E-H are used to bring the second eight channels onto the data bus. U22 provides a unique board ID pattern on the data bus when selected.

V. TROUBLESHOOTING

As a general guideline, if only certain bits on a card fail to function properly, the cause is usually associated with the input optical isolators. Complete board failure is associated with U1 through U3. If there are multiple boards in the user system, the boards may be interchanged (after setting switch S1) to pinpoint the cause. Before swapping boards, check all inputs to ensure that excessive currents are not being applied.

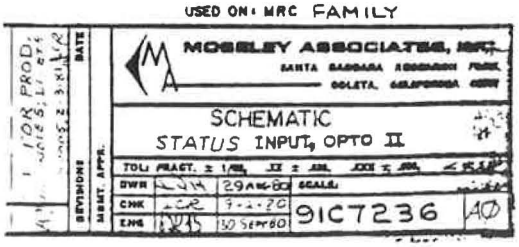
Verify that, when current is passed through the appropriate input, pin 5 of the optical isolator drops below 0.8 volts.

If not, suspect the optical isolator or a defective input on U4 or U5. Check for a periodic low pulse on U2 pin 8. This indicates that the CPU is trying to read data from this card. Low going pulses should also appear on pins 1 and 19 of U4 and U5. If not, suspect U1 through U3 or S1. Note that, upon power up of the unit, at least one of the 16 inputs must be inactive (no current flow) or the CPU will not recognize the existence of the board. (MRC-1 only.)

FIGURE 1
S1 PROGRAMMING

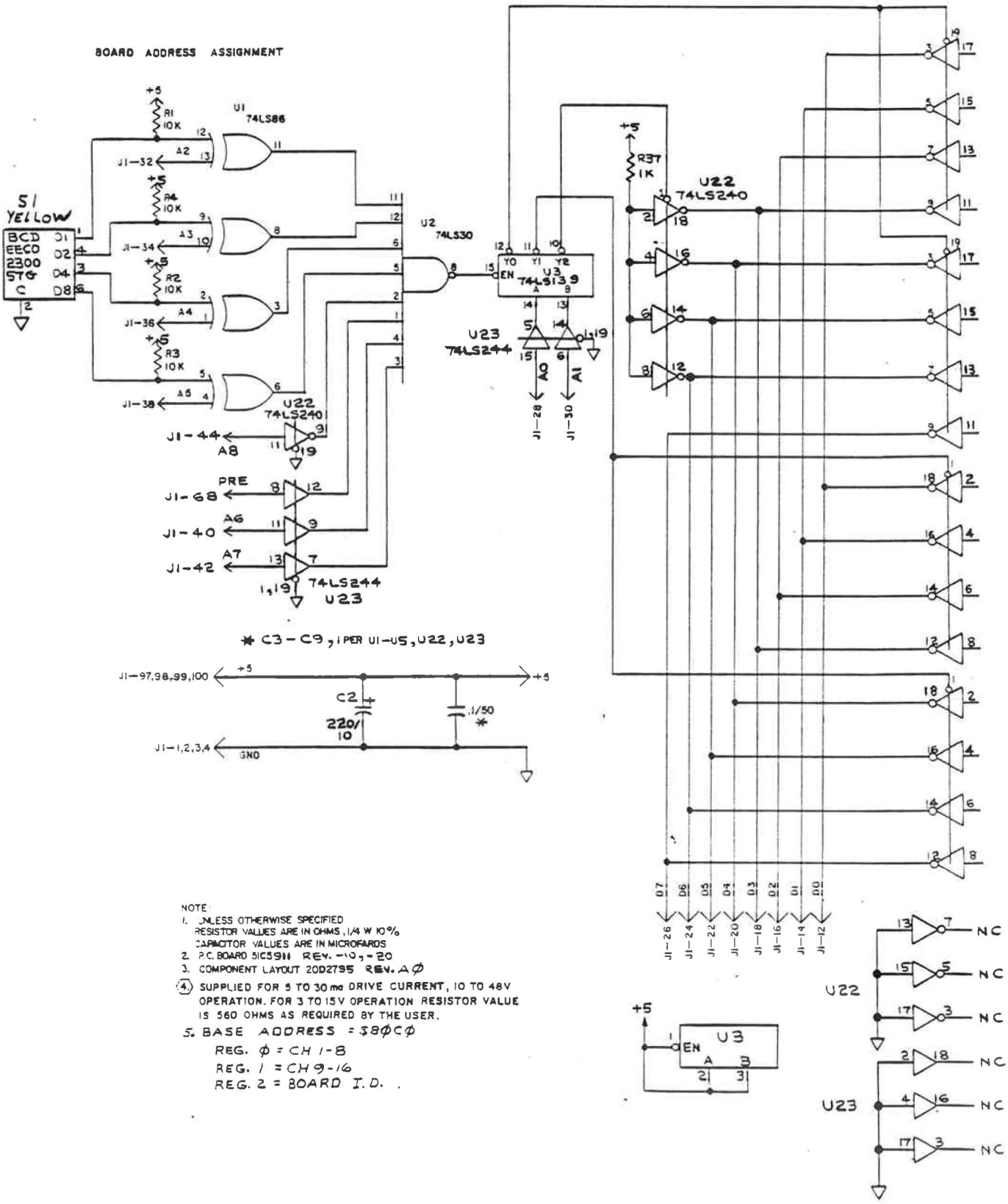
Address	Channels
0	1-16
1	17-32
2	33-48
3	49-64
4	65-80
5	81-96
6	97-112
7	113-128
8	129-144
9	145-160
A	161-176
B	177-192
C	193-208
D	209-224
E	225-240
F	241-256

USED ON: MRC FAMILY



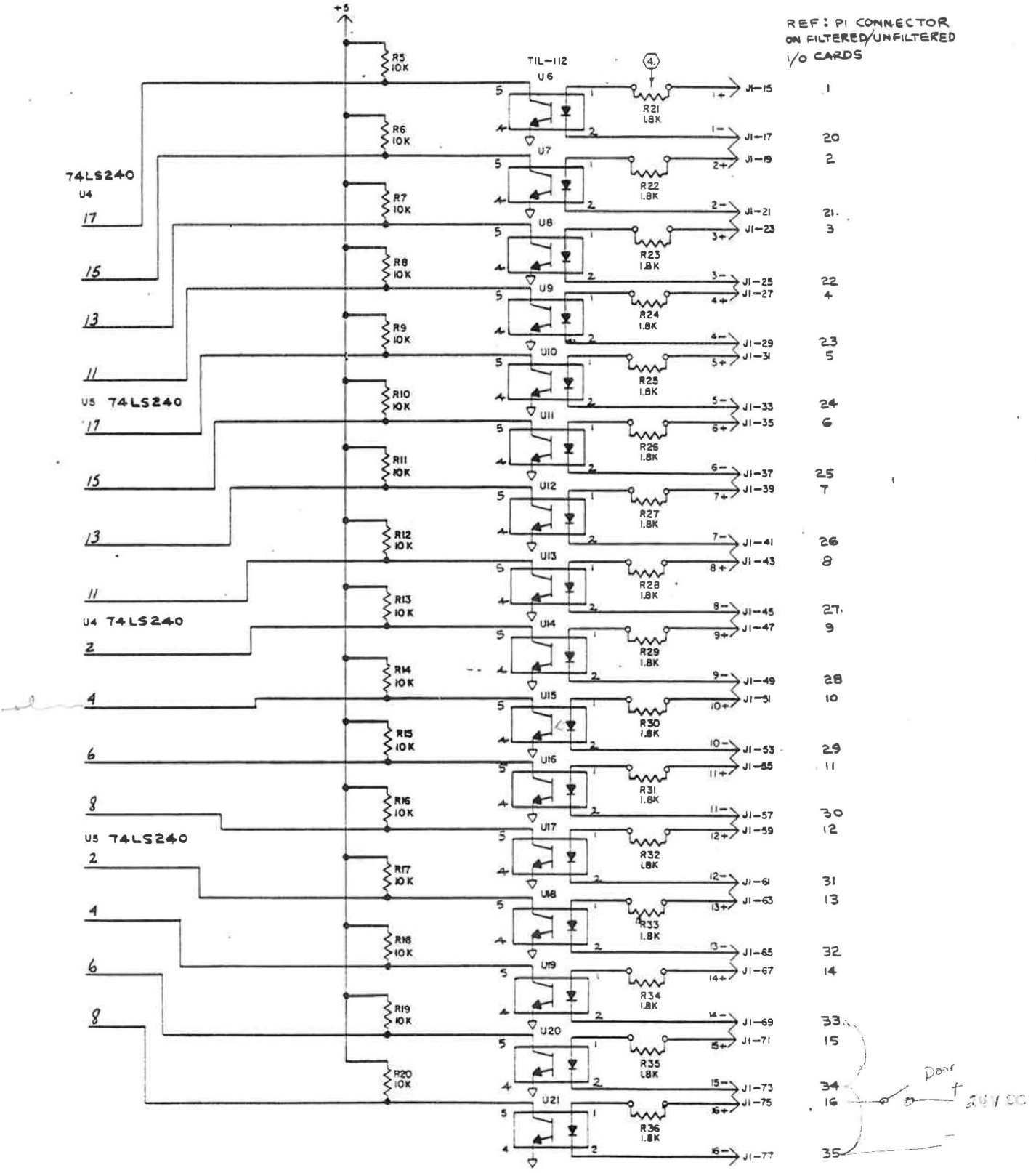
TYPE NO.	REF DESIG	PS GND PIN NO.	+5V PIN NO.
74LS86	U1	7	14
74LS30	U2	7	14
74LS139	U3	8	16
74LS240	U4, U5, U22	10	20
74LS244	U23	10	20
TIL-112	U6 THRU U21	4	

Continued on next page



NOTE

1. UNLESS OTHERWISE SPECIFIED
   RESISTOR VALUES ARE IN OHMS, 1/4 W 10%
   CAPACITOR VALUES ARE IN MICROFARDS
2. P.C. BOARD 51C5911 REV. -10, -20
3. COMPONENT LAYOUT 20D2795 REV. AØ
4. SUPPLIED FOR 5 TO 30 ma DRIVE CURRENT, 10 TO 48V OPERATION. FOR 3 TO 15V OPERATION RESISTOR VALUE IS 560 OHMS AS REQUIRED BY THE USER.
5. BASE ADDRESS = $8ØCØ
   REG. Ø = CH 1-8
   REG. 1 = CH 9-16
   REG. 2 = BOARD I.D.



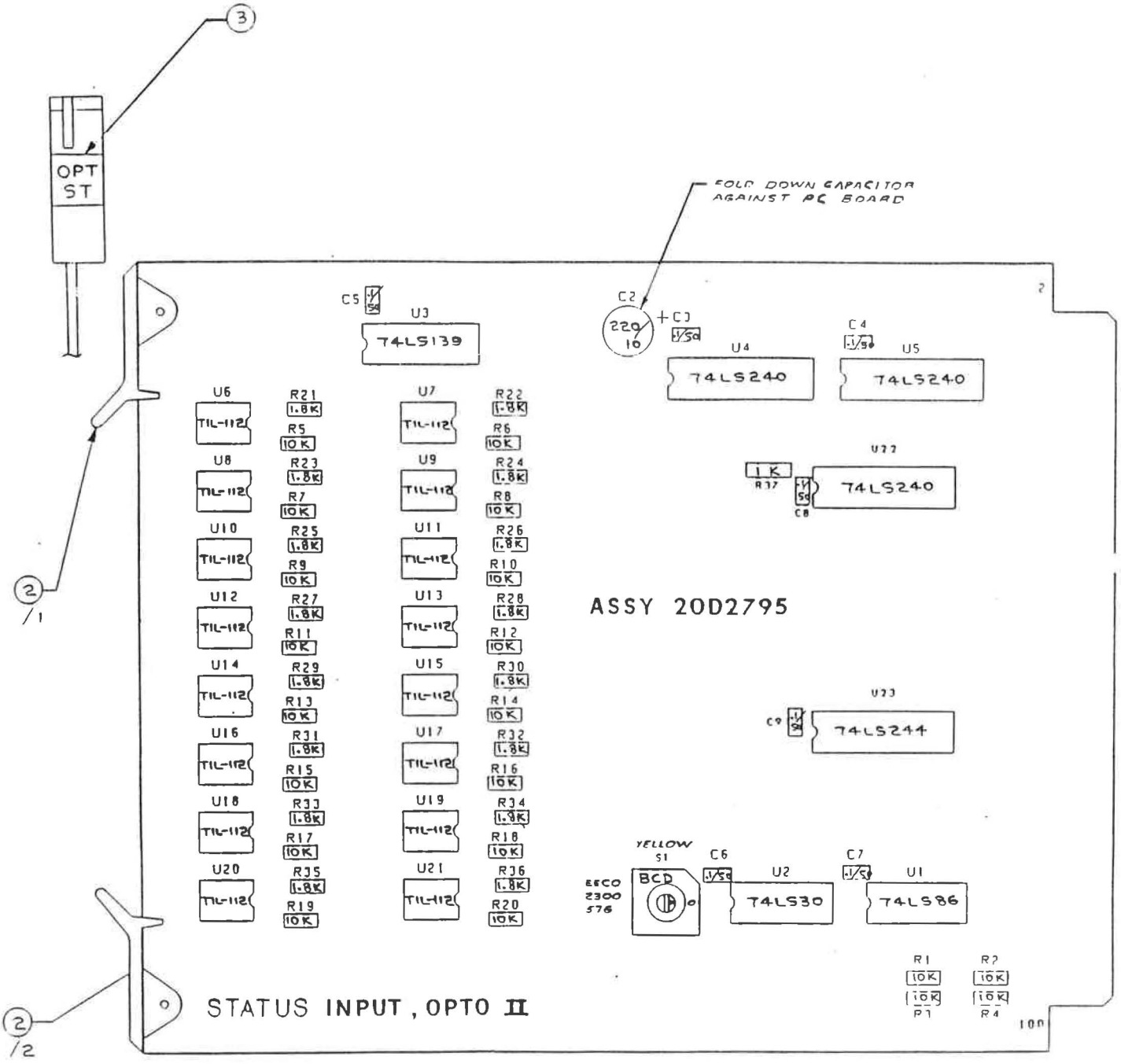
USED ON: MRC FAMILY

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA

SCHEMATIC
STATUS INPUT, OPTO II

DWN		29 AUG 80
CHK		9-2-80
ENG		30 SEP 80

91C7236 40



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   RESISTOR VALUES ARE IN OHMS 1/4W 10%
   CAPACITOR VALUES ARE IN MICROFARADS
2. I.C. SOCKETS TO BE INSTALLED AT EACH I.C. LOCATION
3. SWITCH S1 TO BE INSTALLED WITHOUT A SOCKET
4. P C BOARD 51C5911 REV. -10, -20
5. SCHEMATIC 91C7236 REV. AØ

REVISIONS	DATE	APPR
REL FOR PROD. STATUS WAS ORIGINAL E.C.O. 2300	5 NOV 80	

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA CALIFORNIA 93017

COMPONENT LAYOUT
STATUS INPUT, OPTO II

DWN 5 NOV 80 SCALE
CHK 11-11
ENG

20D2795 AØ

ITEM NO	DESCRIPTION	REF DESIG	STOCK NO	QTY
19	CAPACITOR 220µf 10V	C2	4280186	1
18	" .1 µf 50V	C3-C9	4310207	7
17	RESISTOR 10K, 1/4W, 10%	R1-R20	4410379	20
16	" 1.8K, 1/4W, 10%	R21-R36	4410270	16
15	" 1K, 1/4W, 10%	R37	4410247	1
14	SWITCH BCD, EECO 2300 576	S1 YELLOW	3150117	1
13	SOCKET, I.C., 6 PIN	U6-U21	3250008	16
12	" " 14 PIN	U1, U2	3250024	2
11	" " 16 PIN	U3	3250032	1
10	" " 20 PIN	U4, U5, U22, U23	3250057	4
9	I.C. TIL-112	U6-U21	3730777	16
8	" SN74LS244	U23	3660859	1
7	" SN74LS240	U4, U5, U22	3660974	3
6	" SN74LS139	U3	3660800	1
5	" SN74LS86	U1	3660743	1
4	" SN74LS30	U2	3660735	1
3	LABEL MAI 10A1068-6		3430337	1
2	EJECTOR PAIR, VERO C12409-1,-2.		1250075	1
1	P C BOARD, SIC5911-10,-20		3472453	1

REL. FOR PROD. STATUS MAS DIGITAL 22 DEC 81 LK

REVISIONS | MGMT APPR | DATE

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA CALIFORNIA 93117

COMPONENT LAYOUT
STATUS INPUT, OPTO II

TOL FRACT ± 1/32 .X ± .030 .XX ± .010 ∠ ± 1/2°

DWN 5 NOV 80 SCALE

CHK 11-11 801

ENG 11 Nov 80

20D2795 AØ

OUTPUT - OPEN COLLECTOR

Schematic 91C7171
Assembly 20C2755

I. PURPOSE

This board provides 16 open-collector outputs for driving control relays.

II. SPECIFICATIONS

Maximum voltage that can be applied to outputs without causing output latch-up is 55V. Up to 300 mA may be sinked by the 75452 drivers.

III. ELECTRICAL ADJUSTMENTS

Switch S1 is used to assign a board address from Ø to 15. Board Ø will output Channels 1 through 16; Board 1 will output Channels 16 through 32, etc. Programming of S1 is shown in Fig. 1. S1 is programmed at the factory and will not normally require changing. Any replacement board should be switched to the same configuration as the original board.

IV. THEORY OF OPERATION

IC U1, in conjunction with switch S1 is used as a programmable inverter for address selection. IC U2 ANDS the outputs of U1 along with VMA (Valid Memory Address), PRE (I/O Select), A7 and A8 to form the board address location.

With all four switches in the OFF position, the address for the board will begin at 8180 and end at 8193 as each card required four addresses. If all four switches are ON, the address will begin at 81BC and end at 81BF.

The output of IC U2 is inverted by IC U3 to form an active high board select, which is fed to the chip select on IC U4 (pin 24) and to the bus buffer selector IC U3. If the CPU requests data from the PIA (Peripheral Interface Adapter), U6, the R/*W (Read/Write) line, P1-64, will be high, enabling pin 19 of IC U13 and IC U14, allowing data to pass onto the data bus. This read function is used to check operation of the PIA. If R/*W is low, pin 1 of IC U13 and IC U14 will be low, enabling a command to be written into the PIA.

Output CB2 on IC U6 is used to disable all outputs simultaneously during a failsafe condition. Transistors Q1 and Q2 are current source to interface the PIA with the drivers.

V. TROUBLESHOOTING

1. Partial Failure (Some Channels Work)

This indicates that at least some PIA channels are functioning. Trace back from the output driver to the output of the PIA. Example: Assume Channel 1 does not function. If tally-back does not function, suspect IC's U13, U14 or U4. If the tally-back functions, the failure is in the output driver.

2. Complete Failure (All Channels)

Check IC U4 pin 19 for a low level. If the ENABLE signal is low, check operation of Q1 and Q2. If pin 19 is

high, check PIA pin 24 for an active high pulse when a raise on this board is attempted. If no pulse is seen, verify operation of S1, U1, U2 and U3.

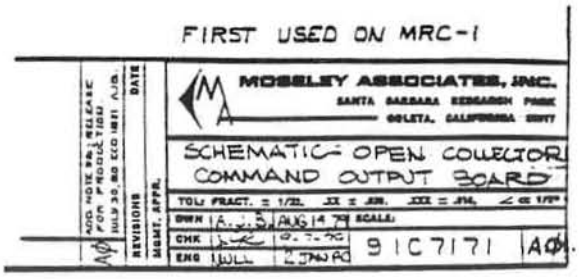
If a pulse is seen at PIA pin 19, verify that the pulses are repeated at pin 1 of IC U13 and IC U14. If these pulses are present, suspect U13, U14 or U4.

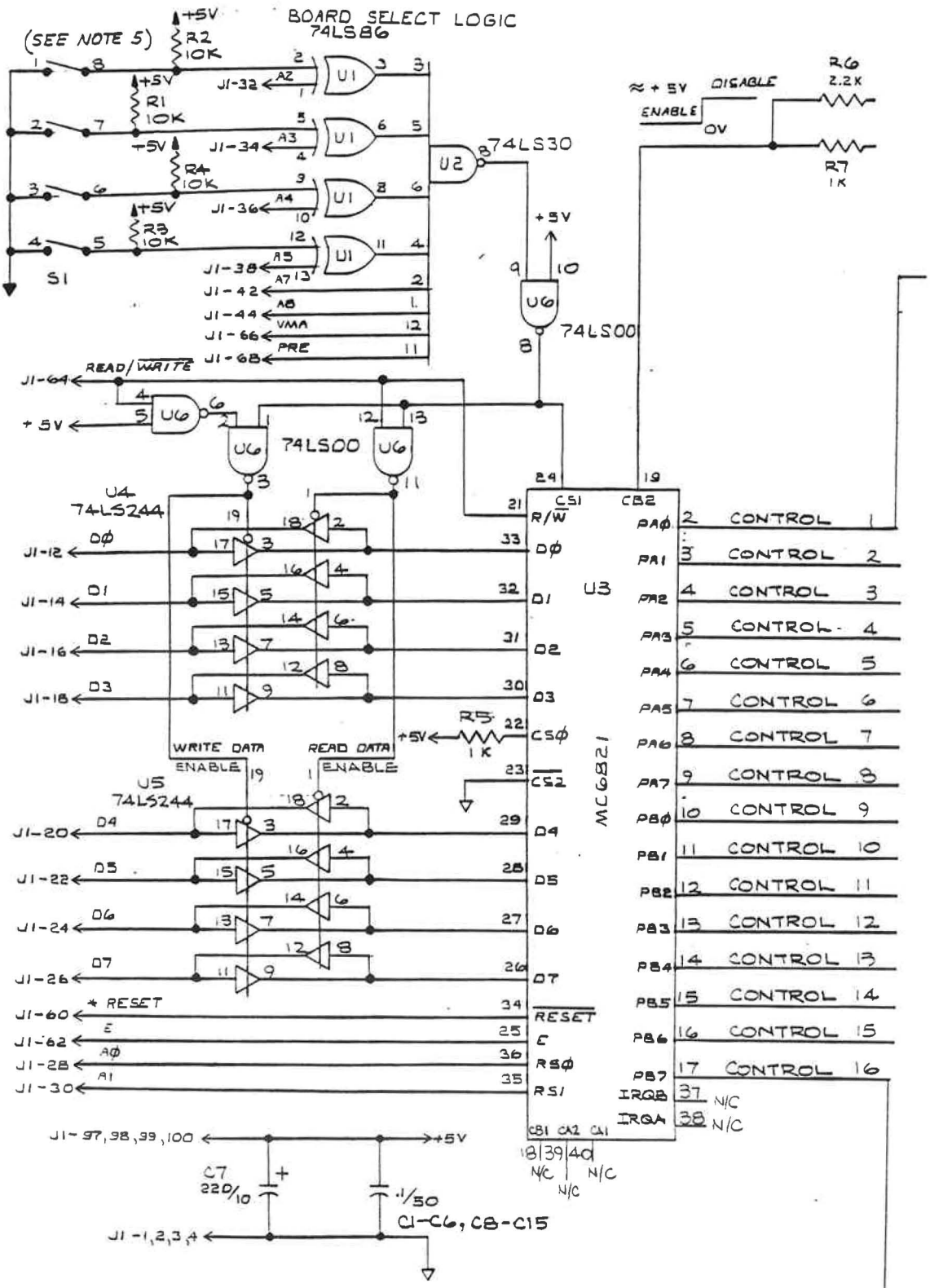
Pos 4	Pos 3	Pos 2	Pos 1	Address	Channels
OFF	OFF	OFF	OFF	0	1-16
OFF	OFF	OFF	ON	1	17-32
OFF	OFF	ON	OFF	2	33-48
OFF	OFF	ON	ON	3	49-64
OFF	ON	OFF	OFF	4	65-80
OFF	ON	OFF	ON	5	81-96
OFF	ON	ON	OFF	6	97-112
OFF	ON	ON	ON	7	113-128
ON	OFF	OFF	OFF	8	129-144
ON	OFF	OFF	ON	9	145-160
ON	OFF	ON	OFF	10	161-176
ON	OFF	ON	ON	11	177-192
ON	ON	OFF	OFF	12	193-208
ON	ON	OFF	ON	13	209-224
ON	ON	ON	OFF	14	225-240
ON	ON	ON	ON	15	241-256

FIGURE 1

S1 PROGRAMMING

FIRST USED ON MRC-1



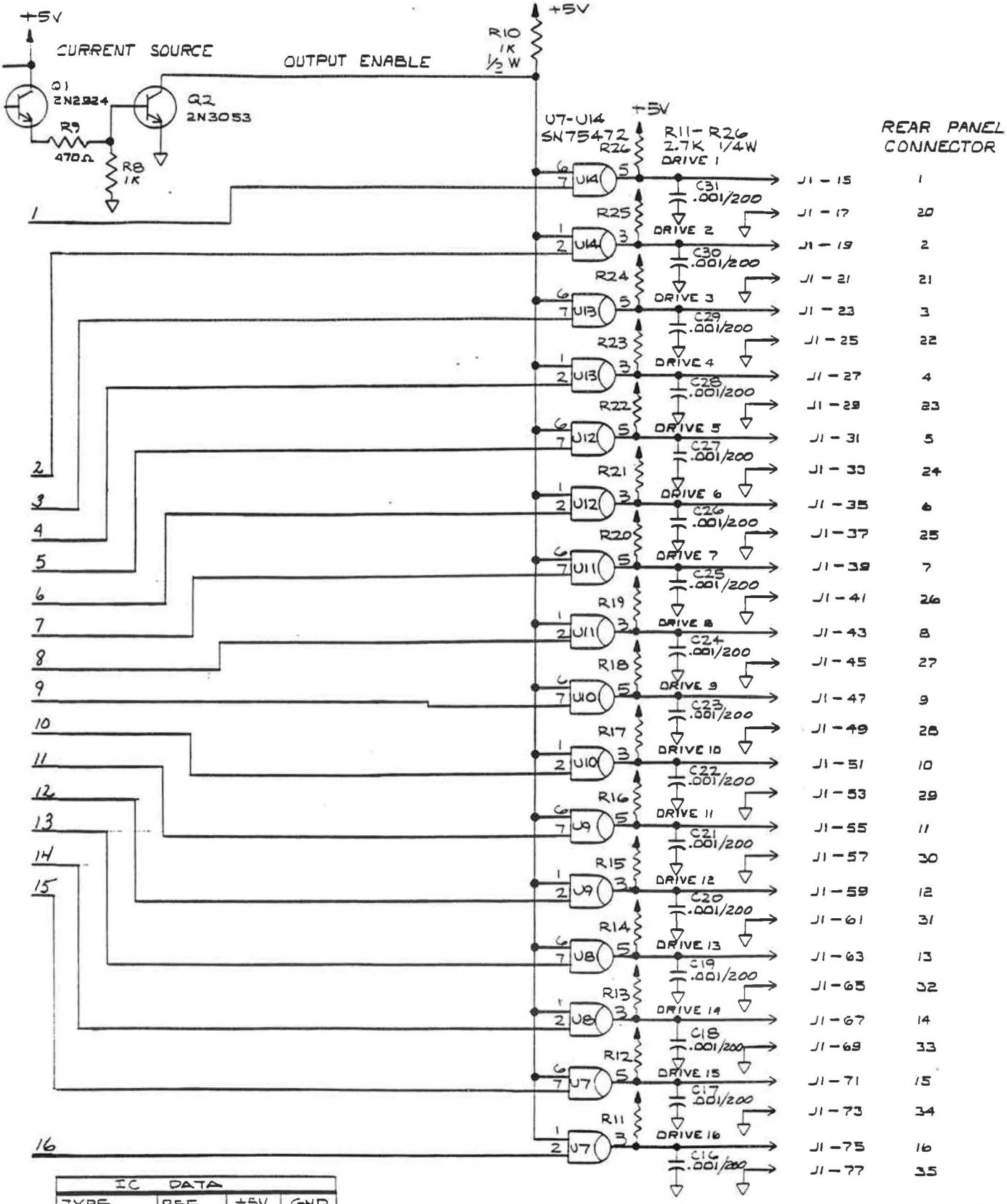


NOTES:

1. UNLESS OTHERWISE SPECIFIED ALL RESISTOR VALUES ARE IN OHMS, 1/4 W, 10%.
   CAPACITOR VALUES ARE IN MICROFARADS.
2. TRANSISTOR PINOUTS BOTTOM VIEW.

3. COMPONENT LAYOUT 20D2755
4. P.C. BOARD 51C5885-50
5. SWITCH - DIP - CTS 206-4
6. RESISTORS R11 THRU R26 ARE INSTALLED ONLY FOR 20D2755-2

Continued on next page



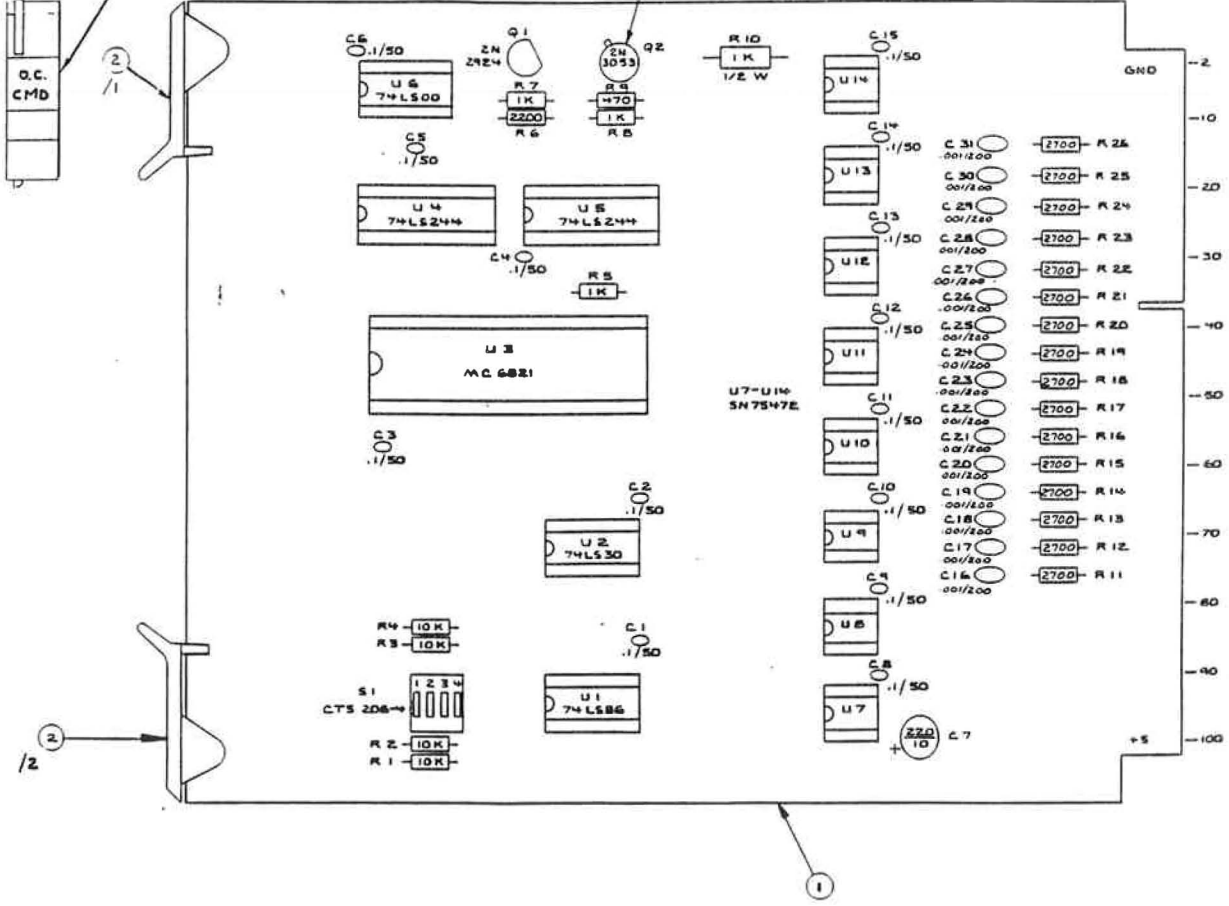
IC DATA			
TYPE	REF	+5V	GND
74LS86	U1	14	7
74LS30	U2	14	7
74LS00	U6	14	7
MC6821	U3	20	1
SN75472	U7-U14	8	4
74LS244	U4, U5	20	10

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA

SCHEMATIC - OPEN COLLECTOR COMMAND OUTPUT BOARD

DWN	B.J.S.	AUG 14 73	SCALE:
CHK		9-7-73	91C7171 A
ENG	WILL	2 JAN 74	

REVISIONS: A ADD NOTE #3, RELEASE FOR PRODUCTION JULY 30, 73 ECO 1821 A/D.



NOTES

1. UNLESS OTHERWISE SPECIFIED
   RESISTOR VALUES ARE IN OHMS, 1/4 W, 10 %.
   CAPACITOR VALUES ARE IN MICROFARADS.
2. P.C. BOARD 51C5885-50.
3. SCHEMATIC 91C7171.
4. RESISTORS R11 THRU R26 ARE INSTALLED ONLY FOR 20D2755-2

REVISIONS	DATE	MGMT. APPR
B4 ADDED NOTE 4; RELEASED FOR PROD. ECO 1821, 7-30-80 RB		
A9 ADD ITEM 9 ECO1696 WPO:21APR 80		

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA 93017

COMPONENT LAYOUT
O.C. COMMAND OUTPUT ASSY.

TOL: FRACT. ± 1/32, XX ± .030, XXX ± .010, ∠ ± 1/2°
DWN CWF 3 MAR 80 SCALE: 2X
CHK [illegible] 80
ENG [illegible] 22 MAR 80

20D2755 B9

ITEM NO.	DESCRIPTION	REF. DES16.	STOCK NO.	QTY.
28	RESISTOR 270Ω	R11-26	4410296	16
27	" 1K 1/2W	R10	4420261	1
26	" 10K	R1-4	4410379	4
25	" 220Ω	R6	4410288	1
24	" 1K	R5,7,8	4410247	3
23	RESISTOR 470Ω	R9	4410205	1
22	CAPACITOR .001	C16-31	4310090	16
21	" .1/50	C1-6,8-15	4310207	14
20	CAPACITOR 220/10	C7	4280186	1
19				
18	SWITCH CTS 206-4	S1	3190011	1
17				
16	I.C. SOCKET AMP 640379-1	U3	3250099	1
15	" " " 640464-1	U4,5	3250057	2
14	" " " 640357-1	U1,2,6	3250024	3
13	I.C. SOCKET AMP 640463-1	U7-14	3250016	8
12				
11	TRANSISTOR 2N3053	Q2	3630035	1
10	TRANSISTOR 2N2924	Q1	3630027	1
9	LABEL	1DA1068-9	3430360	1
8	" SN75472	U7-U14	3660941	8
7	" MC 6821	U3	3710027	1
6	" 74LS244	U4,5	3660859	2
5	" 74LS86	U1	3660743	1
4	" 74LS30	U2	3660735	1
3	I.C. 74LS00	U6	3660669	1
2	EJECTOR, PAIR	VERO 12409/1 & /2	1250075	1
1	P.C. BOARD	5105885	3472644	1

REVISIONS	DATE	MGMT. APPR.
B ADDED NOTE 4, RELEASED FOR PROD. ECO 1821, 23 JAN 80 AB		
A ADD ITEM 9 ECO1696 WP 6 24 MAR 80		

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA 93017

COMPONENT LAYOUT
O.C. COMMAND OUTPUT ASSY.

TOL: FRACT. ± 1/32. XX ± .030. XXX ± .010. ∠ ± 1/2°
DWN PWF 3/MAR 80 SCALE: 2X
CHK [illegible] 7 MAR 80
ENG [illegible] 22 MAR 80

20D2755 B

OUTPUT - OPTICALLY ISOLATED

Schematic 91C7129
Assembly 20B2705
PC Board 51B5846

I. PURPOSE

This module provides 16 optically isolated outputs for con-control of external equipment.

II. SPECIFICATIONS

The maximum voltage that should be applied to the outputs is 48 VDC. The maximum voltage drop on a ON channel is 1.4V, with a maximum of 250 mA load. When a channel is OFF, the leakage current will not exceed 50 μA. The outputs incorporate built-in reverse polarity and inductive load protection. The maximum voltage from an output line to ground is ±50 VDC. Exceeding that voltage may cause damage to the board. Output is floating with respect to the chassis.

III. ELECTRICAL ADJUSTMENTS

Switch S1 is used to assign a board address from Ø to 15. Board Ø will output Channels 1 through 16; Board 1 will output Channels 17 through 32, etc. Programming of S1 is given in Fig. 1. S1 is programmed at the factory and will normally only be reset if a defective board is replaced. In this case, the switch on the new board should be set to the same position as the board it is replacing.

IV. THEORY OF OPERATION

IC U1, in conjunction with S1, is used as a programmable inverter for address selection. IC U2 ANDS the outputs of U1 along with VMA (Valid Memory Address), PRE (I/O Select), A7 (Address Line 7), and A8 (Address Line 8) to form the address at which the board will operate. With all four switches on S1 OFF, the address for the board will begin at 8180 and end at 8193 as each card requires four addresses. If all four switches on S1 are ON, the address for the board will begin at 81BC and end at 81BF.

The output of U2 is inverted by U3B to form an active high board select which is fed to the chip select on U6 (pin 24) and the bus buffer selectors U3C and U3D. If the CPU desires to read data from the PIA (Peripheral Interface Adapter) U6, the R/W (Read/Write) line, P1-64, will be high. This causes the output of U3D to go low, which enables U4A-D and U5A-D to activate. This allows data from U6 to pass through U4 and U5 to the data bus. If the CPU desires to write data to U6, the R/W line will be low. This causes the output of U3C to go low, which enables U4E-H and U5E-H to activate. This allows data from the data bus to pass through U4 and U5 to U6.

Output CB2 on U6 is used to disable all outputs simultaneously. This occurs during failsafe. To enable outputs, CB2 is brought low, forward biasing Q33 and Q34 which supplies +5V to the optical isolators. Q1 through Q16 are used to boost the output current of U6 to a sufficient value in order to drive U7 through U22. The outputs of U7 through U22 are used to forward bias the Darlington output transistors Q17 through Q32 (floating from chassis).

V. TROUBLESHOOTING

1. Partial Failure (Some Channels Work)

This indicates that the PIA (Peripheral Interface Adapter), U6, is at least partially functioning. Trace back from the output stage to the output of the PIA. Example: Assume Output 1 does not function. If the tally-back does not function, suspect U4-U6. If the tally-back functions, the failure is in the output driver of U6 or the transistor buffers. Typical voltages are shown for the output buffers. Note the different output voltages for the PA series outputs and PB series outputs of the PIA.

2. Complete Failure (All Channels)

Check U6 pin 19 for a low level. If it is, verify that the emitter of Q34 is near 5V. If it is not, suspect Q33 or Q34. Check pin 24 for an active high pulse when a raise is attempted for a channel on that board. If no pulse is seen, check S1, U1, U2 and U3 pins for correct operation. If a pulse is seen, verify that pulses appear at U4 and U5 pins 1 and 19; if not, suspect U3. If these pulses are present, suspect U4, U5 and U6.

Pos 4	Pos 3	Pos 2	Pos 1	Address	Channels
OFF	OFF	OFF	OFF	0	1-16
OFF	OFF	OFF	ON	1	17-32
OFF	OFF	ON	OFF	2	33-48
OFF	OFF	ON	ON	3	49-64
OFF	ON	OFF	OFF	4	65-80
OFF	ON	OFF	ON	5	81-96
OFF	ON	ON	OFF	6	97-112
OFF	ON	ON	ON	7	113-128
ON	OFF	OFF	OFF	8	129-144
ON	OFF	OFF	ON	9	145-160
ON	OFF	ON	OFF	10	161-176
ON	OFF	ON	ON	11	177-192
ON	ON	OFF	OFF	12	193-208
ON	ON	OFF	ON	13	209-224
ON	ON	ON	OFF	14	225-240
ON	ON	ON	ON	15	241-256

FIGURE 1

S1 PROGRAMMING

FIRST USED ON: MRC-1

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA

SCHEMATIC

DIGITAL OUTPUT, OPTICALLY ISOLATED

TOL: FRACT. ± 1/32, .XX ± .03, .XXX ± .010, ∠ ± 1/2°

DWN	AJ B.	OCT. 25, 78
CHK	FXY	15 FEB 79
ENG	WATT	15 FEB 79

SCALE:

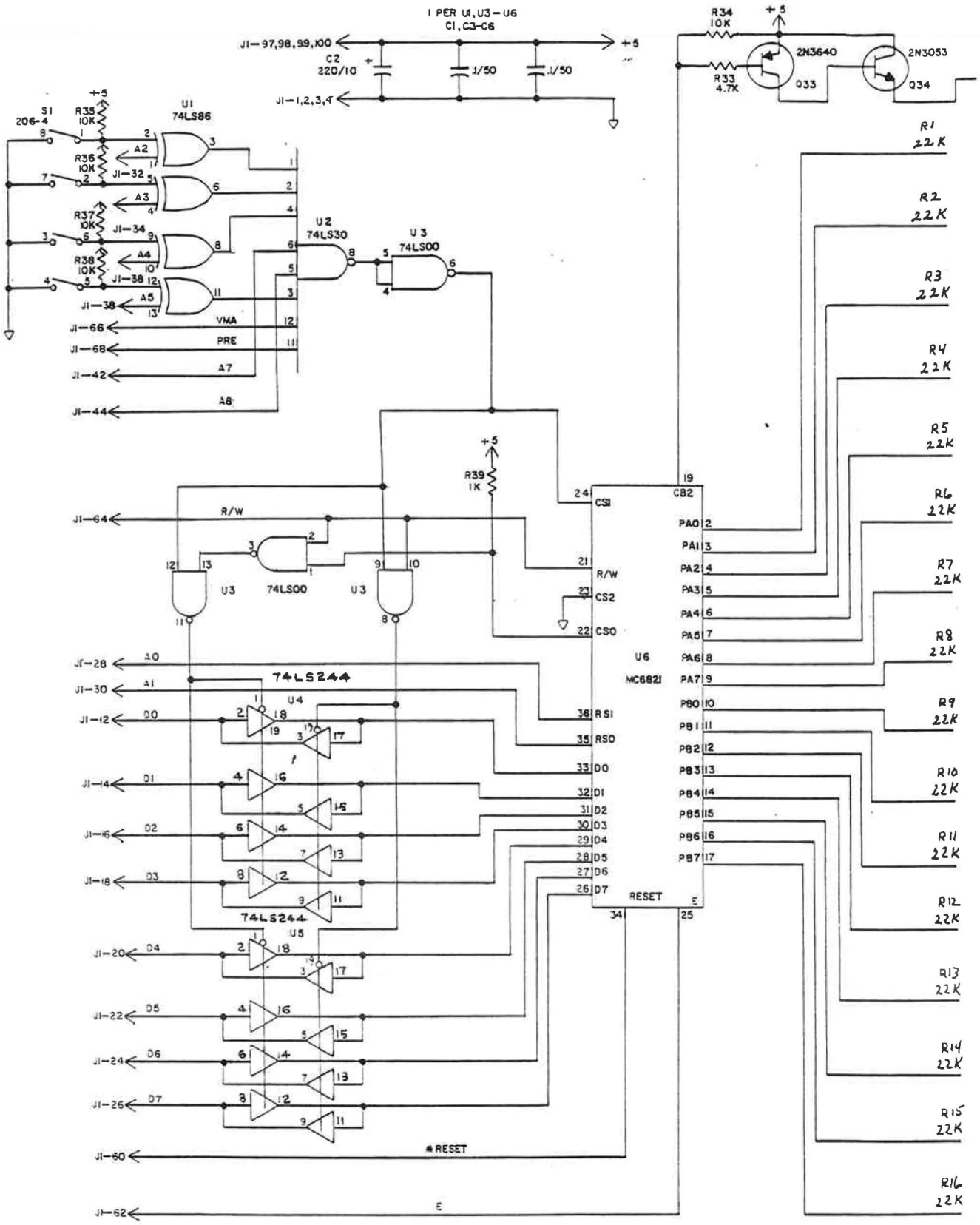
91C7129 D

REVISIONS

A	RELEASED FOR PRODUCTION 16 FEB 79 FXY
B	PER ECO 1552 LDH 18 JAN 80
	REPLACED 8T59 DRIVERS WITH 74LS244 BUS DRIVERS
C	MOC8030 WAS TIL112 PER ECO 1695 LDH 29 APR 80
D	Q1-32 WAS 2N6387 ECO 3078 17 AUG 81 CAII

DATE

MGMT. APPR.

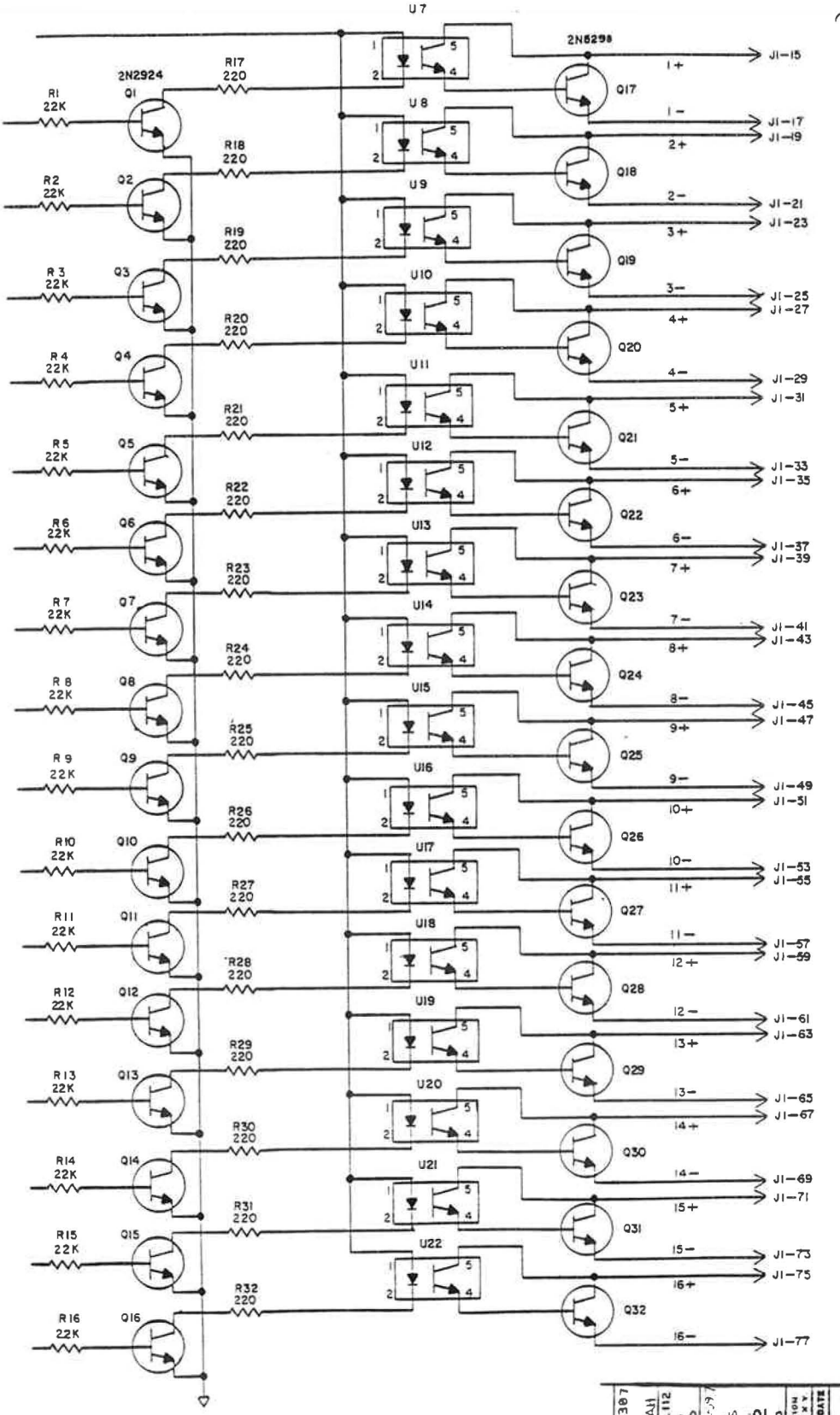


NOTES :
1. UNLESS OTHERWISE SPECIFIED
   RESISTOR VALUES ARE IN OHMS, 1/4 W 10%
   CAPACITOR VALUES ARE IN MICROFARDS
2. P.C. BOARD 51C5846
3. COMPONENT LAYOUT 2002705

Continued on next page

MOC8030

REF: P1 CONNECTOR
ON FILTERED/ UNFILTERED
I/O CARDS



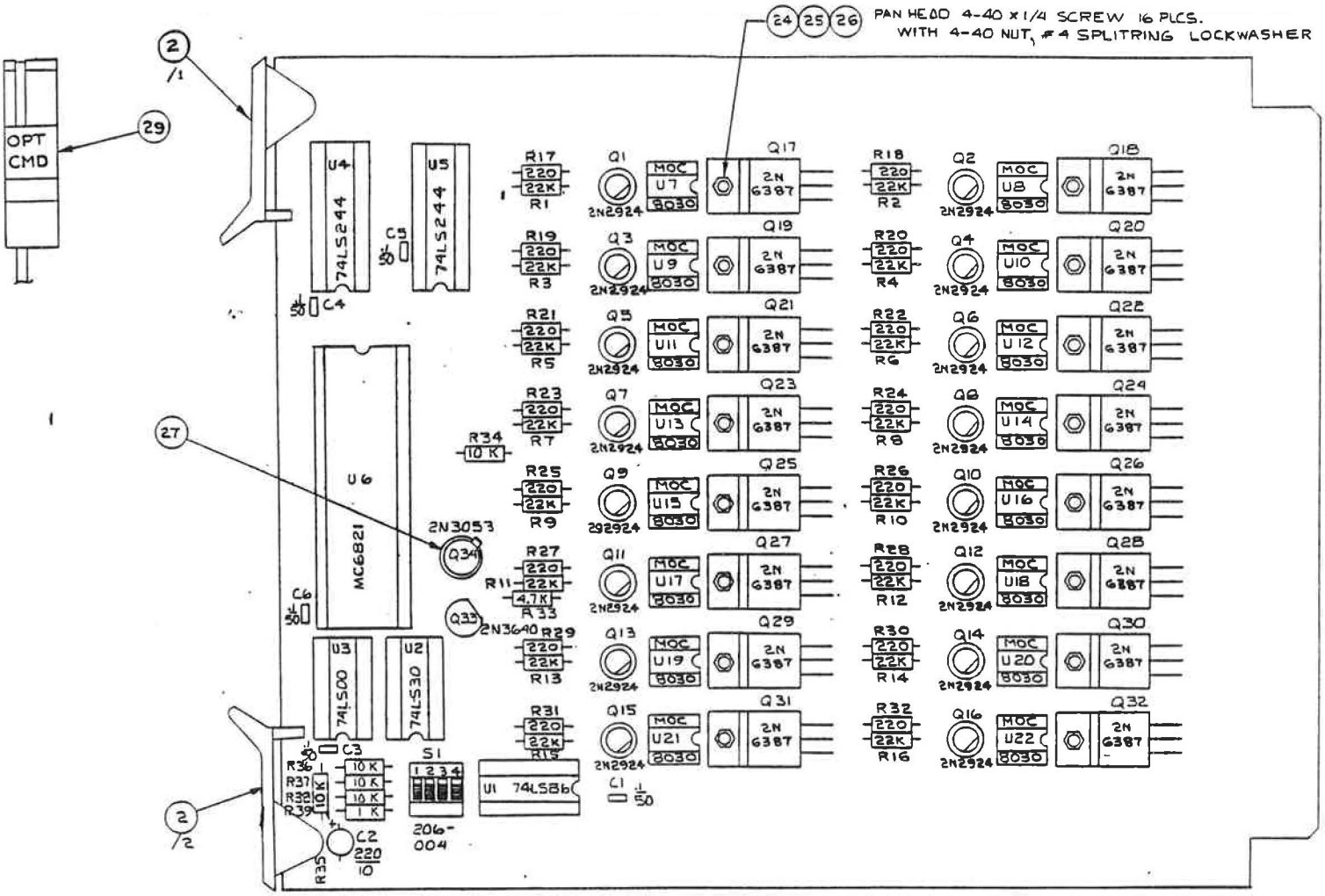
REVISIONS				DATE
MGMT. APPR.	RELEASED FOR PRODUCTION			
A	PER ECO 1552 LDH 18 JAN 80			
B	MOC8030WASTIL112 PER ECO 1495 LDH 29 APR 80	DELETED R17-32 W/A52NG307 DELIVERS WITH 74LS244 BUS DRIVERS		
C	917-32 WAS 2NG307 ECO 3078 17AUG81 CAH			

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA 93017

SCHEMATIC
DIGITAL OUTPUT, OPTICALLY ISOLATED

TOL: FRACT. ± 1/32, XX = .031, XXX = .014, ∠ = 1/2°

DWN	A.J.B.	OCT. 25, 78	SCALE:
CHK	F.I.Y.	15 FEB 79	91C7129 D
ENG	WATT	15 FEB 79	



NOTES:

1. UNLESS OTHERWISE SPECIFIED
   RESISTOR VALUES ARE IN OHMS, 1/4 W, 10%.
   CAPACITOR VALUES ARE IN MICROFARDS
2. P.C. BOARD 51C5846 REV. -12,-21
3. SCHEMATIC 91C7129 REV. CØ
4. ALL TRANSISTORS TO BE SOLDERED (WITHOUT SOCKETS)
5. INSTALL DIPSWITCH, S1, WITHOUT SOCKET AND WITH SWITCH NO.1 ON LEFT SIDE WHEN VIEWING BOARD AS SHOWN

REVISIONS	DATE	MOSELEY ASSOCIATES, INC.
ECO 01695 CHGD PER		SANTA BARBARA RESEARCH PARK
ECO 01696 LDH	29 APR 80	GOLETA, CALIFORNIA 93017
REV 4 REDRAWN WAS 20B2705		COMPONENT LAYOUT
ECO 01552 CHGD PER AJB	3 MAR 80	DIGITAL OUTPUT OPTICALLY ISOL.
		TOL: FRACT. ± 1/32. XX = .030. XXX = .010. ∠ = 1/2°
		OWN LDB 22 FEB 80 SCALE: 2 X
		CHK 3 MAR 80 20D2705 E1
		ENG

ITEM	DESCRIPTION	REF. DES.	STOCK NO.	QTY.
29	LABEL	10A1068-8	3430352	1
28	SOCKET, 6 PIN, ICC-063-53-6	U7-U22	3250008	16
27	PAD, XISTOR, INSUL, RCTO5075-4A	Q34	3250347	1
26	NUT #4-40		1050582	16
25	LOCKWASHER SPLIT RING #4		1050632	16
24	SCREW PAN HD #4-40 x 1/4		1050129	16
23	SOCKET 14 PIN 640357-1	U1, U2, U3	3250024	3
22	" 20 " 640464-1	U4, U5	3250057	2
21	" 40 " 640379-1	U6	3250099	1
20	CAPACITOR K220E10 220/10	C2	4280186	1
19	" CY20C104M .1/50	C1, C3-C6	4310207	5
18	IC MOC8030	U7-U22	3730868	16
17	RESISTOR 1/4W 10% 220Ω	R17-R32	4410163	16
16	" 22K	R1-R16	4410411	16
15	" 10K	R34-R38	4410379	5
14	" 4.7K	R33	4410308	1
13	" 1K	R39	4410247	1
12	TRANSISTOR 2N3640	Q33	3630092	1
11	TRANSISTOR 2N3053	Q34	3630035	1
10	SWITCH CTS 206-004	S1	3190071	1
9	IC MC6821P	U6	3710027	1
8	" SN74LS244	U4, U5	3660859	2
7	" SN74LS86	U1	3660743	1
6	" SN74LS30	U2	3660735	1
5	" SN74LS00	U3	3660669	1
4	TRANSISTOR 2N6387	Q17 THRU Q32	3630381	16
3	TRANSISTOR 2N2924	Q1 THRU Q16	3630027	16
2	EJECTOR SET C12409/1, /2		1250075	1
1	P C BOARD	51C5846-12,-21	3471901	1

REVISIONS

MGMT. APPR.	DATE	
		ADDED U33 ECO 2098 4-29-80 LDH
EØ		CHGD PER ECO 1695 AND ECO 1696 LDH. 29 APR 80
DØ		REV 4 RELEASED WAS 20B2705 CHGD PER ECO 1552 AJB 3 MAR 80

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA 93017

COMPONENT LAYOUT
DIGITAL OUTPUT OPTICALLY ISOL.

TOL: FRACT. ± 1/32. XX = .030. XXX = .010. ∠ = 1/2°

DWN	AJB	20 FEB 80	SCALE: 2 X
CHK		3 MAR 80	2002705 E1
ENG		MAR 80	

FILTERED INTERFACE

Schematic 91A7119
Assembly 20B2718
PC Board 51A5851

I. PURPOSE

This unit is used to provide a means of connecting to a I/O board where RF filtering is required. Each line is passed through a LC lowpass filter to inhibit RF. A metal shield cover is used to prevent RF field leakage.

II. SPECIFICATIONS

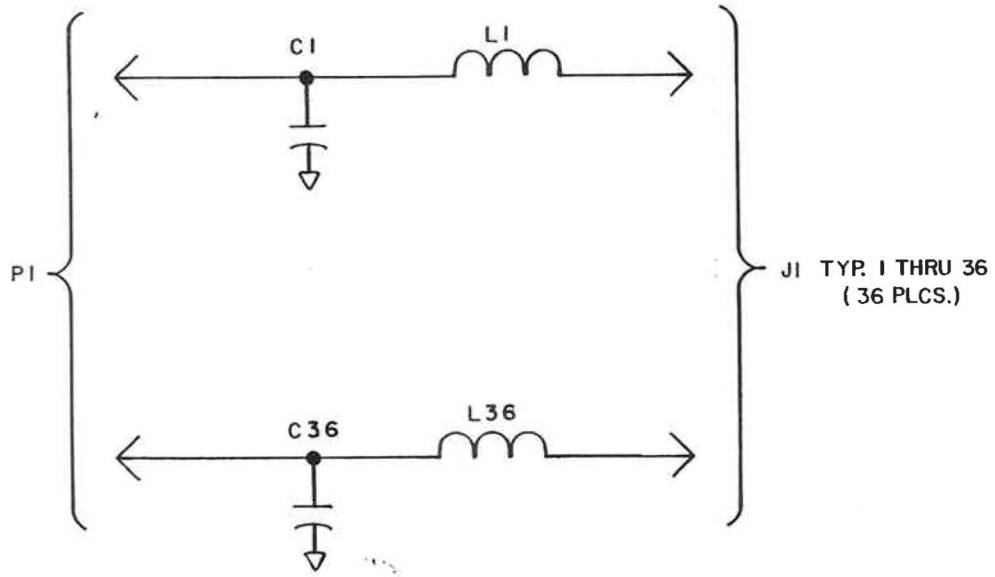
Attenuation:

-10 dB	200 kHz
-20 dB	700 kHz
-40 dB	2 MHz

III. TROUBLESHOOTING

Check for foreign particles across the connector pads, broken traces, and improper solder joints. Check the inductors for continuity and the capacitors for leakage.

Proper shielding and grounding techniques should be observed for all I/O lines.



NOTES:

1. UNLESS OTHERWISE SPECIFIED CAPACITOR VALUES ARE IN MICROFARDS.
2. C1 THRU C36 ARE .1 at 50V
   L1 THRU L36 ARE 6.8 uH
3. P.C. BOARD 51A5851
4. COMPONENT LAYOUT 20B2718

P1	J1
15	1
17	20
19	2
21	21
23	3
25	22
27	4
29	23
31	5
33	24
35	6
37	25
39	7
41	26
43	8
45	27
47	9
49	28
	19 NOT USED
51	10
53	29
55	11
57	30
59	12
61	31
63	13
65	32
67	14
69	33
71	15
73	34
75	16
77	35
79	17
81	36
83	18
85	37

PIN CONNECTIONS.

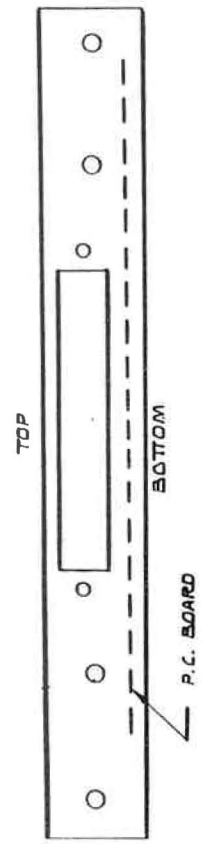
REVISIONS	DATE	MGMT. APPR.
A	RELEASED FOR PRODUCTION 27 FEB 79 F.X.Y.	

MOSELEY ASSOCIATES, IN
SANTA BARBARA RESEARCH P
GOLETA, CALIFORNIA 9

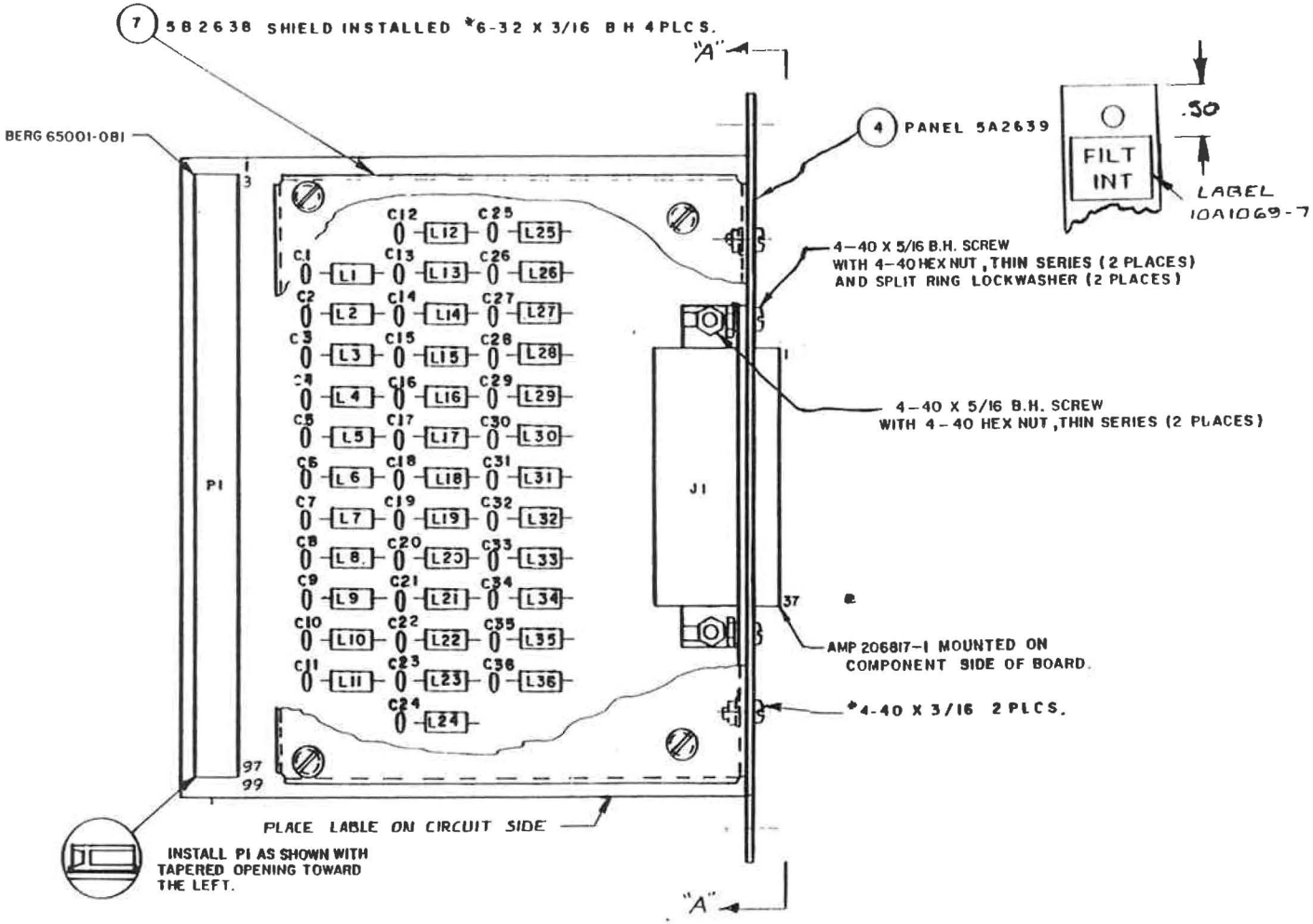
SCHEMATIC
MRC—1 FILTERED INTERFACE

TOL: FRACT. ± 1/32, .XX ± .030, .XXX ± .010, ∠ ±

DWN	A. J. B.	9 NOV. 78	SCALE:
CHK	FXY	27 FEB 79	91A7119
ENG	HATT	27 FEB 79	



VIEW "A-A"



NOTES :
1. UNLESS OTHERWISE SPECIFIED CAPACITOR VALVES ARE IN MICROFARDS.
2. C1 THRU C36 ARE .1 at 50V
   L1 THRU L36 ARE 6.8 uH
3. P.C. BOARD 51A5851
4. SCHEMATIC 91A7119

REVISIONS			
D1	ADD PART LABLE ON BOARD PER ECO 1888	AJB	
C1	REVISE ARTWORK TO WAS 00		
C2	3 DEC. 78 ECO 1484	AJB	
B1	CHANGE TO NEW PRODUCTION (6 SEPT 78 PCO 1362)	AJB	
B0	BERG 65001-081 WAS 65001-035. (7 SEPT 78 ECN 1362)	FXY	
A	RELEASED FOR PRODUCTION (27 FEB 79)	FXY	

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA 93017

COMPONENT LAYOUT
MRC-1 FILTERED INTERFACE

TOL: FRACT. ± 1/32, .XX ± .030, .XXX ± .010, ∠ ± 1/2°

DWN	AJB	7 NOV 78	SCALE: 1:1
CHK	FXY	27 FEB 79	20B2718 D2
ENG	HATT	2 FEB 79	

DIODE-FILTERED INTERFACE

Schematic 91A7207
Assembly 20C2772
PC Board 51C5899

I. PURPOSE

This unit provides filtering and damping for the TTL Status Input Assembly (91C7155). Each input is passed through an LC low-pass filter to inhibit RF. Diodes CR1-CR32 prevent voltages from rising above about 5.8 volts or below -0.8 volt when the input signal changes suddenly.

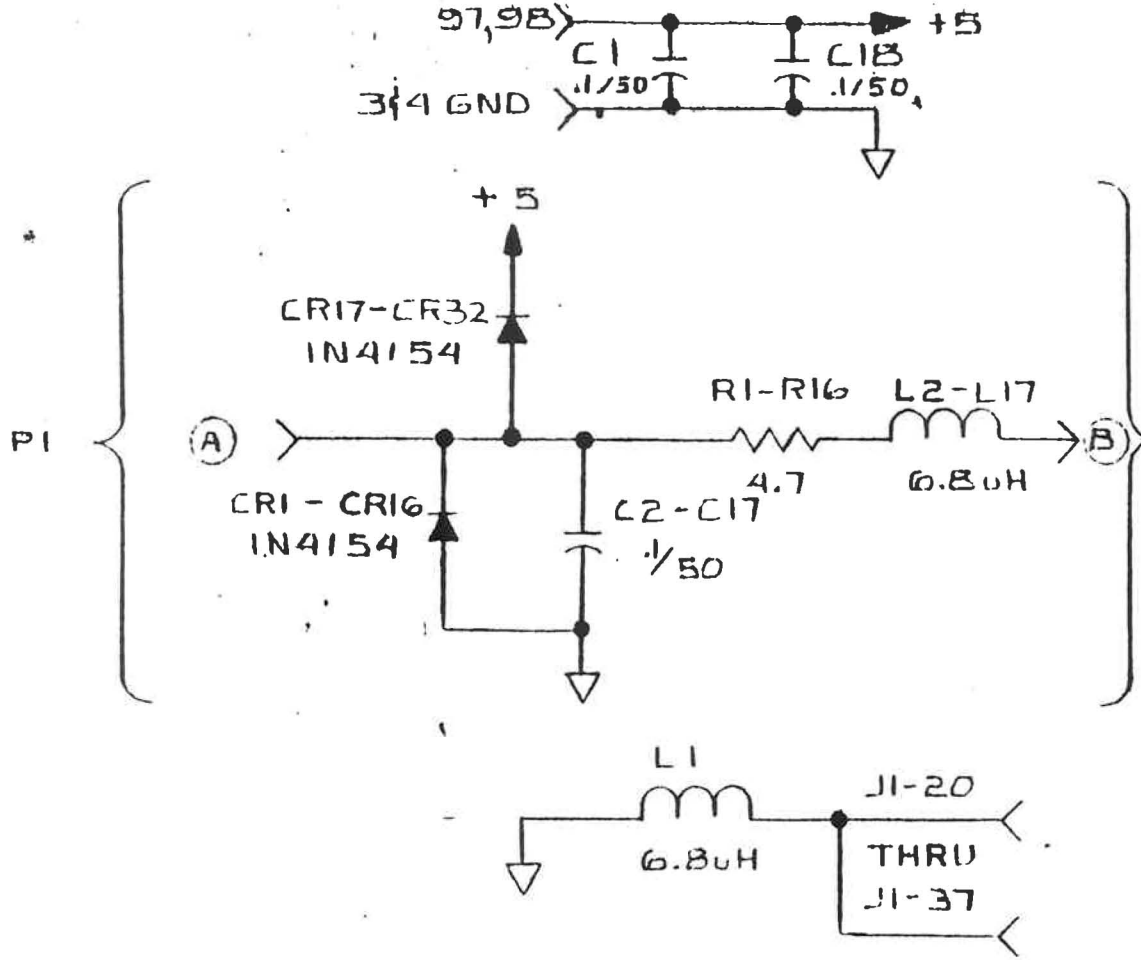
II. SPECIFICATIONS

The attenuation at various frequencies is essentially the same as that of the filtered interface board.

III. TROUBLESHOOTING

Check for foreign particles across the connector pads, broken traces, and improper solder joints. Check the inductors for continuity and the capacitors for leakage.

Proper shielding and grounding techniques should be observed for all I/O lines.



A	B
P1	J1
15	1
19	2
23	3
27	4
31	5
35	6
39	7
43	8
47	9
51	10
55	11
59	12
63	13
67	14
71	15
75	16

PIN CONNECTIONS

1. UNLESS OTHERWISE SPECIFIED RESISTOR VALUES ARE IN OHMS. CAPACITOR VALUES ARE IN MICROFARADS.
2. C2 THRU C17 ARE .1 @ 50V
   L1 THRU L17 ARE 6.8uH
3. P.C. BOARD 51C5899
4. COMPONENT LAYOUT 20C2772

REVISIONS			
MGMT. APPR.	DATE		
A∅	RELEASED FOR PROD. ECO1719 30APR80 D.W.		

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA 93017

SCHEMATIC
MRC-1 DIODE FILTERED I/O

TOL: FRACT. ± 1/32, .XX ± .030, .XXX ± .010, ∠ ± 1/2°

DWN	A.J.B	26NOV79	SCALE:
CHK	[illegible]	12-26-79	
ENG	WILL	2JAN80	91A7207 A∅

91A7202 A∅

REMOTE TERMINAL

AC POWER SUPPLY
7" Chassis

Schematic 91C7179
Assembly 21C2655

I. AC POWER SUPPLY

The power supply used in the 7-inch chassis is easily removed for adjustment, service, or replacement. The rear panel AC connector contains an RF filter, fuse, and a circuit board used to set the AC line voltage. A nine-pin Molex connector interfaces the power supply with the chassis wiring harness.

A. Adjustment

Three voltage adjustment potentiometers are present for +5V, +15V and -15V. A sealed potentiometer is included for current limiting.

B. 120 Volt Operation

The unit is shipped from the factory for 120V. Normally, no changes are required. The voltage selection card should have 110V exposed and easily visible. If some other voltage is visible, remove card and re-insert so that 120V is on the top. A 1A fuse is used for 120V.

C. 240V Operation

Change the voltage card so that the 240V label is visible when the card is installed. Install a 1/2A fuse.

Power-One INC.
D.C. POWER SUPPLIES

APPLICATION DATA
Including:
1. Schematic
2. Parts Lists
3. Specification
4. Outline & Mounting Dwg.
5. General User Information

MODEL

HCBB-75W

SPECIFICATIONS

AC Input: 115/230 VAC ± 10% 47-440 HZ(Derate Current 10% for 50 HZ operation)

Input Fusing: See Table

DC Output: See Table

Line Regulation: ± .05% for a 10% input change

Load Regulation: ± .05% for a 50% load change

Output Ripple: 3mv Pk-Pk +.02% V out

Transient Response: 30μ sec for 50% load change

Overload & Short Circuit Protection: Automatic current limit/foldback

Temperature Coefficient: ± .03%/°C maximum

Cooling: Units are full rated to 50°C in free air, must be derated or fan cooled when mounted in confined area

Temperature Rating: 0 - 50°C, full rated, derate linearly to 40% at 70°C

Efficiency: 55% at nominal input, full load on output

Weight: 8 lbs.

Vibration: Per Mil-Std-810B, method 514, proc. I, curve AB (to 50HZ)

Shock: Per Mil-Std-810B, method 516, procedure V

AC CONNECTION & FUSE TABLE

For Use At	Primary Fuse At	Connect	Apply Power To
115	2A	1-3,2-4	1 & 4
230	1A	2-3	1 & 4

OUTPUT RATING

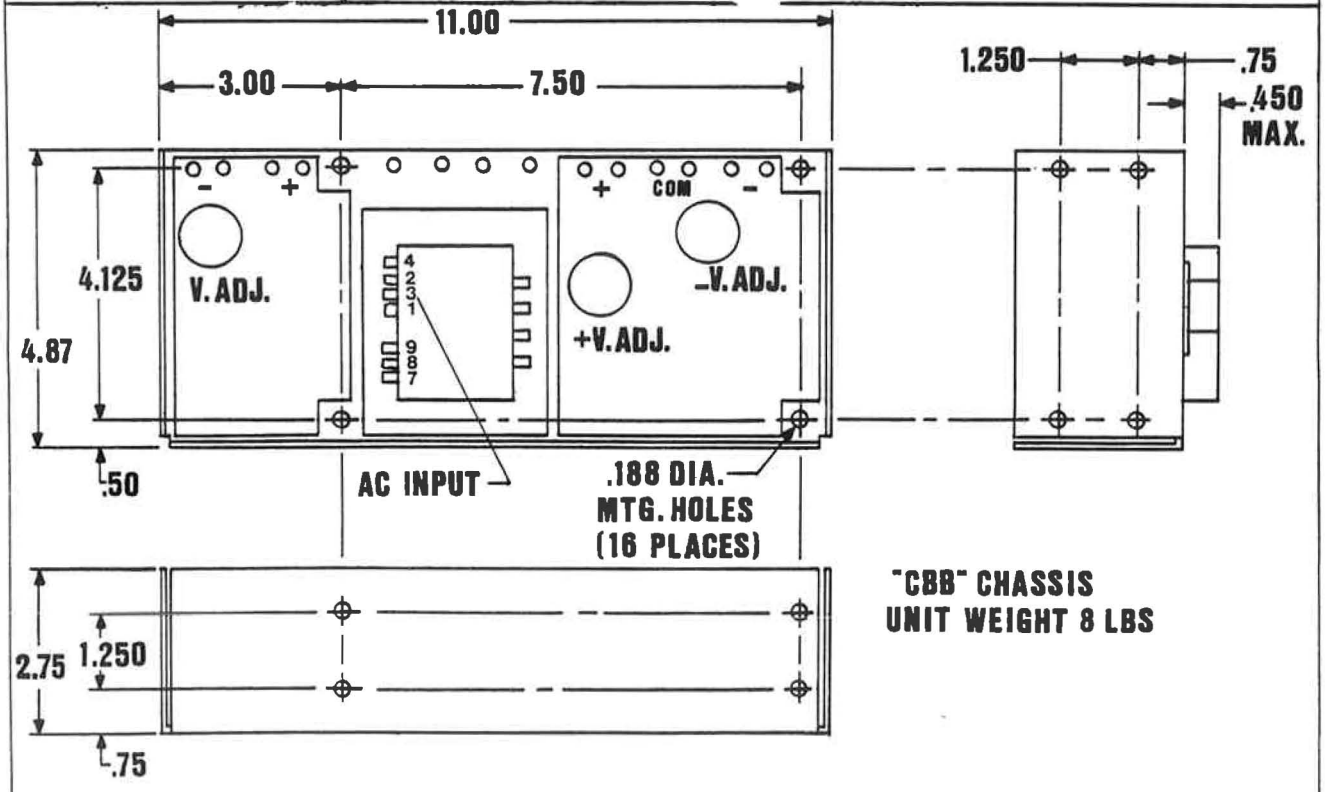
5V @ 6A/OVP @ 6.2 ±.4V
+15V @ 1.5A (Adj. range: 9-15V)
-15V @ 1.5A (ADJ. RANGE: 9-15V)
-or-
- 5V @ .7A*

*This may be accomplished by jumpering E1 to E2 and readjusting the output voltage pot, R16.

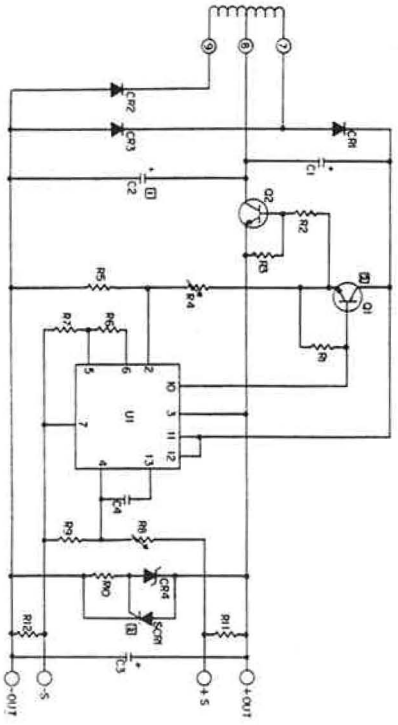
2 YEAR GUARANTEE

POWER-ONE, INC. will repair or replace any power supply of its manufacture that does not perform to published specifications as a result of defective materials or workmanship for a period of 2 years from date of original purchase. No other obligations or liabilities are implied or expressed. Returns must be freight prepaid.

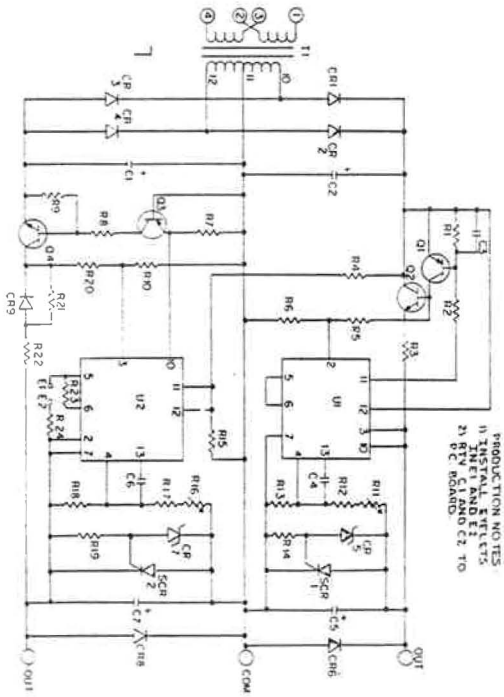
IMPORTANT: This power supply features Remote Sensing capability. Remote Sensing terminals are provided for customer hook-up when used in applications utilizing this feature.
When not using Remote Sensing, or when testing the unit to its specifications, the Remote Sensing terminals should be connected to their respective output terminals as follows: +S to + OUT
-S to - OUT



REMOTE TERMINAL



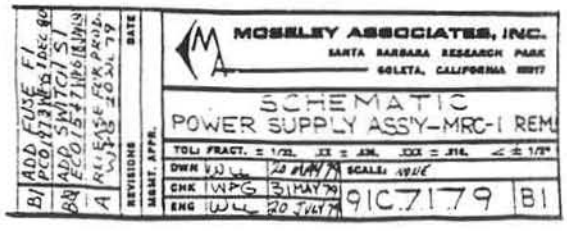
REF DES	HCS-16 OVP	POWER-ONE P/N	DESCRIPTION
C1	1000 Mf, 35V	101-10108	CAPACITOR, ELECT
C2	14000 Mf, 15V	102-10096	CAPACITOR, ELECT
C3	2200 Mf, 15V	101-10107	CAPACITOR, ELECT
C4	.0033/100	104-10092	CAPACITOR, MYLAR
CR1	AEIC	111-10251	DIODE, 1A, 200V
CR2,3	MR750	111-10256	DIODE, 6A, 50V
CR4	IN752A	112-10004	DIODE, ZENER
SCR1	SO508LS3	140-10015	SCR, 8A
Q1	2N6351	172-10243	TRANSISTOR
Q2	12505-2	171-10262	TRANSISTOR
R1	3.9K	151-10329	RESISTOR, ¼W 5% CF
R2	2.7K	151-10305	RESISTOR, ¼W 5% CF
R3,12	6.8Ω	151-10513	RESISTOR, ¼W 5% CF
R4,10	22Ω	151-10525	RESISTOR, ¼W 5% CF
R5,7,6,	2.2K	151-10378	RESISTOR, ¼W 5% CF
R9	2K	192-10512	RESISTOR, 1W 2% MF
R4,8	1.5K	155-10085	POTENTIOMETER
U1	44723	130-10287	IC VOLTAGE REGULATOR
T1	12247	082-12247	TRANSFORMER
CHASSIS	11031	412-11031	CHASSIS
PC B	12098	505-12098	P.C. BOARD

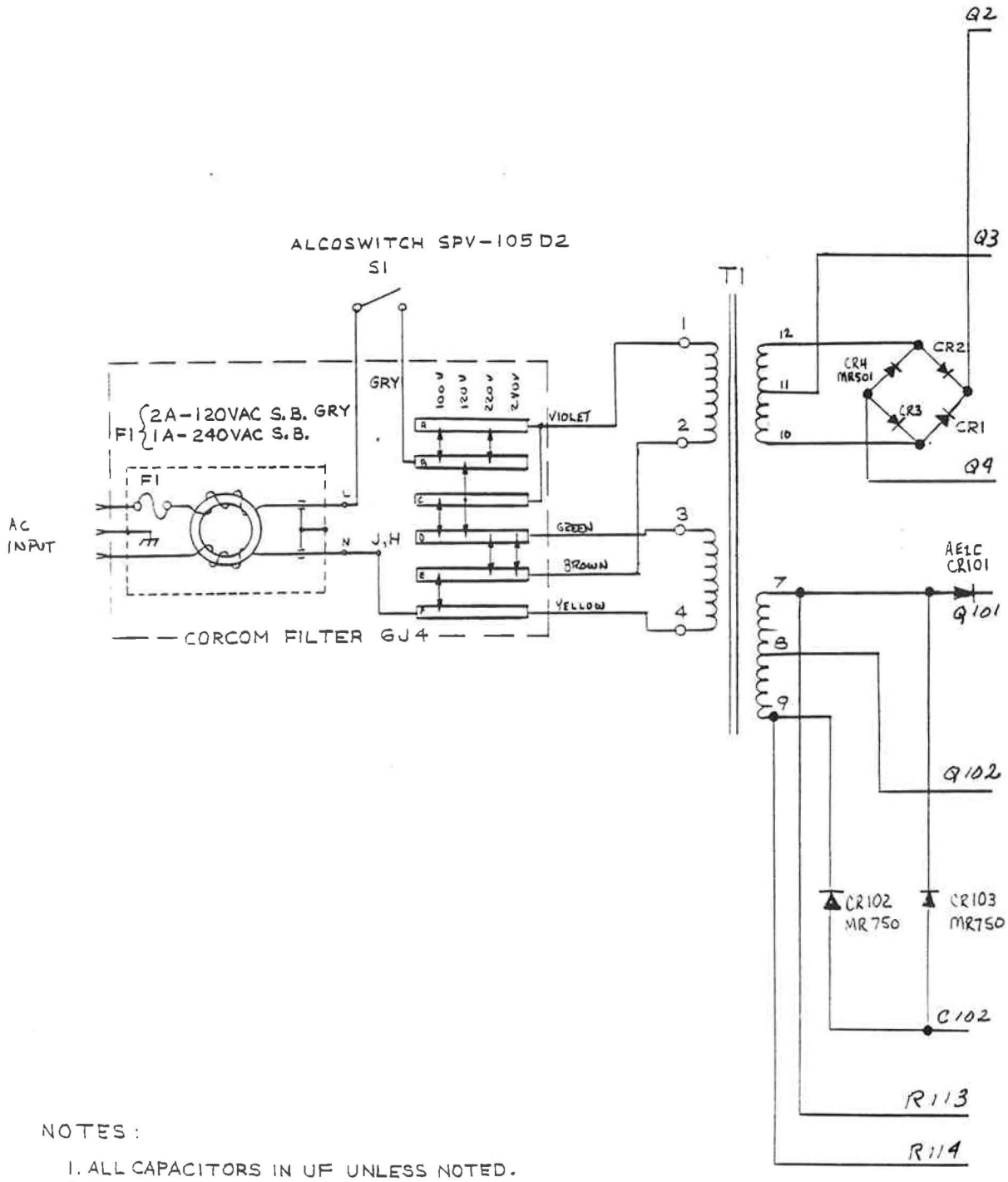


PRODUCTION NOTES
1) INSTALL 5 TELETS
2) R14, C4 AND C2 TO P.C BOARD

REF DES		
C1,2	1000/35	102-10096
C3	2200/15	101-10107
C4,5,6	.01/100	104-10092
CR1,2,3,4,5	AEIC	111-10251
CR6,7	AEIC	111-10251
CR8,9	IN752A	112-10004
Q1,2	12505-3	171-10250
Q3	2N3906A	171-10261
SCR 1,2	J106Y3	140-10015
U1,2	J106Y3	130-10287
R1	1K	151-10365
R4,5,6,9	330Ω	151-10333
R7,8,10	4.7K	151-10381
R11,15		
R12,13	150Ω	151-10345
R14	220Ω	151-10349
R15,16	1.2K	151-10307
R23	2.2K	151-10313
R24	2.7K	151-10315
R20,21	240Ω	151-10370
R17	1.6K	151-10377
R3,22	1.42Ω	155-10075
R18,19	1.5K	155-10085
T1	12171	082-12171
P.C. B	12080	505-12080
CHASSIS	11101	412-11101

	TRANSFORMER
	P.C. BOARD, MOUNT BOARD
	CHASSIS, ALUM
	DIODE 3A 100V
	DIODE ZENER
	TRANSISTOR
	TRANSISTOR
	SCR, 8A
	IC VOLTAGE REGULATOR
	RESISTOR ¼W 5% CF
	½W 5% CF
	¼W 5% CF
	½W 5% CF
	¼W 5% MF
	½W 5% CF
	½W 5% CF
	½W 5% CF
	POTENTIOMETER


B1 ADD FUSE F1 PER ECO 1057
B0 ADD SWITCH S1 ECO 1057
A RELEASE FOR PROD. 20 JUL 79
REVISIONS
MGMT. APPR.
DATE
MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA
SCHEMATIC
POWER SUPPLY ASSY-MRC-1 REM
TOL: FRACT. ± 1/32 .XX ± .030 .XXX ± .010 ∠ ± 1/2°
DWN WJL 20 JULY 79
CHK WPG 31 MAY 79
ENG WJL 20 JULY 79
SCALE: NONE
91C7179
B1

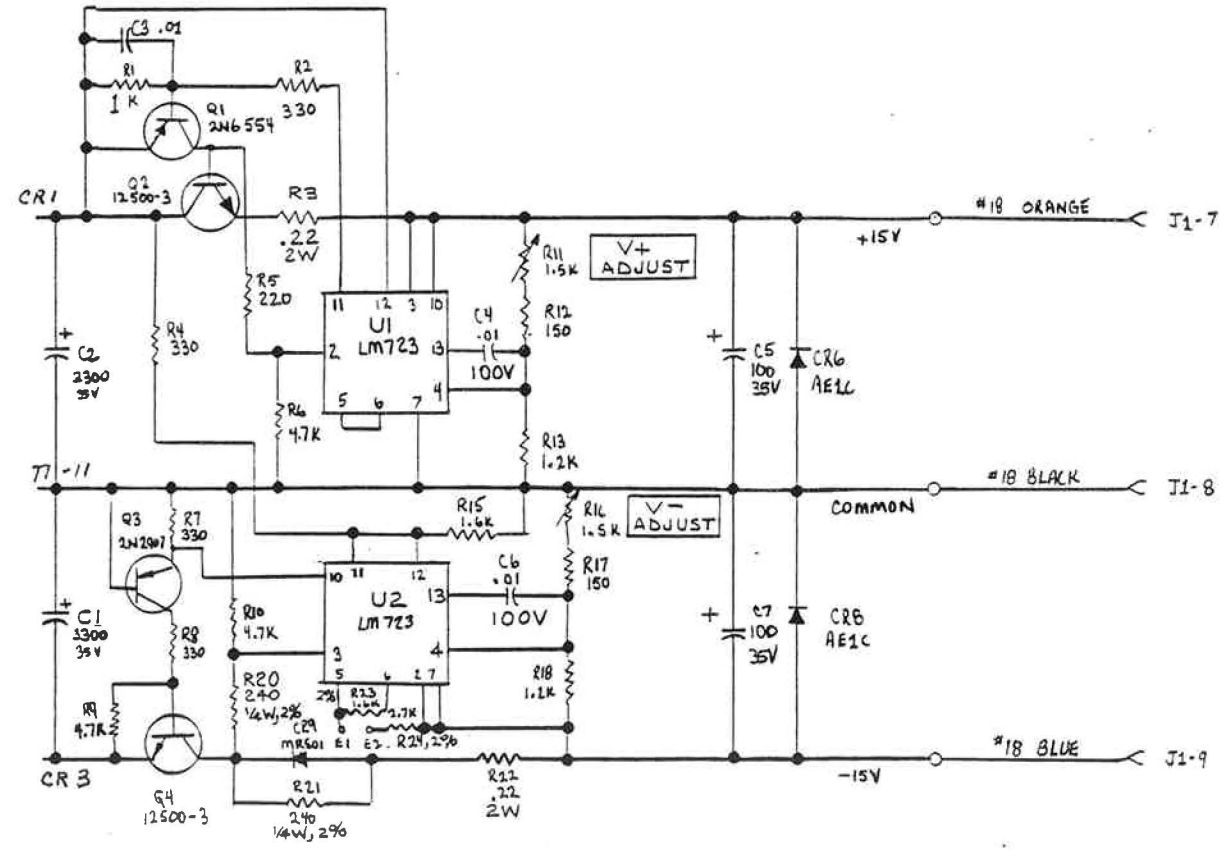


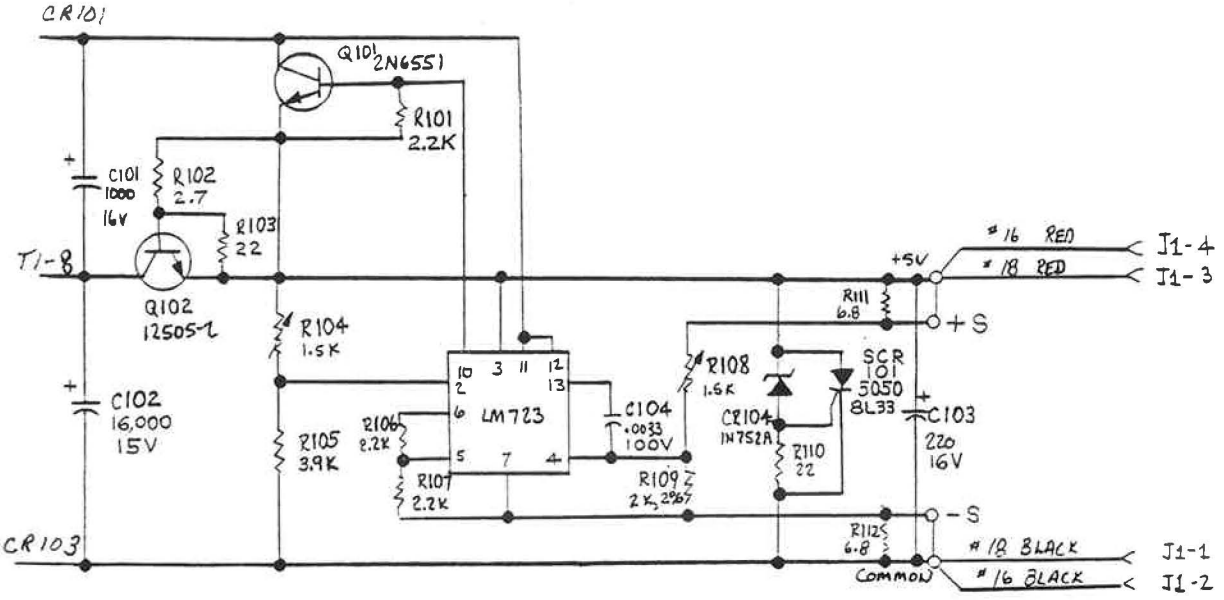
NOTES:

1. ALL CAPACITORS IN UF UNLESS NOTED.
2. ALL RESISTORS IN OHMS, 1/2 W, ±5%, UNLESS NOTED.
3. POWER SUPPLY IS MODEL HCBB-75W, MADE BY POWER-ONE INC. CAMARILLO, CALIF.

± ASSEMBLY DWG 21C2655

Continued on next page





T1-7
#22 GRY/WHT — R113 100 1/4W, ±10% — #22 WHT/BLU — J1-6

#22 GRY — R114 100 1/4W, ±10% — #22 WHT/GRN — J1-5 AC POWER SAMPLE

T1-9

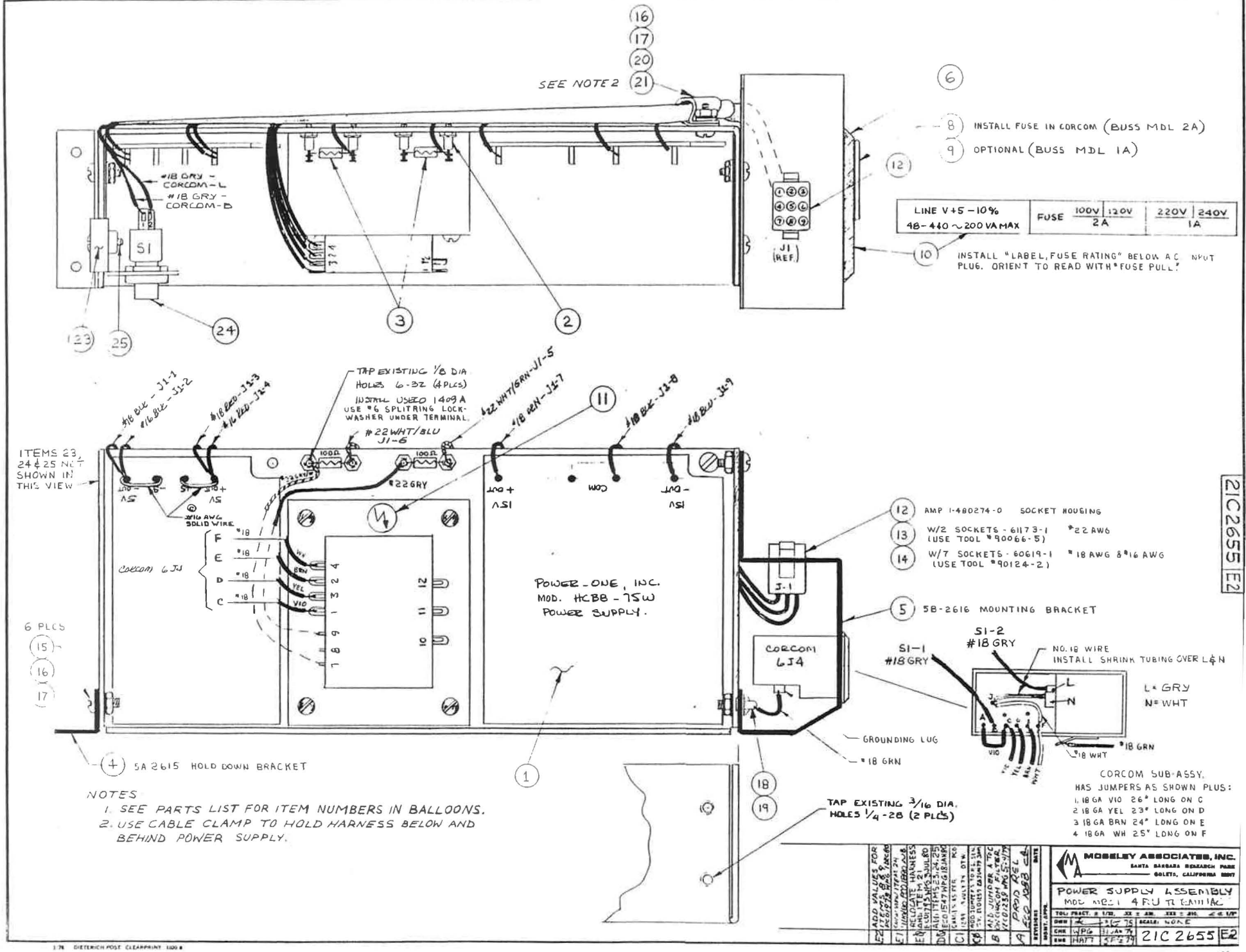
REVISIONS		DATE
B1	ADD FUSE F1 PER ECO 1373 DTD DEC 78	
B	ADD SWITCH S1 PER ECO 1514 DTD JAN 79	
A	RELEASE FOR PROD.	20 JUL 79

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA 93117

SCHEMATIC
POWER SUPPLY ASSY-MRC-1 REM

TOL: FRACT. ± 1/32, XX ± .030, XXX ± .010, ∠ ± 1/2°
DWN WJW 20 MAY 79 SCALE: NONE
CHK WPG 31 MAY 79
ENG DCL 20 JULY 79

91C7179 B1


SEE NOTE 2
#18 GRY - CORCOM-L
#18 GRY - CORCOM-D
S1
J1 (REF.)
INSTALL FUSE IN CORCOM (BUSS MDL 2A)
OPTIONAL (BUSS MDL 1A)
LINE V +5 -10%
48-440 ~200 VA MAX
FUSE 100V 120V 2A 220V 240V 1A
INSTALL "LABEL, FUSE RATING" BELOW A C INPUT PLUG. ORIENT TO READ WITH "FUSE PULL"
#16 BLK - J1-1
#16 BLK - J1-2
#18 BRN - J1-3
#16 RED - J1-4
TAP EXISTING 1/8 DIA HOLES 6-32 (4 PLCS)
INSTALL USECO 1409A USE #6 SPLITRING LOCK-WASHER UNDER TERMINAL.
#22 WHT/GRN - J1-5
#22 WHT/BLU J1-6
#22 GRY
#18 BRN - J1-7
#18 BLK - J1-8
#18 BLU - J1-9
ITEMS 23, 24 & 25 NOT SHOWN IN THIS VIEW
#16 AWG SOLID WIRE
CORCOM 6J5
POWER-ONE, INC. MOD. HCBB-75W POWER SUPPLY.
J-1
CORCOM 6J4
6 PLCS
5A 2615 HOLD DOWN BRACKET
AMP 1-480274-0 SOCKET HOUSING
W/2 SOCKETS - 61173-1 (USE TOOL #90066-5) #22 AWG
W/7 SOCKETS - 60619-1 (USE TOOL #90124-2) #18 AWG & #16 AWG
5B-2616 MOUNTING BRACKET
S1-1 #18 GRY
S1-2 #18 GRY
NO. 18 WIRE INSTALL SHRINK TUBING OVER L & N
L = GRY
N = WHT
GROUNDING LUG
#18 GRN
#18 WHT
#18 GRN
TAP EXISTING 3/16 DIA. HOLES 1/4-28 (2 PLCS)
CORCOM SUB-ASSY. HAS JUMPERS AS SHOWN PLUS:
1. 18 GA VIO 26" LONG ON C
2. 18 GA YEL 23" LONG ON D
3. 18 GA BRN 24" LONG ON E
4. 18 GA WH 25" LONG ON F
NOTES
1. SEE PARTS LIST FOR ITEM NUMBERS IN BALLOONS.
2. USE CABLE CLAMP TO HOLD HARNESS BELOW AND BEHIND POWER SUPPLY.
MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA
POWER SUPPLY ASSEMBLY
MOD MR-1 4 FRU TRAINIAC
SCALE: NONE
21C2655 E2

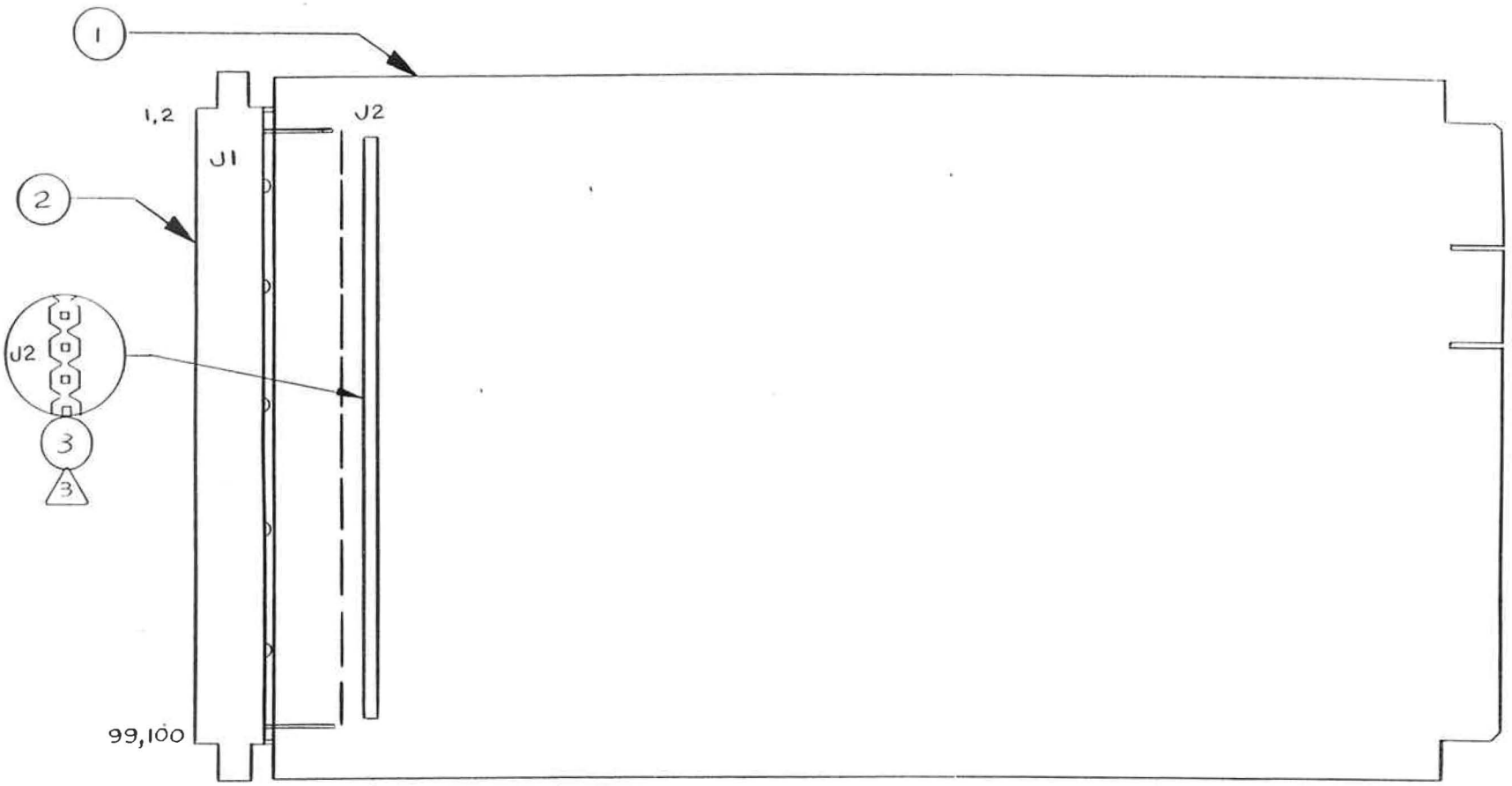
EXTENDER BOARD

Assembly 20B2724
PC Board 51B5854

I. PURPOSE

This card is for troubleshooting active boards by allowing access to the board. Test leads can also be attached to the connector leads for ease in examining bus signals and I/O signals. This board contains no active components.

Exposure of MRC-1 cards outside the protected RF chassis environment via the extender card may cause the unit to be susceptible to RF effects.



QTY.	DESCRIPTION	REF. DES.	STOCK NO.	ITEM NO.
3	WAFER ASSY, MLD · MOLEX 22-03-2201	TRIM TO FIT AS REQD	3250545	3
1	CONNECTOR MAI 2A1413-3	J1	3090180	2
1	P.C. BOARD MAI SIB5854	REV. 11,-21	347968	1
*	EXTENDER BOARD MAI 20P2724		9204348	*

NOTES:

1. P.C. BOARD SIB5854 REV. -11,-21
2. MOUNT CONNECTOR J1 ON P.C. BOARD AS SHOWN AND SOLDER.
3. INSTALL ITEM 3, TRIM TO FIT AS REQD.

ITEM NO: 9200338
USED ON: MRC FAMILY

*STOCK NO. WAS: 9200338 ECO 3474 C4 30APR82

REVISIONS: ECO 2092 CAH 13APR81 — REDRAWN

MOSELEY ASSOCIATES, INC.
SANTA BARBARA RESEARCH PARK
GOLETA, CALIFORNIA 93017

COMPONENT LAYOUT
EXTENDER BOARD

TOL: FRACT. ± 1/32, .XX ± .030, .XXX .010, ∠ ± 1/2°

DWN	CAH	13APR81	SCALE 1:1
CHK		4-21-71	20B2724 EØ
ENG			

PARENT ITEM NO 9051434 SPARE PTS KIT MRC-1 SP-56 06/14/82 DATE 6/15/82 PAGE 1

MOSELEY ASSOCIATES INC
111 CASTILIAN DRIVE
GOLETA CA 93117
805 968-9621

COMPONENT ITEM NO.	STOCK LOCA	MANUFACTURER PART NUMBER	COMPONENT DESCRIPTION	QUANTITY PER	UM	UNIT SALES PRICE	TOTAL SALES PRICE
3390127	2715	FLV160	LED RED 2.0@20 WIDE DIFFUSED	10	EA	.58	5.80
3390143	2715	MV-5354	LED YEL 10.@20 NARROW DIFFUSED	2	EA	1.37	2.74
3390150	2722	MV-5254	LED GRN 3.0@20 NARROW DIFFUSED	2	EA	1.37	2.74
3600053	2744	1N914	DIO 1N914 75V 75MA SI A398	1	EA	.14	.14
3600145	2721	1N4154	DIO 1N4154 25V 4NS SI 0035	1	EA	.16	.16
3600202	2744	1N4740A Z10.0A	DIO Z1N4740A 10V 1W 5% AIAY	1	EA	1.09	1.09
3600236	2744	1N4745A	DIO Z1N4745A 16V 1W 5% AIAY	1	EA	.42	.42
3610003	2721	10D2	DIO 10D2 200V 1A SI 0039	2	EA	.39	.78
3610169	2744	SZ3.1	DIO ZSZ3.1 3.1V	1	EA	3.08	3.08
3630027	2721	2N2924-LFS	XT NS2N2924LFS.2W160M025V.1A7P	3	EA	.54	1.62
3630035	2721	2N3053	XT NP2N3053 05W100M080V.7A	1	EA	1.47	1.47
3630191	2744	2N4037	XT PP2N4037 01W060M060V01A	1	EA	1.54	1.54
3630316	2744	2N5293	XT NP2N5293 36W800K080V04A	3	EA	1.73	5.19
3650066	2743	LM-329BZ	RGLTR PLM329BZ 6.9V 30MA TO92	1	EA	4.73	4.73
3650074	2743	LM340T-12 /7812	RGLTR PLM340T12/7812	1	EA	2.56	2.56
3650124	2743	MC78L12ACP	RGLTR PMC78L12 12V 0.1A TO92	1	EA	1.37	1.37
3650132	2712	MC79L05 ACP	I.C. NMC79L05 05V 0.1A TO92	1	EA	2.80	2.80
3650140	2743	MC79L12	RGLTR NMC79L12 12V 0.1A TO92	1	EA	2.80	2.80
3650157	2743	MC79L15ACP	RGLTR NMC79L15 15V 0.1A TO92	1	EA	3.50	3.50
3650165	2743	MC7905T	RGLTR NMC7905T 05V 1.5A TO220	1	EA	4.38	4.38
3650173	2743	UA 7805 UC	IC UA 7805 UC OP AMP PRECISION	1	EA	4.38	4.38
3660008	2712	SN72741P	IC UA741P OPAMP GEN COMP	1	EA	.83	.83

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COMPONENT ITEM NO.	STOCK LOCA	MANUFACTURER PART NUMBER	COMPONENT DESCRIPTION	QUANTITY PER	UM	UNIT SALES PRICE	TOTAL SALES PRICE
3660487	2743	SN74154N	IC SN74154N 4-16LINE DEMUX	1	EA	3.75	3.75
3660537	2742	SN74174N	IC SN74174N HX D EDGE/TR	2	EA	1.75	3.50
3660669	2743	SN74LS00N	IC SN74LS00N QU 2IN NAND	2	EA	.84	1.68
3660677	2743	SN74LS02N	IC SN74LS02N QU 2IN NOR	1	EA	.84	.84
3660685	2743	SN74LS04N	IC SN74LS04N HX INV	1	EA	.95	.95
3660693	2743	SN74LS08N	IC SN74LS08N QU 2IN AND	1	EA	.84	.84
3660719	2743	SN74LS20N	IC SN74LS20N DU 4IN NAND	1	EA	.79	.79
3660727	2743	SN74LS27N	IC SN74LS27N TR 3IN NOR	1	EA	1.58	1.58
3660735	2743	SN74LS30N	IC SN74LS30N SI 8IN NAND	2	EA	.67	1.34
3660743	2743	SN74LS86N	IC SN74LS86N QU 2IN EXCL OR	2	EA	1.79	3.58
3660750	2743	SN74LS107AN	IC SN74LS107AN DU JK MAS/SL	1	EA	2.63	2.63
3660768	2743	SN74LS123N	IC SN74LS123N DURETRMONOMULTI	1	EA	2.08	2.08
3660776	2743	SN74LS132N	IC SN74LS132N QU 2IN NAND ST	1	EA	1.89	1.89
3660792	2743	SN74LS138N	IC SN74LS138N 3-8LINEDECDEMUX	1	EA	1.96	1.96
3660800	2743	SN74LS139N	IC SN74LS139N DU2-4LNDECDEMUX	1	EA	1.75	1.75
3660826	2743	SN74LS163AN	IC SN74LS163AN BINCOUNT PRESET	1	EA	2.21	2.21
3660859	2743	SN74LS244N	IC SN74LS244N OCT BUS/DRIV ST	4	EA	3.47	13.88
3660867	2743	SN74LS367	IC SN74LS367 HEX BUF 3/ST	1	EA	1.61	1.61
3660875	2743	SN74LS368	IC SN74LS368 HEX INV 3/ST	1	EA	1.61	1.61
3660917	2742	SN75451P	IC SN75451P DU AND HIGHV OC	1	EA	1.02	1.02
3660925	2742	SN75452BP	IC SN75452BP DU NAND HIGHV OC	1	EA	1.05	1.05
3660941	2742	SN75472N	IC SN75472N DU NAND HIGHV OC	2	EA	3.40	6.80

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COMPONENT ITEM NO.	STOCK LOCA	MANUFACTURER PART NUMBER	COMPONENT DESCRIPTION	QUANTITY PER	UM	UNIT SALES PRICE	TOTAL SALES PRICE
3660958	2743	SN74LS32	IC SNF4LS32 QU 2IN OR	1	EA	3.50	3.50
3660966	2742	SN74LS260N	IC SN74LS260N DU 5IN NOR	1	EA	1.40	1.40
3660974	2743	SN74LS240	IC SN74LS240 OCT BUS/DRIV ST	2	EA	3.15	6.30
3680063	2912	CD4040BE	IC CD4040BE 12 STAGE BIN CT	1	EA	4.66	4.66
3680162	2912	SCL4011AE	IC SCL4011AE QU 2IN NAND	1	EA	1.12	1.12
3680212	2733	MC14411P	IG BIT RATE GEN	1	EA	28.00	28.00
3680220	2733	MC14052BCP	IC DIFFERENTIAL AMUX 4CH	2	EA	3.78	7.56
3690021	2742	TIL-308	IC TIL-308 DISP 7 SEG LDP	2	EA	24.22	48.44
3710019	2912	MC6802P	IC MC6802P MICROPROCESSOR	1	EA	23.90	23.90
3710027	2912	MC6821P	IC MC6821P PIA INTERFACE	2	EA	14.70	29.40
3710035	2912	MC6828P	IC MC6828P PRIOR INTERRUPT	1	EA	31.85	31.85
3710043	2912	MC6850P	IC MC6850P ACIA INTERFACE	1	EA	13.83	13.83
3710076	2912	MM53107N	IC MM53107 OSC ZEXP17 DIV	1	EA	4.90	4.90
3710225	2912	M5L2114LP-3	IC M5L2114LP-3 RAM STATIC 1KX4	1	EA	23.38	23.38
3730132	2912	LF13300D	IC LF13300D A-D CONV 4.5DIG	1	EA	23.28	23.28
3730157	2743	LM-308AN	IC LM308AN OPAMP PRECISION	1	EA	6.30	6.30
3730207	2743	LM-339N	IC LM339N COMPARITOR QUAD	1	EA	1.65	1.65
3730355	2743	MC1488L	IC MC1488L QU LINE DRIVER	1	EA	4.03	4.03
3730363	2743	MC1489L	IC MC1489L QU LINE RECEIVER	1	EA	3.96	3.96
3730462	2743	RC4136N	IC RC4136N OPAMP QUAD 741	1	EA	2.98	2.98
3730595	2912	ADB1200PCN	IC ADB1200PCN A-D CONV 12+SGN	1	EA	19.25	19.25
3730694	2742	NE-531	IC NE-531 OPAMP HI SLEW	1	EA	8.40	8.40

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COMPONENT ITEM NO.	STOCK LOCA	MANUFACTURER PART NUMBER	COMPONENT DESCRIPTION	QUANTITY PER	UM	UNIT SALES PRICE	TOTAL SALES PRICE
3730777	2742	TIL-112	IC TIL-112 OPTOCOUPLER	1	EA	1.89	1.89
3730819	2742	XR-2206CP	IC XR-2206CP VCO WAVE GEN	1	EA	11.13	11.13
3730827	2742	XR-2211CP	IC XR-2211CP FSK MODEM	1	EA	13.30	13.30
3730868	2742	MOC-8030	IC MOC-8030 OPTICAL ISOLATOR	4	EA	2.63	10.52
3730876	2733	TL072A	IC DUAL OP-AMP	1	EA	5.60	5.60

TOTAL PRICE 451.99