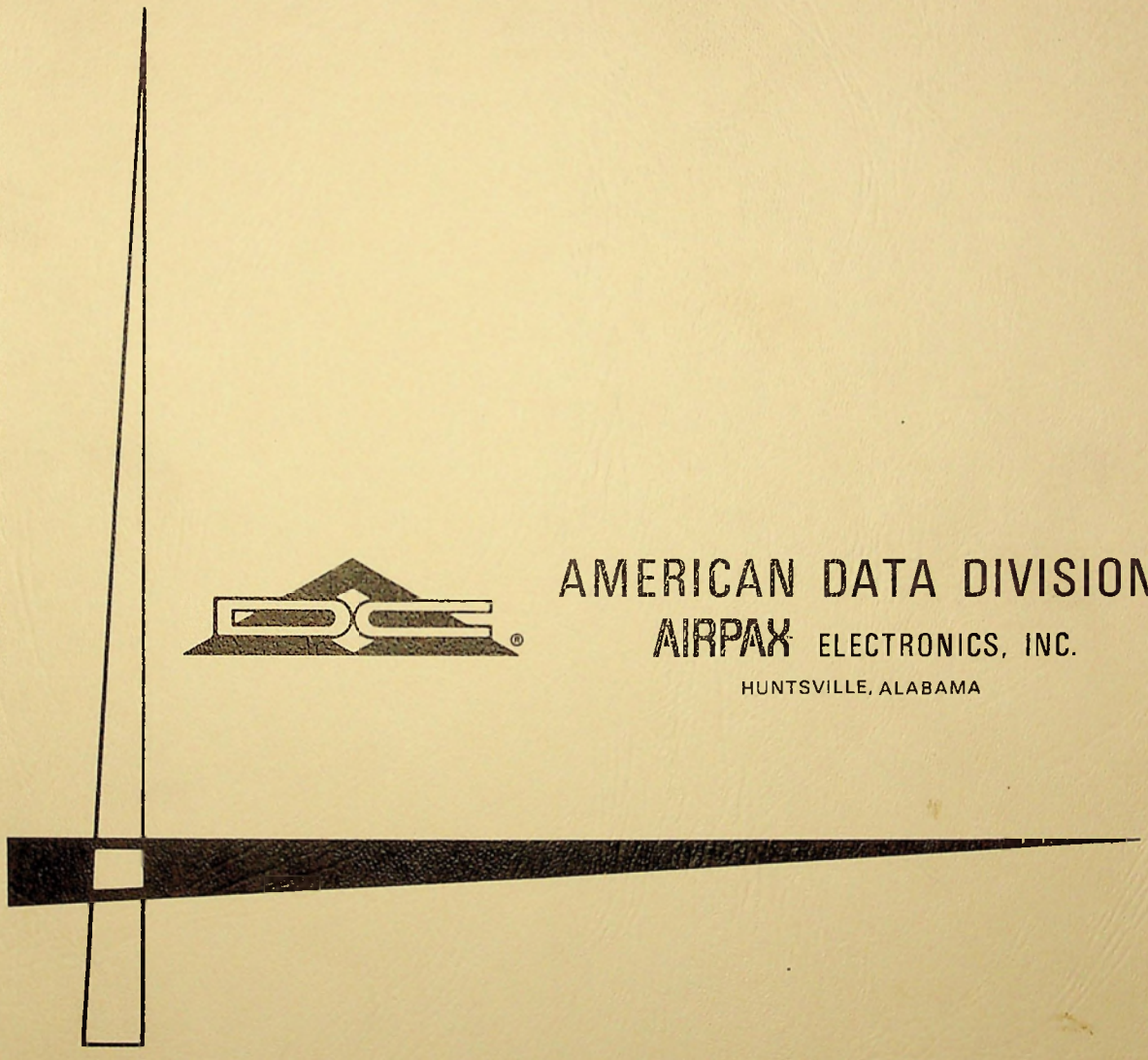
MATRIX



AMERICAN DATA DIVISION

AIRPAX ELECTRONICS, INC.

HUNTSVILLE, ALABAMA

401 WYNN DRIVE, N.W.
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INSTRUCTION MANUAL

SERIES 900/900E

VIDEO/AUDIO SIGNAL ROUTING SWITCHER

-0-

Stock W/O Authorization #2735

Cy 25 of 25

AMERICAN DATA DIVISION
AIRPAX ELECTRONICS, INC.

401 WYNN DRIVE • P. O. BOX 5228 • HUNTSVILLE, ALABAMA 35805 USA • TELEPHONE 205 837-5180 • TWX 810 726-2125

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SECTION 1 - INTRODUCTION

Description

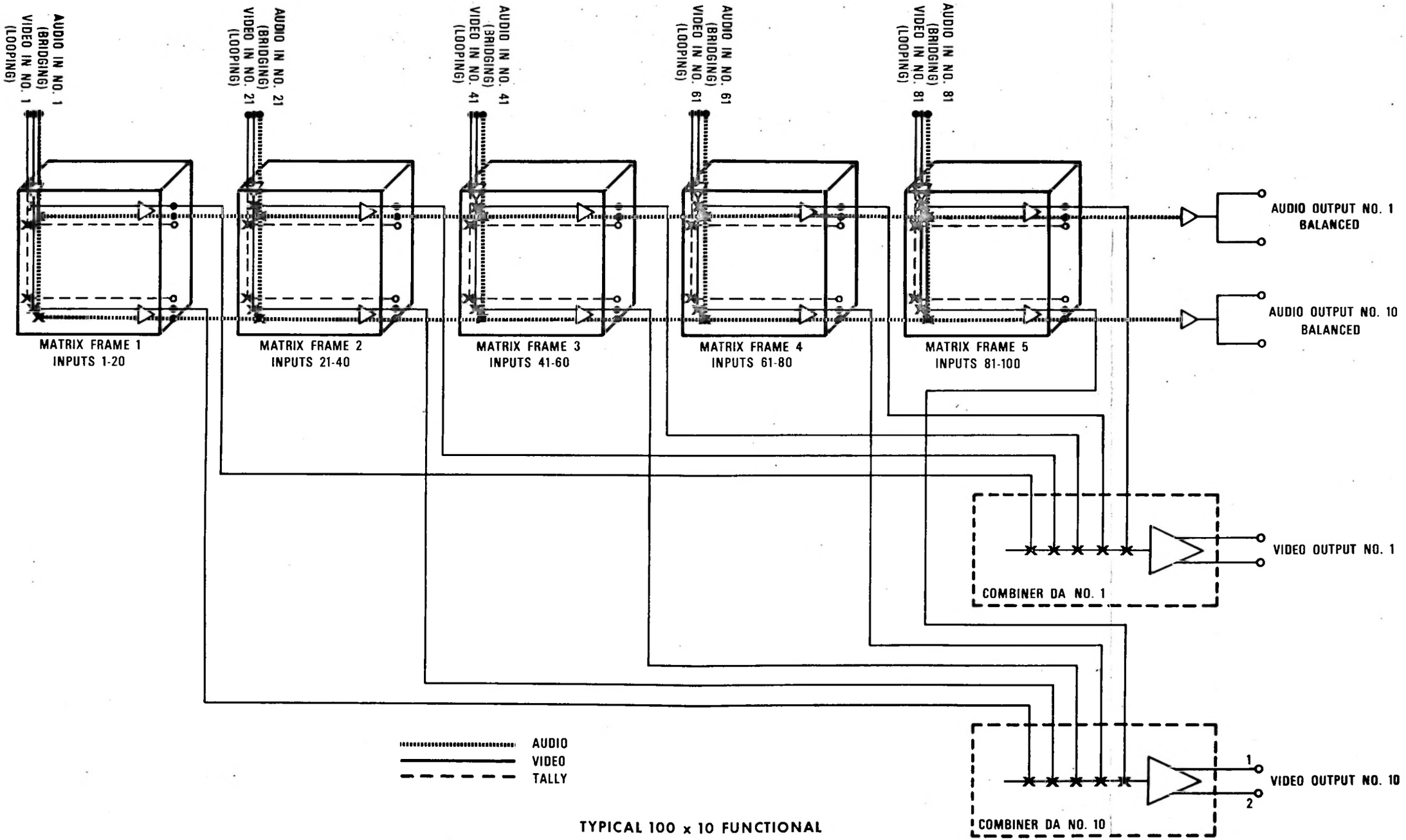
The series 900/900E matrix frame is a video-audio-tally routing switcher with up to twenty inputs and up to ten outputs per frame assembly. Frame assemblies are combined horizontally by means of combiner amplifiers to create routing systems larger than 20 x 10. High input impedance and a low reflection factor allow more than one box to be looped through vertically to form 20 x 20's, 20 x 30's, etc. Up to ten frames can be tied together vertically to provide a 1 x 100 configuration. A typical 100 x 10 configuration is shown in the block diagram, "Typical 100 x 10 Functional".

Video input and output connections are made through BNC connectors located on the back plane of the routing switcher. Audio input and output connections are made through AMP multipin connectors with press lock retaining mechanisms. Control inputs, tally outputs and power inputs are also made through AMP connectors on the back plane with press lock retaining mechanisms.

The fundamental 20 x 10 series 900/900E matrix is controllable by one 16-bit BCD word, or by individual bus 8-bit BCD words, or by 20 discrete control lines for each output bus. ADC offers a number of control methods for the matrix or a number of matrices. Details on controls are normally contained in the systems manual and in the individual control instruction manual.

For matrix arrangements of 20 x 20 and smaller, ADC normally supplies a standard ADC Model 501 power supply. For larger matrix arrangements, purchased Lambda, Hewlett-Packard, or equivalent supplies are provided. In the case of purchased supplies, the manufacturer's standard manual will be supplied.

The basic series 900/900E matrix frame is 10.5 inches high and mounts in a standard 19 inch relay rack. Each matrix frame contains up to twenty 1 x 10 audio/video crosspoint cards and up to ten audio/video output amplifiers. These cards can be easily removed for maintenance or replacement and can generally be moved to other locations in the matrix with very little effect on system performance.



TYPICAL 100 x 10 FUNCTIONAL

SECTION 2 - INSTALLATION

General

The series 900/900E audio/video routing switcher is carefully inspected, tested and calibrated before shipment to insure years of stable, trouble-free service. Each frame requires 10.5 inches of vertical space in a standard 19 inch relay rack. No special cooling requirements are necessary since it was designed to operate in a temperature range from 0^{o} to 50^{o} C. However, care should be taken to prevent an excessive ambient heat rise in closed, unventilated equipment racks. This is especially true if this equipment is installed in the same rack with vacuum tube equipment.

Inspection

Immediately upon receipt, inspect the packing boxes or crates for external signs of abusive handling. If such a condition is noted, notify the carrier immediately. If no external damage is visible, remove the packing material from around the matrix frame(s), control panel(s) and power supplies. Inspect to see that all PC boards are installed properly in their respective connectors and are securely fastened. Make a check of all equipment for any visible damage which may have occurred during transit.

Unpacking, Damage and Shipping

While unpacking and checking the various modules against the packing list, you may find it to your advantage to mount them in the equipment rack as you progress. The cable layout supplied must be utilized so that cable lengths will be long enough.

CAUTION

Do not interchange or substitute coax cables as marked. System timing will be affected.

Any variation from the specified inventory should be reported to ADC immediately. Write to: American Data Corporation, 401 Wynn Drive NE, P. O. Box 5228, Huntsville, Alabama 35805. If shipment damage is incurred, obtain a report from your express

agent or trucker and mail it to the address indicated earlier. Do not return damaged parted until instructed to do so by ADC.

If electronic units must be returned for service, tag them with your name, complete address, and exact description of difficulties encountered. Use original shipping cartons, if possible. If they are not available, wrap the unit in heavy paper before placing it in a carton which should be large enough to permit the use of at least three inches of shredded paper or excelsior between all sides of the unit and the carton. Mark the carton FRAGILE and clearly address it as shown earlier. Include your own name and address on the carton and ship by prepaid express. The unit will be returned express collect. Bear in mind that the carrier will disclaim responsibility for damage if, in his opinion, it was caused by improper packing.

Power Requirements

AC voltage - 105 to 125 volts ac, 60 Hz or 200 to 240 volts ac, 50 Hz (on special order). The equipment is normally wired for ac supply voltages of 105 to 125 volts (117 volts ac nominal), 50 to 60 Hz, unless otherwise specified. Current limiting is used on all the dc outputs providing brief short-circuit protection. Primary ac is fused against excessive current drains.

A three wire ac plug is provided for protection against accidental power shorts to chassis. In no case should the three wire plug be removed or tampered with.

Installation

The series 900/900E Routing Switchers are available in many configurations, making it impossible to include all installation directions in the instruction manual. A system connection diagram will be supplied for systems having more than one matrix frame. Care must be exercised in following instructions for system connections since system timing can be dramatically affected by intermixing video cables. Standard "good commerical practices" should be used in cabling, service loops, cable supports, etc. Should any difficulty be encountered with the installation or during initial system tests, please contact ADC immediately.

After you have completed visual inspection and installation of the equipment, ADC suggests that you apply a 1 volt p-p signal to

all video inputs and an 8 dBm audio signal to all audio inputs, then switch each input (audio and video) to each output. This will functionally test all the control logic, each crosspoint (audio and video) and all output amplifiers. Do not attempt to adjust GAIN, PHASE or RESPONSE controls at this time. In the event that a discrepancy is noted, make a note of it and follow the maintenance procedure given in Section 6 of this instruction manual.

SECTION 3 - SPECIFICATIONS

Electrical

Power - ac	105 - 125 volts ac, 50 - 60 Hz or 200 - 240 volts ac, 45 - 55 Hz (on order)
Power - dc	+12 volts dc battery (optional) to keep the crosspoints latched in the event of power failure.

Video

Input

Signal level	1 volt p-p video
Impedance	50 K ohm - bridging
Return loss	Greater than 45 dB to 5 MHz
Number of inputs	Up to 20 per bus (basic frame) audio/video

Output

Level	1 volt p-p
Impedance	75 ohms
Number of outputs per bus	Two
Isolation between outputs	Greater than 36 dB to 4.2 MHz
Level difference	Less than 1%
DC on output	Less than 0.05 volts
Frequency response	±0.1 dB to 5 MHz ±0.5 dB to 8 MHz Less than -1.0 dB at 10 MHz

Hum (peak to peak)	Greater than 60 dB below output
Bounce (10% - 90% APL)	Less than 0.1 volt
Gain	Nominal - unity, adjustable ±3 dB
Linear chroma distortion (MOD 20T pulse, 1/2 line pulse)	±0.1 dB relative chroma level ±10 ns relative chroma time
Line tilt	Less than 0.5%
Field tilt	Less than 1.0%
Differential gain (10% - 90% APL)	Less than 0.5%
Differential phase (10% - 90% APL)	Less than 0.5°
Maximum axis shift	Less than 0.1 volt
Amplitude stability	Less than 0.1% for ±10% line voltage change Less than 0.25% for 24 hours
Switching time	Less than 0.1 sec
Crosstalk	Greater than 60 dB at 3.58 MHz Greater than 56 dB at 4.43 MHz
Path length accuracy (all inputs to any output)	±1.0° (3.58 MHz or 4.43 MHz)

Audio

Input

Signal level	-10 to +18 dBm, +8 dBm nominal
Impedance	600 ohms balanced or high impedance bridging

Number of inputs	Up to 20 per bus
Output	
Signal level	+8 dBm nominal, +18 dBm maximum
Number of outputs	One
Impedance	600 ohms balanced
Frequency response (reference 1 kHz)	±0.5 dB, 20 Hz to 20 kHz
Harmonic distortion (+18 dBm output)	Less than 0.5% from 20 Hz to 20 kHz
Signal-to-noise ratio (20 Hz to 20 kHz)	Greater than 75 dB below +18 dBm output
Gain	20 dB nominal
Switching time	Less than 0.1 sec
Crosstalk (20 Hz to 20 kHz)	Greater than 70 dB below +18 dBm
Common mode rejection	Greater than 60 dB at 60 Hz
Maximum common mode voltage	24 volts p-p
Environmental	
Operating temperature range	0° to $+60^{\circ}$ C
Storage temperature range	-20° to $+70^{\circ}$ C
Control	
Control voltage (ON)	Momentary single pole closure to matrix ground (2.5 mA)
Control voltage (OFF)	+5 volts dc

900E Specifications

The series 900E is configured identically to the professional series. System specifications are reduced on the following parameters to:

Crosstalk (3.58 or 4.43 MHz)	Greater than 50 dB
Differential phase (10% to 90% APL)	Less than 1^{o}
Differential gain (10% to 90% APL)	Less than 1%
Path length accuracy	Within $\pm 2^{o}$
Signal-to-noise ratio	Greater than -52 dB
Audio frequency response	$\pm$1 dB (20 Hz to 20 kHz)
Audio distortion	Less than 1% (20 Hz to 20 kHz)
Audio signal-to-noise ratio	Greater than -65 dB below +18 dBm
Audio crosstalk	Greater than -60 dB below +18 dBm

SECTION 4 - REFERENCE DATA

VIDEO LEVELS

Composite Video Level	140 IEEE Units	1.0	V p-p
Picture Signal	90 IEEE Units	0.642	V p-p
	92.5 IEEE Units	0.66	V p-p
Set Up	10 IEEE Units	0.0714	V p-p
	7.5 IEEE Units	0.0535	V p-p
Synchronizing Pulses	40 IEEE Units	0.285	V p-p

DB VOLTAGE RATIO AS RELATED TO IEEE UNITS AND PERCENTAGE

IEEE Units Down From 140 Units	dB Down	% Down From 100 Units	dB Down
2	0.1	1%	0.08
5	0.3	2%	0.17
10	0.7	3%	0.25
15	1.0	4%	0.34
20	1.4	5%	0.42
30	2.1	10%	0.90
40	2.9	15%	1.4
50	3.8	20%	1.93
60	4.8	25%	2.5
70	6.0	30%	3.04
80	7.4	40%	4.40
90	8.9	50%	6.02
100	10.9	60%	8.0
110	13.4	70%	10.4
120	16.9	80%	14.0
130	22.9	90%	20.0

PROPAGATION DELAY THROUGH COAXIAL CABLE

Velocity of Propagation (VP) in solid polyethylene dielectric coaxial cable is 66% of velocity in free space. This is equal to 7.874 inches per nanosecond, 20.000 cm per nanosecond. Practical figures are:

8" (20 cm) coaxial cable = 1 nanosecond
6" (15.4 cm) coaxial cable = 1° at 3.58 MHz
T at 3.58 MHz = 279 nanoseconds
T per degree at 3.58 MHz = 0.77 nanosecond

1 nsec	=	1.28°	=	7.9"	(20 cm)
2 nsec	=	2.56°	=	15.7"	(40 cm)
3 nsec	=	3.84°	=	23.6"	(60 cm)
4 nsec	=	5.12°	=	31.5"	(80 cm)
5 nsec	=	6.40°	=	39.4"	(1 m)
6 nsec	=	7.68°	=	47.2"	(1.2 m)
7 nsec	=	8.96°	=	55.1"	(1.4 m)
8 nsec	=	10.24°	=	63.0"	(1.6 m)
9 nsec	=	11.52°	=	70.9"	(1.8 m)
10 nsec	=	12.80°	=	78.7"	(2.0 m)

1	=	0.775 nsec	=	6.1"	(15.4 cm)
5	=	3.875 nsec	=	30.3"	(77.0 cm)
10	=	7.75 nsec	=	60.6"	(1 m 54.0 cm)
15	=	11.625 nsec	=	7' 6.9"	(2 m 31.0 cm)
20	=	15.50 nsec	=	10' 1.3"	(3 m 8.0 cm)
25	=	19.375 nsec	=	12' 7.6"	(3 m 85.0 cm)
30	=	23.25 nsec	=	15' 1.9"	(4 m 62.0 cm)
60	=	46.50 nsec	=	30' 3.8"	(9 m 24.0 cm)
90	=	69.75 nsec	=	45' 5.7"	(13 m 86.0 cm)
180	=	139.50 nsec	=	90' 11.3"	(27 m 72.0 cm)
270	=	209.25 nsec	=	136' 5.0"	(41 m 58.0 cm)
360	=	279.00 nsec	=	181' 10.7"	(55 m 44.0 cm)

ADC CROSSPOINT
TYPE I

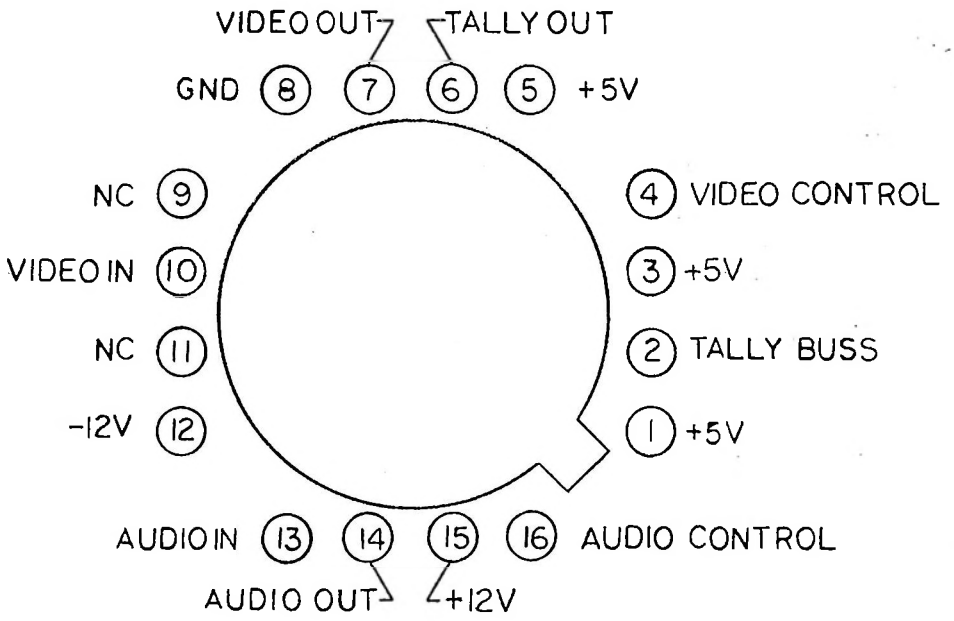


Fig. 4-1
HYBRID CROSSPOINT

A D C CROSSPOINT
TYPE II

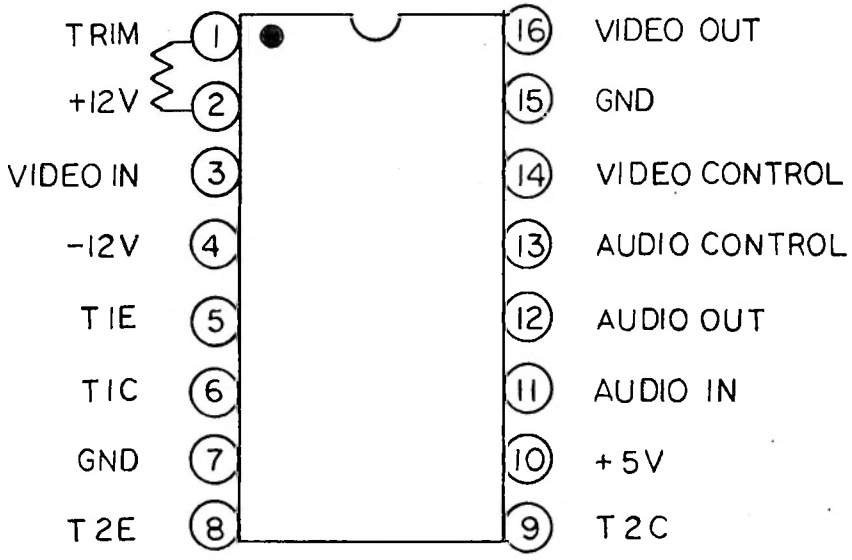


Fig. 4-2
MONOLITHIC CROSSPOINT

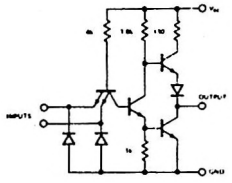
QUADRUPLE 2-INPUT POSITIVE NAND GATE

S5400–A,F,W • N7400–A,F

DIGITAL 54/74 TTL SERIES

S5400 N7400

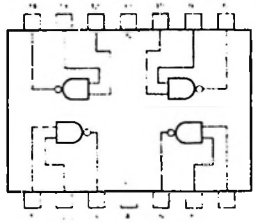
SCHEMATIC (each gate)



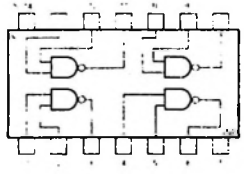
NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



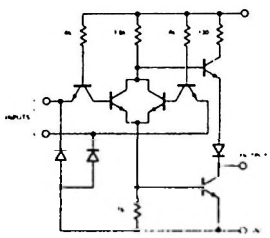
RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5400 Circuits		4.5	5	5.5	V
N7400 Circuits		4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S5400 Circuits	-55	25	125	C
	N7400 Circuits	0	25	70	C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 level at output	V_{CC} = MIN			2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 level at output	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -400μA	V_{in} = 0.8V,		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16mA	V_{in} = 2V,			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX		S5400	-20		-55	mA
				N7400	-18		-55	

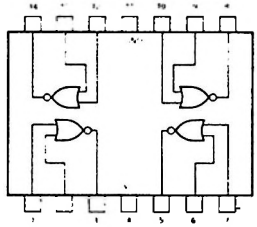
SCHEMATIC (each gate)



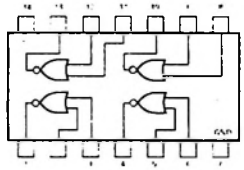
NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



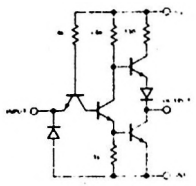
RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S5402 Circuits	4.5	5	5.5	V
	N7402 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S5402 Circuits	-55	25	125	°C
	N7402 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at either input terminal to ensure logical 0 level at output	V_{CC} = MIN			2			V
$V_{in(0)}$	Logical 0 input voltage required at both input terminals to ensure logical 1 level at output	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -400μA	V_{in} = 0.8V		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16mA	V_{in} = 2V,			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output Current†	V_{CC} = MAX		S5402	-20		-55	mA
				N7402	-18		-55	

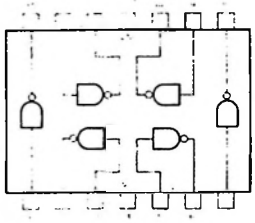
SCHEMATIC (each inverter)



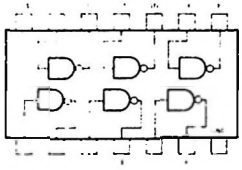
NOTE Component values shown are nominal

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S5404 Circuits	4.5	5	5.5	V
	N7404 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output, N				10	
Operating Free-Air Temperature Range, T_A:	S5404 Circuits	-55	25	125	°C
	N7404 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 level at output	V_{CC} = MIN			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -400μA	V_{in} = 0.8V,		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16mA	V_{in} = 2V,			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 level input current	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX		S5404	-20		-55	mA
				N7404	-18		-55	

BCD-TO-DECIMAL DECODER/DRIVER WITH OPEN COLLECTOR HIGH VOLTAGE OUTPUTS

S5445–F,W • S54145–F,W • N7445–B • N74145–B

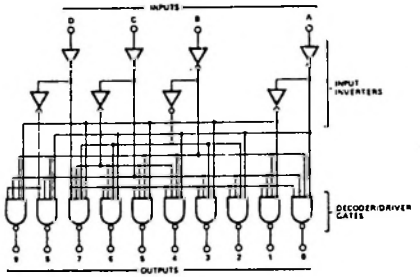
DIGITAL 54/74 TTL SERIES

S5445
S54145
N7445
N74145

DESCRIPTION

The 54/7445 and 54/74145 BCD-to-Decimal Decoder/Driver is a TTL MSI array. It features standard TTL inputs and high voltage, high current (80mA) outputs. The 54/7445 minimum output breakdown is 30 volts and the 54/74145 minimum output breakdown is 15 volts.

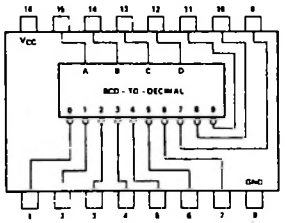
LOGIC DIAGRAM



NOTE: 1. These voltage values are with respect to network ground terminal.

PIN CONFIGURATIONS

B,F,W PACKAGE



TRUTH TABLE

INPUTS			
D	C	B	A
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

OUTPUTS									
0	1	2	3	4	5	6	7	8	9
0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1
1	1	1	1	0	1	1	1	1	1
1	1	1	1	1	0	1	1	1	1
1	1	1	1	1	1	0	1	1	1
1	1	1	1	1	1	1	0	1	1
1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1):	S5445, S54145 Circuits	4.5	5	5.5	V
	N7445, N74145 Circuits	4.75	5	5.25	V
Voltage on any Output	S5445, N7445 Circuits			30	V
	S54145, N74145 Circuits			15	V

TYPES SN5442A THRU SN5444A, SN54L42 THRU SN54L44, SN7442A THRU SN7444A, SN74L42 THRU SN74L44 4-LINE-TO-10-LINE DECODERS (1-OF-10)

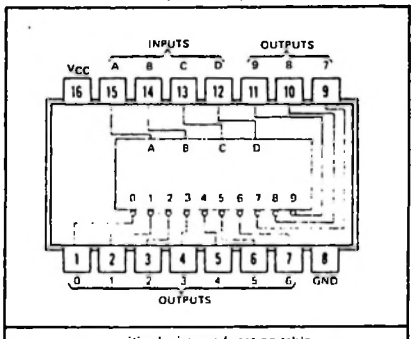
BULLETIN NO. DL-S 7211861, DECEMBER 1972

'42A, 'L42 . . . BCD-TO-DECIMAL
'43A, 'L43 . . . EXCESS-3-TO-DECIMAL
'44A, 'L44 . . . EXCESS-3-GRAY-TO-DECIMAL

- Also for Application as
  - 4-Line-to-16-Line Decoders
  - 3-Line-to-8-Line Decoders
- Diode-Clamped Inputs

TYPES	TYPICAL POWER DISSIPATION	TYPICAL PROPAGATION DELAYS
'42A, '43A, '44A	140 mW	17 ns
'L42, 'L43, 'L44	70 mW	49 ns

SN54'/SN74' . . . J, N, OR W PACKAGE
SN54L'/SN74L' . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The '42A and 'L42 BCD-to-decimal decoders, the '43A and 'L43 excess-3-to-decimal decoders, and the '44A and 'L44 excess-3-gray-to-decimal decoders feature familiar transistor-transistor-logic (TTL) circuits with inputs and outputs which are compatible for use with other TTL and DTL circuits. D-c noise margins are typically one volt.

The 'L42, 'L43, 'L44 decoders are designed specifically for power-critical or battery-operated systems. The '42A, '43A, and '44A decoders are intended for higher-performance systems, especially new designs, where power is not critical. For ultra-high performance and/or speed-critical memory decoders, the SN54S138/SN74S138 and SN54S139/SN74S139 are recommended.

FUNCTION TABLE

NO.	'42A, 'L42 BCD INPUT				'43A, 'L43 EXCESS-3-INPUT				'44A, 'L44 EXCESS-3-GRAY INPUT				ALL TYPES DECIMAL OUTPUT									
	D	C	B	A	D	C	B	A	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	L	H	H	L	L	H	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	L	H	L	L	L	H	H	L	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	L	H	H	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	L	H	H	H	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	L	L	L	H	H	L	L	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	L	H	L	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	L	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level

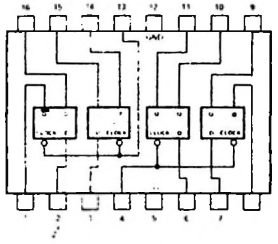
DESCRIPTION

The S5475B/N7475B is a monolithic, quadruple, bistable latch with complementary Q and $\bar{Q}$ outputs. Information present at a data (D) input is transferred to the Q output when the clock is high, and the Q output will follow the data input as long as the clock remains high. When the clock goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the clock is permitted to go high.

This latch is ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units.

PIN CONFIGURATIONS

B PACKAGE



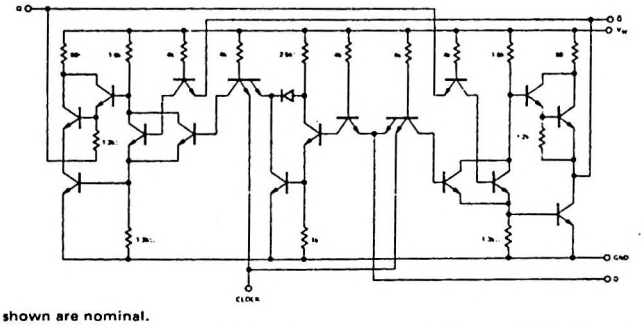
TRUTH TABLE

LOGIC

(Each Latch)		
t_n	t_{n+1}	
D	Q	$\bar{Q}$
1	1	0
0	0	1

NOTES:
1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.
3. These voltages are with respect to network ground terminal.

SCHEMATIC (each latch)



NOTE: Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 3):	S5475 Circuits	4.5	5	5.5	V
	N7475 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Outputs				10	
Operating Free-Air Temperature Range, T_A:	S5475 Circuits	-55	25	125	°C
	N7475 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 level at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 level at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -400μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA			0.4	V

DESCRIPTION

This monolithic TTL monostable multivibrator features d-c triggering from positive or gated negative-going inputs with inhibit facility. Both positive and negative-going output pulses are provided with full fan-out to 10 normalized loads.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry for the B input allows jitter-free triggering from inputs with transition times as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions on the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse lengths may be varied from 40 nanoseconds to 40 seconds by choosing appropriate timing components. With no external timing components (i.e., pin (9) connected to pin (14), pins (10), (11) open) an output pulse of typically 30 nanoseconds is achieved which may be used as a dc triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

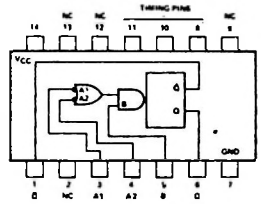
Jitter-free operation is maintained over the full temperature and V_{CC} range for more than six decades of timing capacitance (10 pF to 10μF) and more than one decade of timing resistance (2kΩ to 40kΩ). Throughout these ranges, pulse width is defined by the relationship $t_{p(out)} = C_T R_T \log_e 2$.

Circuit performance is achieved with a nominal power dissipation of 90 milliwatts at 5 volts (50% duty cycle) and a quiescent dissipation of typically 65 milliwatts.

Duty cycles as high as 90% are achieved when using R_T = 40kΩ. Higher duty cycles are achievable if a certain amount of pulse-width jitter is allowed.

PIN CONFIGURATIONS

A,F PACKAGE



TRUTH TABLE

t_n INPUT			t_{n+1} INPUT			OUTPUT
A1	A2	B	A1	A2	B	
1	1	0	1	1	1	Inhibit
0	X	1	0	X	0	Inhibit
X	0	1	X	0	0	Inhibit
0	X	0	0	X	1	One Shot
X	0	0	X	0	1	One Shot
1	1	1	X	0	1	One Shot
1	1	1	0	X	1	One Shot
X	0	0	X	1	0	Inhibit
0	X	0	1	X	0	Inhibit
X	0	1	1	1	1	Inhibit
0	X	1	1	1	1	Inhibit
1	1	0	X	0	0	Inhibit
1	1	0	0	X	0	Inhibit

1 = $V_{in(1)} \geq 2V$ 0 = $V_{in(0)} \leq 0.8V$

1. A1 and A2 are negative-edge-triggered logic inputs, and will trigger the one shot when either or both go to logical 0 with B at logical 1.
2. B is a positive Schmitt-trigger input for slow edges or level detection, and will trigger the one shot when B goes to logical 1 with either A1 or A2 at logical 0. (See Truth Table)
3. External timing capacitor may be connected between pin (10) (positive) and pin (11). With no external capacitance, an output pulse width of 30ns is obtained typically.
4. To use the internal timing resistor (2kΩ nominal), connect pin (9) to pin (14).
5. To obtain variable pulse width connect external variable resistance between pin (9) and pin (14). No external current limiting is needed.
6. For accurate repeatable pulse widths connect an external resistor between pin (11) and pin (14) with pin (9) open-circuit.
7. t_n = time before input transition.
8. t_{n+1} = time after input transition.
9. x indicates that either a logical 0 or 1, may be present.

4-LINE TO 16 LINE DECODER/DEMULTIPLEXER

S54154
N74154

S54154–N,Q,F • N74154–N

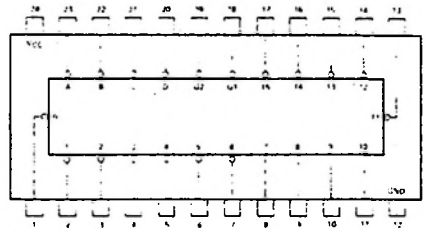
DIGITAL 54/74 TTL SERIES

DESCRIPTION

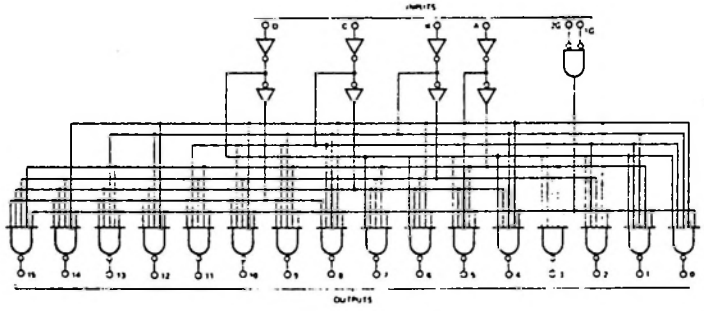
The 54/74154 decodes 4 binary-coded inputs to one of 16 mutually exclusive outputs when each of the two strobe inputs are low. The demultiplexing function is achieved by using the 4 input lines for output addressing and data from one strobe input while the other strobe input is held low.

PIN CONFIGURATIONS

N,Q,F PACKAGE



LOGIC DIAGRAM



TRUTH TABLE

INPUTS						OUTPUTS															
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High, L = Low, X = Irrelevant

TYPES SN54173, SN74173
4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS

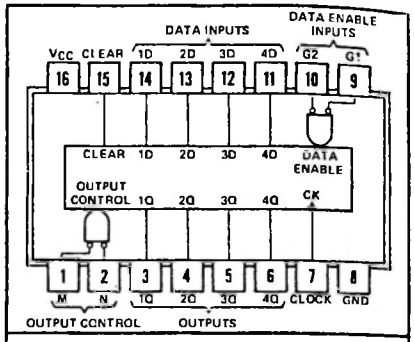
BULLETIN NO. DL-S 7211721, MAY 1972 REVISED DECEMBER 1972

- Three-State Outputs Interface Directly with System Bus
- Gated Output-Control Lines for Enabling or Disabling the Outputs
- Fully Independent Clock Virtually Eliminates Restrictions for Operating in One of Two Modes:

  Parallel Load
  Do Nothing (Hold)

- Average Propagation Delay . . . 23 ns Typical
- Maximum Clock Frequency . . . 35 MHz Typical
- Power Dissipation . . . 250 mW Typical
- For Application as Bus Buffer Registers

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)



positive logic: see function table

description

The SN54173 and SN74173 four-bit registers include D-type flip-flops featuring totem-pole three-state outputs capable of driving highly capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these flip-flops with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. For applications not requiring three-state outputs, the SN54174 or SN74174 hex D-type flip-flop can be used for a 33% reduction in package count and a 40% reduction in power, or the SN54175 or SN74175 quadruple D-type flip-flop can be used for a similar reduction in power.

Gated enable inputs are provided on the SN54173 and SN74173 for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gate output control inputs are also provided. When both are low, the normal logic states (high or low levels) of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the function table.

FUNCTION TABLE

INPUTS					OUTPUT
CLEAR	CLOCK	DATA ENABLE G1	DATA ENABLE G2	DATA D	Q
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however sequential operation of the flip-flops is not affected.

H = high level (steady state)
L = low level (steady state)
↑ = low-to-high-level transition
X = irrelevant (any input including transitions)
Q_0 = the level of Q before the indicated steady-state input conditions were established.

Rated at −5.2 mA high-logic-level drive current, up to 128 of the SN74173 outputs may be connected to a common bus and still drive two Series 54/74 TTL normalized loads. Similarly, up to 49 of the SN54173 outputs can be connected to a common bus and drive one additional Series 54/74 TTL load. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times by 10 nanoseconds. The SN54173 and SN74173 are guaranteed to accept clock input frequencies up to 25 MHz.

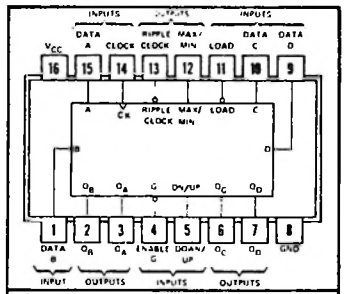
TYPES SN54190, SN54191, SN54LS190, SN54LS191, SN74190, SN74191, SN74LS190, SN74LS191
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

BULLETIN NO. DL-S 7211865, DECEMBER 1972

- Counts 8-4-2-1 BCD or Binary
- Single Down/Up Count Control Line
- Count Enable Control Input
- Ripple Clock Output for Cascading
- Asynchronously Presettable with Load Control
- Parallel Outputs
- Cascadable for n-Bit Applications

TYPE	AVERAGE PROPAGATION DELAY	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'190, '191	20 ns	25 MHz	325 mW
'LS190, 'LS191	20 ns	25 MHz	90 mW

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)



asynchronous inputs: Low input to load sets Q_A=A, Q_B = B, Q_C = C, and Q_D = D

description

The '190, 'LS190, '191, and 'LS191 are synchronous, reversible up/down counters having a complexity of 58 equivalent gates. The '191 and 'LS191 are 4-bit binary counters and the '190 and 'LS190 are BCD counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The clock, down/up, and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Series 54' and 54LS' are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74' and 74LS' are characterized for operation from 0°C to 70°C.

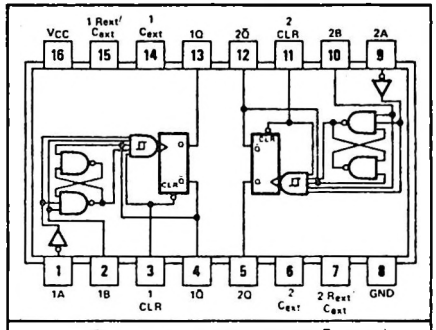
TYPES SN54221, SN54LS221, SN74221, SN74LS221
DUAL MONOSTABLE MULTIVIBRATORS
WITH SCHMITT-TRIGGER INPUTS

BULLETIN NO. DL-S 7412027, MARCH 1974

- SN54221, SN54LS221, SN74221 and SN74LS221 Are Dual Versions of Highly Stable SN54121, SN74121 One-Shots on a Monolithic Chip
- Pulse-Width Variance Is Typically Less than ±0.5% for 98% of the Units
- SN54221 and SN74221 Demonstrate Electrical and Switching Characteristics That Are Virtually Identical to the SN54121, SN74121 One-Shots
- Pin-Out Is Identical to the SN54123 SN74123, SN54LS123, SN74LS123
- Overriding Clear Terminates Output Pulse

TYPE	TYPICAL POWER DISSIPATION	MAXIMUM OUTPUT PULSE LENGTH
SN54221	130 mW	21 s
SN74221	130 mW	28 s
SN54LS221	23 mW	49 s
SN74LS221	23 mW	70 s

SN54221, SN54LS221 . . . J OR W PACKAGE
SN74221, SN74LS221 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: Low input to clear resets Q low and Q̄ high regardless of d-c levels at A or B inputs.

description

The '221 and 'LS221 are monolithic dual multivibrators with performance characteristics virtually identical to those of the '121. Each multivibrator features a negative-transition-triggered input and a positive-transition triggered input either of which can be used as an inhibit input.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions of the A and B inputs and are a function of the timing components, or the output pulses can be terminated by the overriding clear. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 35 nanoseconds to the maximums shown in the above table by choosing appropriate timing components. With R_{ext} = 2 kΩ and C_{ext} = 0, an output pulse of typically 30 nanoseconds is achieved which may be used as a d-c-triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length. Typical triggering and clearing sequences are illustrated as a part of the switching characteristics waveforms.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10 pF to 10 μF) and more than one decade of timing resistance (2 kΩ to 30 kΩ for the SN54221, 2 kΩ to 40 kΩ for the SN74221, 2 kΩ to 70 kΩ for the SN54LS221, and 2 kΩ to 100 kΩ for the SN74LS221). Throughout these ranges, pulse width is defined by the relationship: $t_{w(out)} = C_{ext}R_{ext}\ ln2 \approx 0.7\ C_{ext}R_{ext}$. In circuits where pulse cutoff is not critical, timing capacitance up to 1000 μF and timing resistance as low as 1.4 kΩ may be used. Also, the range of jitter-free output pulse widths is extended if V_{CC} is

FUNCTION TABLE
(EACH MONOSTABLE)

INPUTS			OUTPUTS	
CLEAR	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	⎍	⎎
H	↓	H	⎍	⎎
Also see description and switching characteristics				

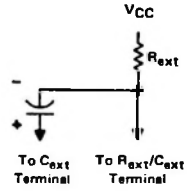
H = high level (steady state)
L = low level (steady state)
↑ = transition from low to high level
↓ = transition from high to low level
⎍ = one high level pulse
⎎ = one low level pulse
X = irrelevant

description (continued)

held to 5 volts and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum recommended R_T. Higher duty cycles are available if a certain amount of pulse-width jitter is allowed.

The variance in output pulse width from device to device is typically less than ±0.5% for given external timing components. An example of this distribution for the '221 is shown in Figure 2. Variations in output pulse width versus supply voltage and temperature for the '221 are shown in Figure 3 and 4, respectively.

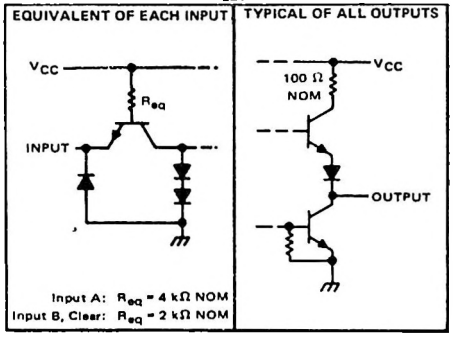
Pin assignments for these devices are identical to those of the SN54123/SN74123 or SN54LS123/SN74LS123 so that the '221 or 'LS221 can be substituted for those products in systems not using the retrigger by merely changing the value of R_{ext} and/or C_{ext}.



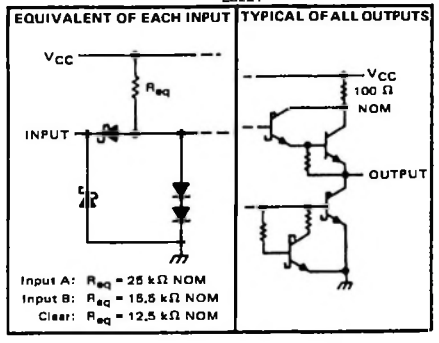
TIMING COMPONENT CONNECTIONS

schematics of inputs and outputs

'221



'LS221



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage:	SN54221, SN74221	5.5 V
	SN54LS221, SN74LS221	7 V
Operating free-air temperature range:	SN54221, SN54LS221	−65°C to 125°C
	SN74221, SN74LS221	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

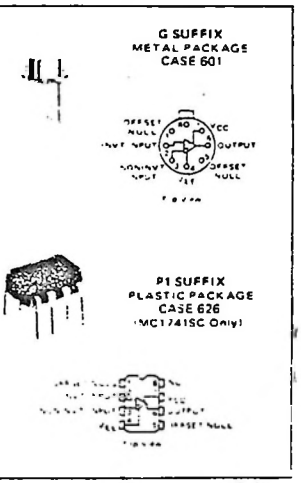
MC1741S
MC1741SC

HIGH SLEW-RATE INTERNALLY-COMPENSATED OPERATIONAL AMPLIFIER

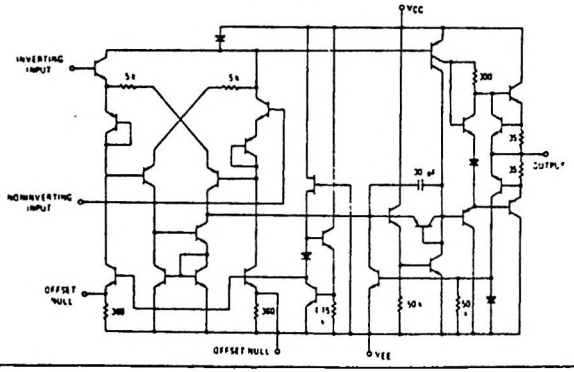
The MC1741S/MC1741SC is functionally equivalent, pin compatible, and possesses the same ease of use as the popular MC1741 circuit, yet offers 20 times higher slew rate and power bandwidth. This device is ideally suited for D-to-A converters due to its fast settling time and high slew rate.

- High Slew Rate — 10 V/μs Guaranteed Minimum
- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch-Up

OPERATIONAL AMPLIFIER
MONOLITHIC SILICON
INTEGRATED CIRCUIT



CIRCUIT SCHEMATIC



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value		Unit
		MC1741SC	MC1741S	
Power Supply Voltage	V_{CC} V_{EE}	+18 -18	+22 -22	Vdc
Differential Input Signal Voltage	V_{in}	±30		Volts
Common-Mode Input Voltage Swing (See Note 1)	V_{ICR}	±15		Volts
Output Short-Circuit Duration (See Note 2)	t_s	Continuous		
Power Dissipation (Package Limitation) Metal Package Derate above T_A = +25°C Plastic Dual In-Line Package Derate above T_A = +25°C	P_D	 680 4.6 625 5.0		 mW mW/°C mW mW/°C
Operating Temperature Range	T_A	0 to +75	-55 to +125	°C
Storage Temperature Range Metal Package Plastic Package	T_{stg}	 -65 to +150 -55 to +125		°C

Note 1. For supply voltages less than ±15 Vdc, the absolute maximum input voltage is equal to the supply voltage.
Note 2. Supply voltage equal to or less than 15 Vdc.

SECTION 5 - CIRCUIT DESCRIPTIONS

1 x 10 Audio/Video Crosspoint Card

Please refer to drawing, 1 x 10 Crosspoint, Monolithic - Model 9101M, Dwg. No. 995 930 0013.

Purpose - The 1 x 10 card buffers and switches the audio input, buffers and switches the video input, and generates both a "row" tally and a "bus" tally output.

Description - A high input impedance (approximately 10 K ohms), differential input, audio amplifier provides over 60 dB of common mode rejection, converts the balanced audio signal to single-ended, and isolates the audio input line from the primary switching system. Resistors R17, R18 and R19 are used to terminate the balanced line. Resistors R24 and R26 can be changed according to the table shown on the reference drawing to vary the gain of the front-end audio amplifier.

A high input impedance (approximately 50 K ohms) video amplifier isolates the switching system from the video input signal which may be looped-through to other matrix boxes or to other equipment. This video amplifier has a gain of approximately 1.6 and functions as a high impedance input, very low output impedance buffer.

Switching of both audio and video is performed by a 16 pin dual-in-line integrated circuit developed by ADC especially for this purpose. Switching is completed when the control line(s) is pulled to matrix ground potential. At this time, two separate tally transistors are activated; one turns on a LED on the card indicating closure and functions as "row" tally output, the second is collector OR'd with corresponding transistors in other crosspoints to form "bus" tally.

Potentiometer R11 provides an approximate $\pm 2^{o}$ phase shift adjustment. With a little care, all paths through the series 900/900E can be phased so that less than $\pm 1^{o}$ of phase error exists between any path through the system.

PMIT: 1/20/77

SYM	ZONE	REVISIONS DESCRIPTION	DATE	APPROVED
	A	ENC PER ECO #420	8/9/76	
	B	ENC PER ECO #495	7/30/76	
	C	ENC PER ECO #534	9/14/76	
	D	ENC PER ECO #567	10/29/76	

LOOPING INPUTS

R19 7.15K
OMIT
R17 7.15K

AUDIO INPUTS

AUDIO GAIN TABLE

GAIN	R24	R26
-12 db	2.5K	2.5K
-6db	5.0K	5.0K
0db	10K	10K
+6db	20K	20K
+12db	40K	40K

TYPICAL 23 THUR 512

TALLY OUT CONTROL AUDIO OUT VIDEO OUT +5V TALLY BUSS

D1 5082-4882 R46 20K 1% R49 20K 1% R50 20K 1% R51 20K 1% R52 20K 1% R53 20K 1% R54 20K 1% R55 20K 1% R56 20K 1% R57 20K 1%

D2 1N914 D4 1N914 D6 1N914 D8 1N914 D10 914 D12 1N914 D14 1N914 D16 1N914 D18 1N914 D20 1N914

R31 470Ω R32 470Ω R33 470Ω R34 470Ω R35 470Ω R36 470Ω R37 470Ω R38 470Ω R39 470Ω R40 470Ω

-5 +12 VIDEO IN AUDIO IN

Z3 XP1 0185 Z4 XP2 0185 Z5 XP3 0185 Z6 XP4 0185 Z7 XP5 0185 Z8 XP6 0185 Z9 XP7 0185 Z10 XP8 0185 Z11 XP9 0185 Z12 XP10 0185

C23 47/35 C24 47/35 C27 47/35 C28 4.7/35 R42 121Ω C26 4.7/35

Z1 1741 Q4 2N2222A R71 5K 3329W R70 5.1K R29 2.2K R27 100Ω R72 500Ω 3329P R88 100Ω R24 10K 1% C13 4.7/35 C14 4.7/35

R19 162Ω,1% R18 232Ω 1% R17 162Ω 1% C12 22/15 C11 22/15 R23 10K 1% R25 10K 1% R26 9.76K 1%

-12V

NOTES:
1. R23,24,25,26 NORMAL MATCHED SET 10K,1% (RNS8C)
2. R26 = 9.76K,1% R72, 500Ω SPECIAL ORDER ONLY.
3. USE R71 & R70 ONLY WHEN REQ'D.

+12V R5 100Ω C3 4.7/35 R7 100Ω C6 .1/50 R11 500Ω 3006P R16 10Ω 1% R3 360Ω R4 150Ω C2 10PF R6 5.6K R10 332Ω 1% C8 4.7/35 C5 .1/50 R9 200Ω 1% R8 100Ω C4 18PF

VIDEO INPUT R19 150Ω R44 100Ω R43 51K R45 1.8K R2 .68K Q7 4124 Q1 4126 Q2 4126 Q3 2222A

R13 1.8K R12 2.2K D24 1N914 F15 500Ω 3006P

D23 1N4004 -12V IN R21 1K Q6 2222A C17 22/15 C18 4.7/15

D25 1N4004 -12V TO AUDIO ONLY R20 360Ω Q8 2907A C15 22/15 C16 4.7/35 R46 2K Q9 2907A C21 22/15 C22 4.7/35

AMERICAN DATA DIVISION
AIRPAX ELECTRONICS, INC

SCALE: APPROVED BY: DRAWN BY CAL J.
DATE 27 SEPT 76 REVISED D

MONOLITHIC, 1 X 10 CROSSPOINT

MODEL 9101M DRAWING NUMBER 995 930 0436

Audio/Video Output Amplifier

Please refer to drawing, Schematic, Audio/Video Output Amplifier - Model 9102M, Dwg. No. 995 930 0014.

Purpose - The audio/video output amplifier card provides the audio and video bus current sources (or load resistors). In addition, it provides a high impedance to the bus and a low output impedance.

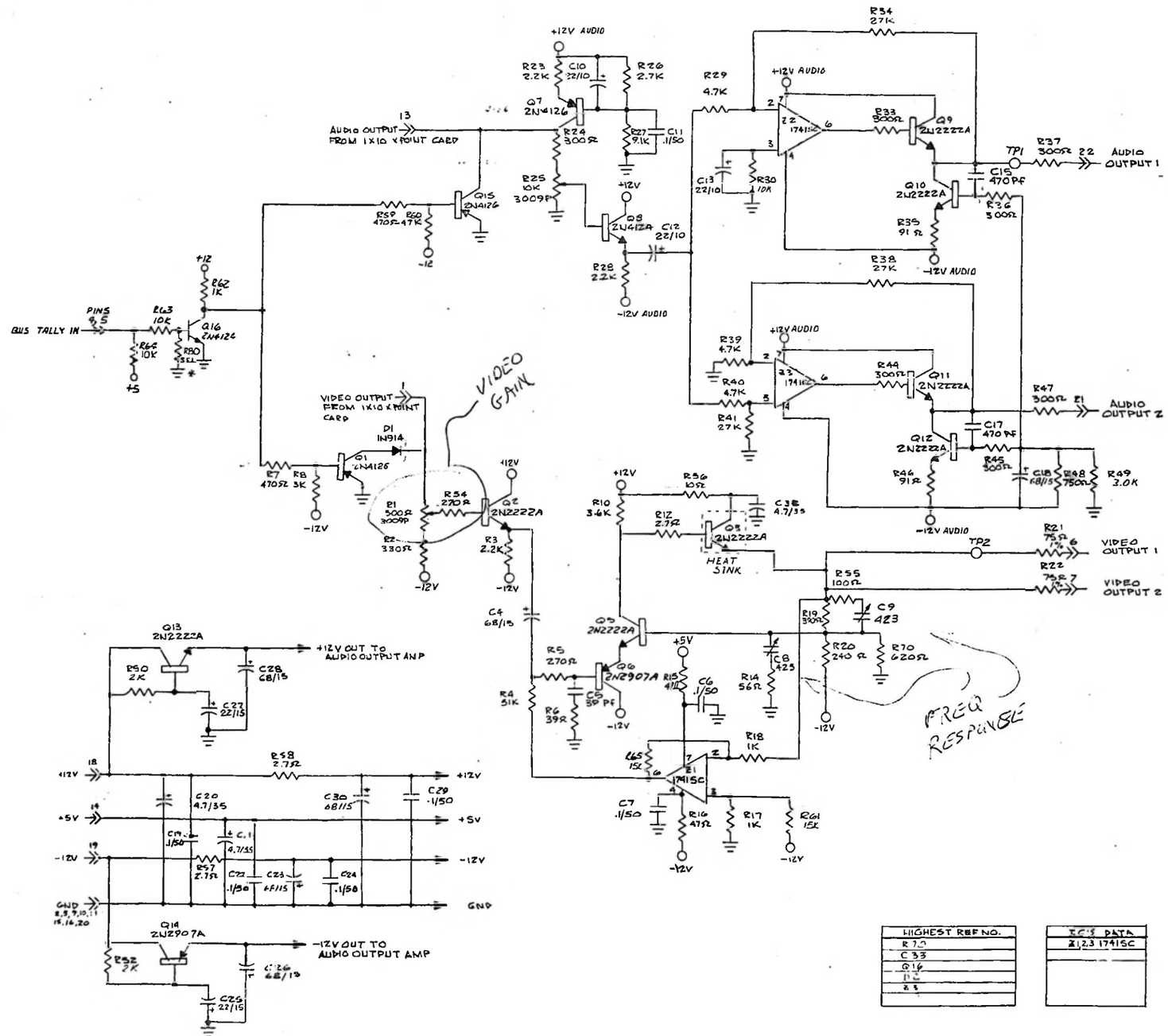
Description - As each crosspoint is turned ON, the audio signal passes through the crosspoint and appears on the collector of Q7, the crosspoint current source. A transistor (Q15) is used as a "blind" crosspoint when there are no crosspoints ON in the bus served by that output amplifier. This prevents "popping" when switching a signal onto this bus. The audio signal on the collector of Q7 is divided by R25 (audio gain control). The integrated circuits Z2 and Z3 generate out-of-phase signal to drive the output transistors Q9 and Q11, which produces a balanced audio output.

The output stage of the ADC designed video crosspoint is an emitter follower whose emitter load is made up of R1 and R2 on the output amplifier. Q1 is a clamping transistor to set the level (dc) at the input to the output amplifier when there are no other crosspoints ON on the bus. Potentiometer R1 is the video GAIN control. The video output amplifier incorporates a dc restoration circuit to maintain the back porch of the composite video signal near ground potential.

The audio amplifier has one balanced, 600 ohm output; the video output amplifier has two 75 ohm, single-ended outputs.

PMT: 1/20/77

REVISIONS			
LTR		DESCRIPTION	DATE	APPROVED
A		INC PER ECO # 554	11-17-76	
B		INC PER ECO # 564	12-7-76	
C		INC PER ECO # 510	7-15-77	
D		INC PER ECO # 583		



HIGHEST REF NO.
R 70
C 33
Q 16
U
R 5

EC'S DATA
21,23 1741SC

NOTE
1. R 70 620Ω IS USED FOR SETTING OVERALL GAIN
2. BUS TALLY IS NOT USED ON SINGLE BOX SYSTEM.
3. WHEN USING AUDIO COMBINER AUDIO OUTPUT 2 IS NOT USED.

COMPANY CONFIDENTIAL

AMERICAN DATA CORPORATION
HUNTSVILLE, ALABAMA

SCALE:	APPROVED BY:	DRAWN BY: ABT
DATE: 12-19-73		REVISED

SCHEMATIC
AUDIO/VIDEO OUTPUT AMP

MODEL 9102M REV D

Matrix Control Logic

Please refer to drawing, Schematic, Rear Panel - Model 9104, Dwg. No. 995 930 0005.

Purpose - The rear panel of the series 900/900E matrix frame contains all the crosspoint control logic. This logic decodes incoming commands and causes the selected crosspoint control line to go to matrix ground.

Description - The series 900/900E matrix is divided into two 10 x 10 sections which ideally lend themselves to control by BCD characters (1-2-4-8). In normal operation, the matrix is set up by a series of 16-bit words made up of four 4-bit characters. These characters are called X-units, X-tens, Y-units and Y-tens. For a 20 x 10 matrix, the X-tens are decoded by Z27 to steer the four bits of X-units data to either the 0 - 9 side or the 10 - 20 side of the matrix. The outputs of Z27 are strappable on each matrix frame so that the units data can be steered in matrices with larger inputs. The matrix frame for inputs 21 - 40 would have straps on the 3 and 4 outputs of Z27.

The X data, of course, controls input while the Y data determines the output. To operate properly, both commands must be present. Y-units are decoded by Z24 to provide ten discrete outputs which gate the X-units data into the latches of the desired output bus. As you can see on the referenced drawing, there are a latch and decoder associated with each ten inputs on each output bus. Once the data is latched, it is decoded into one of ten discrete outputs by the decoder associated with that latch which, in turn, closes the associated crosspoint. Y-tens are decoded by Z25 and the output strapped to identify the matrix frame from an output point of view. Strapping the 1 output of Z25 to pin 19 of Z24, as an example, identifies outputs 1 - 10 and gates only the Y-units commands associated with those outputs to Z24.

A series of ten 16-bit words, therefore, can select the input (1 of 100) desired for each of ten output buses.

In addition to the method of control described above, it is possible, for example, to remove Z11 and install a dual-in-line connector and control the first half of the first bus with any 4-bit latched data. Also, Z1 can be removed and a dual-in-line connector

installed with ten discrete wires which can control the first half of output bus #1. Interlocks would have to be provided in the external control system to prevent turning on more than one crosspoint on a bus.

In normal operation, the control interface unit generates a series of 16-bit words and a strobe which are the command inputs to the series 900/900E matrix frame. The strobe pulse (derived from V-drive) latches the Y-data into Z24 provided, of course, that it is not inhibited by the output of the Y-tens decoder. This provides vertical interval switching for the series 900/900E routing switches.

PMT: 9/17/75

LTR	REVISION	DATE	BY
A	ESC PER ECO # 307	7/12/75	RDS

BCD IN X TENS

BCD IN Y ONES

BCD IN Y TENS

STROBE

X PROGRAM

Y PROGRAM

X UNITS

CONTROLS

IC's DATA	
Z1-Z10,Z27,Z5,41-50	SN7445 or 74L42
Z11-Z20,Z31-Z40	SN7475
Z24	SN74154
Z26	SN74121
Z21,22,23,28,29,30	SN7402
Z51	SN7404
Z52,53	SN7400

HIGHEST REF NO.
R26
C10
Z53
VR2

AMERICAN DATA CORPORATION
HUNTSVILLE, ALABAMA

DRAWN BY: ART

SCHEMATIC REAR PANEL

MODEL 9104

DRAWING NUMBER 9959300009

Control Interface

Please refer to drawing, Strobe Conditioning & Scan Control - Model 9107, Dwg. No. 995 930 0008.

Purpose - The series 900/900E control interface multiplexes inputs from all standard ADC control modules to generate a 16-bit BCD word and strobe pulse to control the series 900/900E matrix.

Description - All information transfer in the control interface is made under the control of one of two clock pulses. The first is a 60 Hz pulse derived from incoming V-drive, which makes all switching occur in the vertical interval. The second clock pulse source is a 60 Hz self-contained oscillator.

A one-shot multivibrator (Z2A) generates a dual clock pulse which first gates new information from the remote control units into the storage registers, then advances the Y-units counter (Z3).

The other side of Z2 (Z2B) creates a strobe pulse from the leading edge of V-drive, which is delayed by an amount determined by R25. This strobe pulse is normally set to occur two to four lines after the vertical sync.

Twenty tri-state 4-bit registers (SN74173's) are arranged in ten sets of 8-bits, which correspond to the ten output buses. Normally, each set of 8-bits represents the input selection (00 to 99) made by each discrete control panel and its associated TAKE button; however, inputs to the control unit may be paralleled for controlling more than a single output from a single control panel. New input select information is stored when a TAKE command and a clock pulse (from Z2A) occur simultaneously.

The Y-units counter also feeds a BCD to the one-of-ten decoder Z4 (SN7445) which controls the output state of the tri-state registers. Each time the Y-units counter advances, a new set of eight X-bits is selected. After a slight delay, the matrix is strobed, entering the new 16-bit control word into the series 900/900E matrix control logic. Each output bus of the matrix is updated every tenth V-drive pulse. This makes the maximum TAKE delay that can occur nine vertical interval periods (9 times 16.6 ms).

PMT: 4/26/76

VERT SYNC PULSE

DUAL CLOCK PULSE

STROBE

+5V DC

FIELD TRIGGER

V.D IN

2270000336

CLOCK 1-5

ENABLE 1-5

ENABLE 6-10

CLOCK 6-10

TO MATRIX STROBE

Y UNITS

'Y' TENS

X TENS

X UNITS

SELECTIVE FEEDTHRU PROGRAMMING OF 'Y' TENS

Z1 7404

Z2 7445

Z3 74190

Z4 7445

Z5 74173

Z6 74173

Z7 74173

Z8 74173

Z9 74173

Z10 74173

Z11 74173

Z12 74173

Z13 74173

Z14 74173

Z15 74173

Z16 74173

Z17 74173

Z18 74173

Z19 74173

Z20 74173

Z21 74173

Z22 74173

Z23 74173

Z24 74173

7417

X TENS 1 X UNITS

X TENS 2 X UNITS

Y TENS 3 X UNITS

Y TENS 4 X UNITS

X TENS 5 X UNITS

X TENS 6 X UNITS

X TENS 7 X UNITS

X TENS 8 X UNITS

Y TENS 9 X UNITS

DCBA TAKE X TENS 10 DCBA X UNITS

X TENS 1 X UNITS

X TENS ( ) X UNITS

Note:
TYPICAL FEED THRU ARRANGEMENT TO ENABLE 1 KEYBOARD TO CONTROL FROM 1 TO 10 INPUTS

PC CARD A321
HIGHEST NUMBER
Q1
Z24
R20
C11
R2 UNUSED

LTR	REVISION	BY	DATE
C	CHANGED PER ECO # 476	TC	4-23-76
B	CHANGED PER ECO # 405	TC	2-13-76
A	ECO # 168	L.D.S	

AMERICAN DATA CORPORATION
HUNTSVILLE, ALABAMA

STROBE CONDITIONING & SCAN CONTROL

MODEL 9107

995 0130-0008

Power Supply

Please refer to drawing, 900 Matrix Power Supply - 900/501, Dwg. No. 999 274 0003.

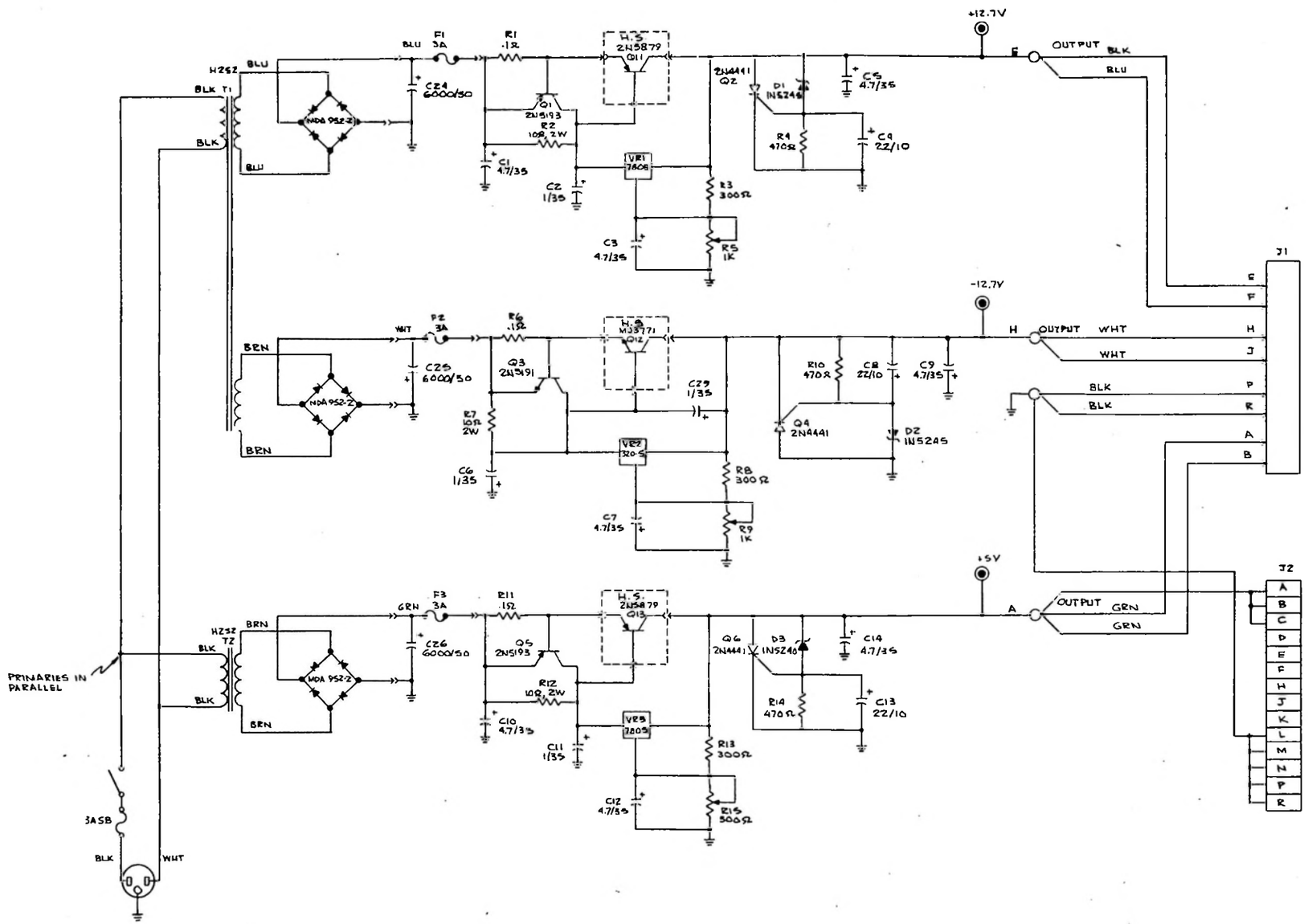
Purpose - ADC provides a standard Model 501 power supply (for systems smaller than 20 x 20) or purchased supplies (Lambda or Hewlett Packard, normally) to supply the +12 volts, -12 volts and +6 volts required by the series 900/900E matrix systems. If your system has purchased supplies, please consult the manufacturer's instruction manual included in the system documentation.

Description - The ADC Model 501 supplies the three voltages (+12, -12, and +6) required by the series 900/900E matrix frame. All three power supplies in the Model 501 are fundamentally the same, therefore, only one will be explained. The rectified, filtered voltage on the plus end of C24 is the unregulated dc source. Fuse F1 protects against catastrophic failure in the event the current limit circuit (R1-Q1) fails to limit current flow. Transistor Q11 and voltage regulator VR1 form a standard voltage regulator. The output voltage can be adjusted by R5. Another safety feature is the "crow-bar" circuit formed by D1-R4-Q2. In the unlikely event that the series regulator fails (shorts), and the output voltage starts to rise, the SCR (Q2) will fire, creating an effective short circuit across the output and causing F1 to blow. Q2 fires when the output voltage exceeds the drop across zener D1 (12 volts) by approximately 2 volts.

Each of the other supplies operates in much the same manner, being comprised of a raw dc supply, fuse, current limiter, series regulator, and an output "crow-bar" circuit.

Each output is metered by a switchable meter circuit.

T: 3/20/75



AMERICAN DATA CORPORATION
- AUTOMATION -

SCALE: —	APPROVED BY:	DRAWN BY ART
DATE 3-24-74		REVISED

900 MATRIX POWER SUPPLY

900/501 — 999274-0063

SECTION 6 - MAINTENANCE

General Data

There are, in general, two aspects to maintaining the series 900/900E matrix and associated controls. These are preventive maintenance and servicing or troubleshooting in the event of failure. All ADC equipment is transistorized, therefore it requires very little preventive maintenance. The inevitable accumulation of dust should be removed periodically with a soft, long bristled brush, a vacuum cleaner (be sure that the power is OFF if hose end is metal), or a stream of low pressure air. An excessive ambient temperature level is certainly the greatest danger to electronic equipment. Although ADC equipment requires no special cooling, during preventive maintenance check the rack enclosure filters (if it has them) and rack ventilation entrance/exit points to insure that they are not obstructed.

ADC provides extender boards for the two PC boards in this equipment. Each card may be made more accessible by installing it on the extender board provided. The dc voltages present on the boards are low enough so that no potential shock hazard exists; but it is still necessary to guard against accidential shorts from tools and other metal (conductor) objects.

If it becomes necessary to replace any solid state components, precautions should be taken to avoid heat damage. The use of long-nosed pliers or other clip-on heat sinks is advised. Also, excessive heat may cause the actual copper PC board circuits to "peel off" the G10 glass epoxy boards. ADC recommends the small, pencil type soldering irons of 20 - 30 watts capacity to reduce the chance of damage to solid state components or the PC board itself.

One of the most effective means of removing the solder from the leads of the device being replaced is to use the so called "solder sponge" technique. ADC recommends the use of a rosin-dipped, tinned, copper braid manufactured by Alpha Industries, or equivalent. If this is not available, copper braid can be obtained by stripping the insulation off short pieces of coaxial cable and using the braided shield dipped in a rosin solution such as Alpha Industries Alpha Realiafoam #809 Flux. A clean, well-tinned soldering iron tip held against the rosin coated braid, which in turn is held against the solder area to be cleaned, will result in quick removal of

solder from this area with minimum possibility of heat damage.

Junction breakdown in transistors and diodes due to excessive current or heat will result in the junction's appearing to be short circuited or open circuited. This can be easily verified by an ohmmeter like the Simpson 260. To avoid the possibility of damaging a good component, set the meter on the ohms x 10 scale. With the knowledge that a forward biased diode presents a low impedance path and a reverse biased diode a high impedance path, you can quickly determine if a diode/transistor junction has failed in either of the two modes previously mentioned.

With the positive lead of the voltmeter on the anode of a silicon diode and the negative lead on the cathode (end with the band), you should read on the ohmmeter something less than 500 ohms, but not a short. Reversing the leads should result in a reading of greater than one megohm, but not an open.

Transistors can be regarded as two diodes connected back-to-back. The diode equivalent to PNP and NPN transistors is shown in Fig. 6-1.

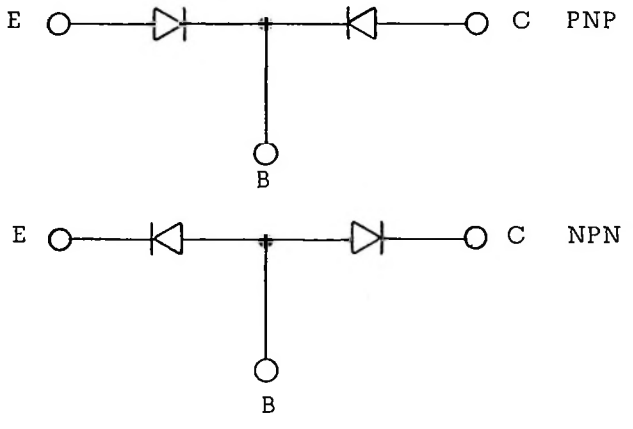


Fig. 6-1 Diode Equivalent of Transistor

The bottom view of a typical transistor used by ADC is shown in Fig. 6-2.

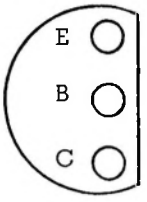


Fig. 6-2 Bottom View of Typical Transistor

Using the technique previously explained for determining the condition of a diode, you can use the Simpson 260 (ohmmeter) to determine the condition of the "diode" junction in a transistor. Again, in the forward direction, the meter should read about 300 - 500 ohms, and in the reversed bias direction, over one megohm. In no case should the meter indicate a short or an open condition.

Series 900/900E Routing Switcher
Test Data

Serial Number _____

Equipment List

Voltmeter - Simpson 260 or equal
Wide Band Oscilloscope - Tektronix 465 or equal
Vectorscope - Tektronix 520A or equal
Audio Signal Generator - Hewlett Packard 200 CD or equal
AC Voltmeter - Hewlett Packard Model 334A or equal
Sweep Generator - Kay Model 154C or equal
Staircase Generator - ADC Model 1108 or equal

The tests outlined here are fundamental and do not include crosstalk, signal-to-noise, bounce, dc, chrominance/luminance delay, etc. These are test usually conducted at the factory and witnessed by the customer.

Power Supply (ADC Model 501)

1. Apply ac power and check the:

+12 volt supply	(+11.5 to +12.5 volts)_____
-12 volt supply	(-11.5 to -12.5 volts)_____
+6 volt supply	(+5.75 to +6.25 volts)_____

2. Connect the power cable to the 900 matrix and measure ripple on the supplied:

+12 volts	(Less than 5 mV p-p)_____
-12 volts	(Less than 5 mV p-p)_____
+6 volts	(Less than 5 mV p-p)_____

3. Reduce the line voltage (Variac) until the ripple increases by 5 mV.

(Less than 105 volts ac)_____

4. Connect the Simpson 260 VOM across the +12 volt supply, remove cable to matrix. _____

5. Check the +12 volt power supply short circuit protection by shorting between +12 volts and ground. _____

6. Repeat steps 4 and 5 for the -12 volt and +6 volt supplies. _____

Matrix

7. Reconnect power cable to matrix. _____

8. Insert 1 volt p-p sweep signal on input 1 and terminate. _____

9. Insert +8 dBm audio signal on audio input 1 and terminate. _____

10. Route input 1 through output 1. _____

11. Adjust output 1 VIDEO GAIN control until the video output level is 1 volt p-p. _____

12. Adjust output 1 FREQUENCY RESPONSE controls while observing the output response at:

5 MHz	(±0.1 dB)	_____
8 MHz	(±0.5 dB)	_____
10 MHz	(Less than -1 dB)	_____

13. Replace the sweep signal with a 1 volt p-p staircase signal modulated with 20 IEEE units of subcarrier and measure the differential gain through the connected routing path.

(Less than 0.5%) _____

14. Measure differential phase through the same path.

(Less than 0.5°) _____

15. Adjust the AUDIO GAIN control until the audio output level is +8 dBm into 600 ohms. _____

16. Using the H-P 334 A, measure distortion.

20 Hz	(Less than 0.5%)	_____
1 kHz	(Less than 0.5%)	_____
20 kHz	(Less than 0.5%)	_____

17. Using the H-P 334A, measure response.

20 Hz	(±0.5 dB)	_____
1 kHz	(0.0 dB)	_____
20 kHz	(±0.5 dB)	_____

18. Repeat steps 8 to 17 for inputs 2 through 20. Make no adjustments except R11 on each crosspoint card to equalize path length delay. _____

19. Route input 1 to output 2. Insert 1 volt p-p sweep signal and +8 dBm audio signal in input 1. _____

20. Adjust output 2 VIDEO GAIN control until the video output level is 1 volt p-p. _____

21. Adjust output 2 FREQUENCY RESPONSE controls while observing the output response at:

5 MHz	(±0.1 dB)	_____
8 MHz	(±0.5 dB)	_____
10 MHz	(Less than -1 dB)	_____

22. Replace the sweep signal with a 1 volt p-p staircase signal modulated with 20 IEEE units of subcarrier and measure the differential gain through output .

(Less than 0.5%) _____

23. Measure differential phase through output 2.

(Less than 0.5°) _____

24. Adjust the AUDIO GAIN control until the audio output level is +8 dBm into 600 ohms. _____

25. Using the H-P 334 A, measure distortion.

20 Hz	(Less than 0.5%)	_____
1 kHz	(Less than 0.5%)	_____
20 kHz	(Less than 0.5%)	_____

26. Using the H-P 334 A, measure response.

20 Hz	(±0.5 dB)	_____
1 kHz	(0.0 dB)	_____
20 kHz	(±0.5 dB)	_____

27. Repeat steps 19 through 26 sequentially, routing input 1 through the remaining outputs. _____

Date_____ Technician _____

The operational tests have now been completed. During system test, ADC checks response, differential gain and phase, etc., for every crosspoint (900 series only) in the system. These test results are included in the system manual. In the event that a problem occurs, put the subject card on its extender and use the Tektronix 465 to trace the video or audio signal to or through the suspected problem area. Use the techniques outlined in the first part of this section to replace any failed solid state components.

SECTION 7 - COMPONENT LAYOUTS, PARTS LISTS AND WIRING LISTS

Component Layouts

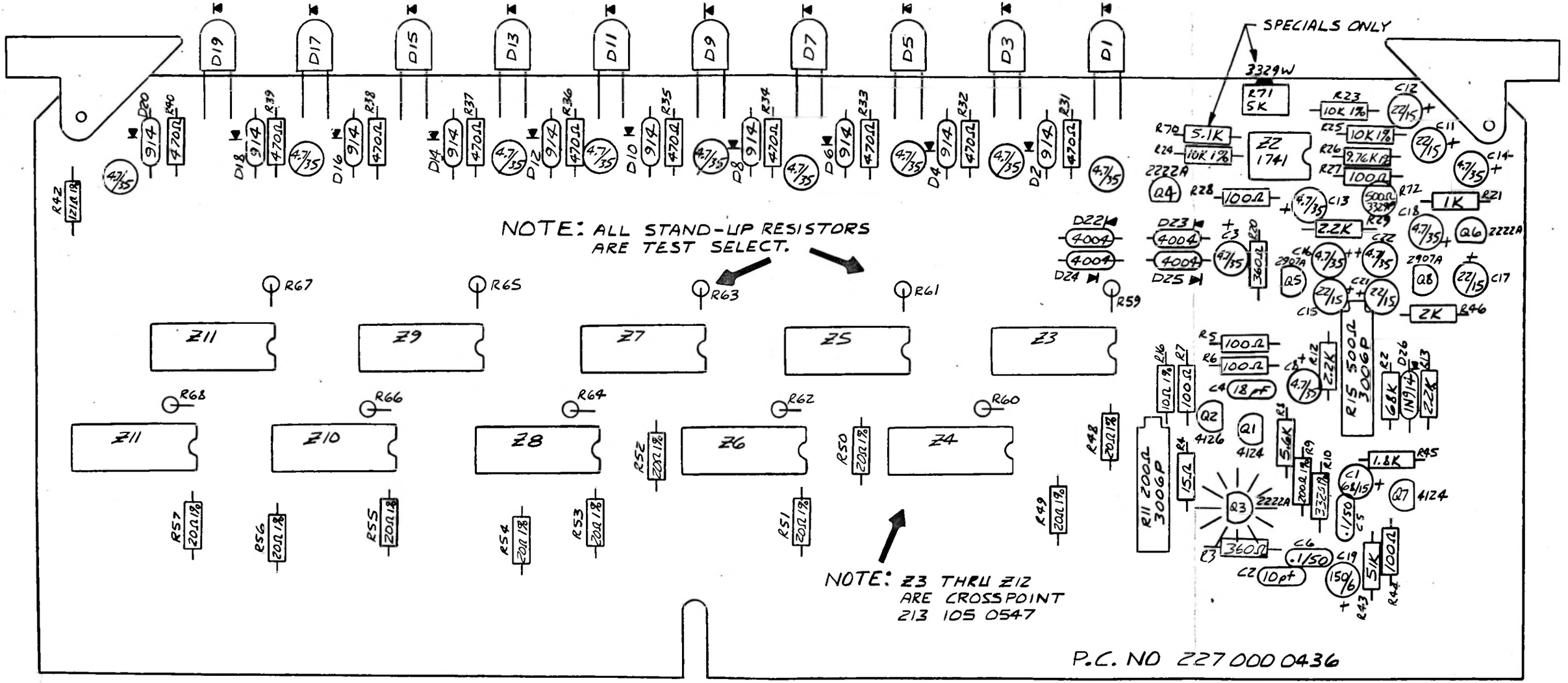
1.	1 x 10 Crosspoint, Monolithic	105 930 0013
2.	Audio/Video Output Amplifier - 9102M	105 930 0014
3.	Component Ass'y, Rear Panel	103 930 0005
4.	Series 900 Rear Panel (photograph)	
5.	Strobe Conditioning & Scan Control	105 930 0008
6.	Random Sync Strobe Generator	105 930 0006
7.	501 Power Supply - 900 Matrix	109 274 0003

Wiring Lists

1. 900 Matrix - Audio Input
2. 900 Matrix - Audio Output
3. Matrix Control - 20 Pin Connector, J1 & J2
4. Matrix - Audio In, Connector J3 & J4
5. Matrix Output Tally - 34 Pin Connector, J5
6. Power Connector - 14 Pin Connector, J8
7. Matrix Input Tally - 34 Pin Connector, J6
8. Matrix - Audio Out, Connector 3, J7

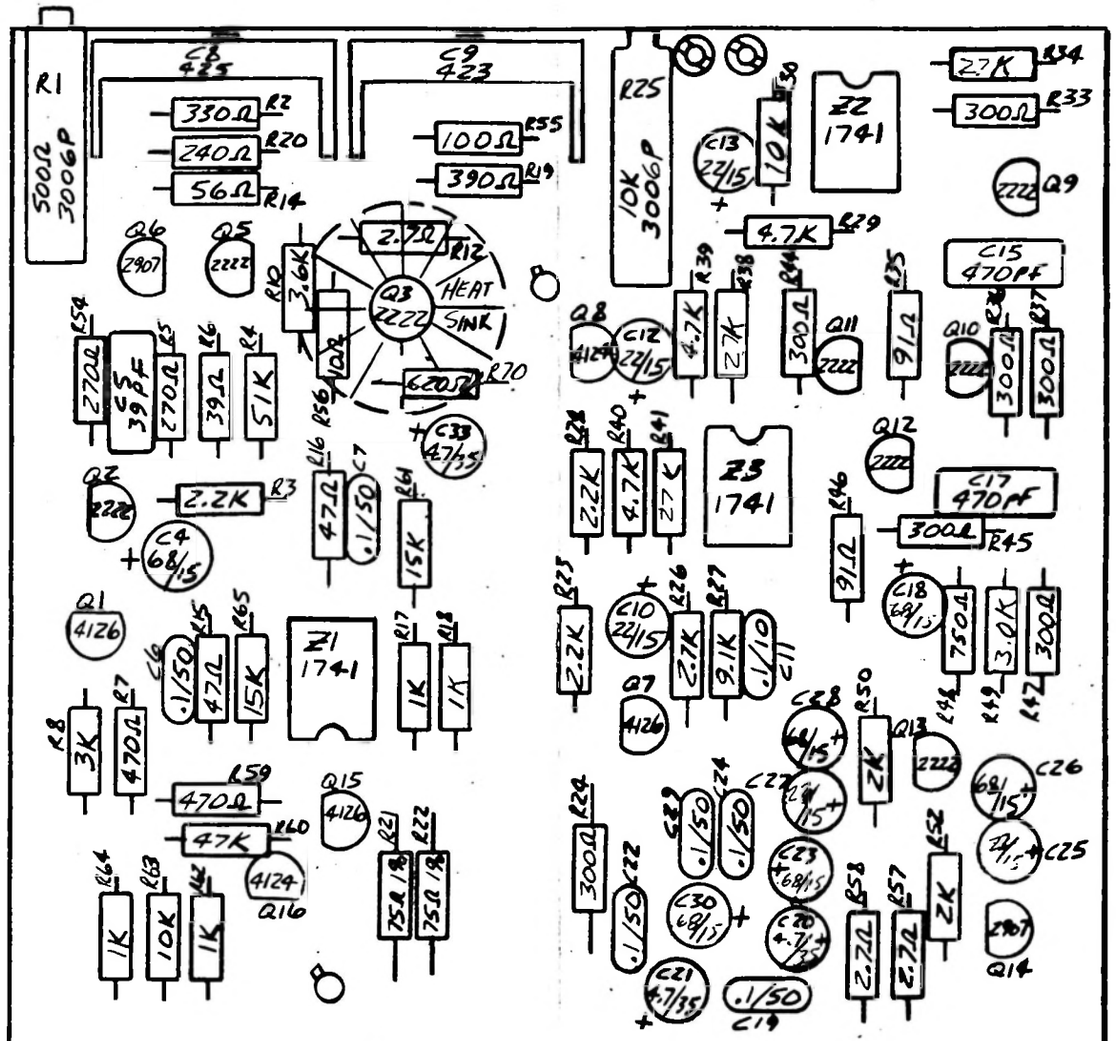
Parts Lists

1. 20 x 10 Routing Switcher Motherboard - 9103
2. Rear Panel - 9104
3. Strobe Conditioning & Scan Control
4. Random Sync Strobe Generator
5. 900 Matrix Power Supply



AMERICAN DATA CORPORATION an AIRPAX COMPANY		
SCALE: 2:1	APPROVED BY:	DRAWN BY EC.
DATE: 3/14/75		REVISED A.
1 X 10 CROSSPOINT, MONOLITHIC		
		DRAWING NUMBER 105 930 0013

PMT: 2/11/76



P.C. NO 0437

AMERICAN DATA CORPORATION AN AIRPAX COMPANY		
SCALE: 2/1	APPROVED BY:	DRAWN BY E.C.
DATE: 4-18-75		REVISED C
AUDIO/VIDEO OUTPUT AMP		
9102M		DRAWING NUMBER 1059300437

Cy: 3/20/76

DMT: 9/17/75

B
200858-2
34 PIN
AMP
HDW TALLY
J6

B
AUDIO IN
10-19
J4

20x10 ROUTING SWX
227000276

B
200858-2
34 PIN
AMP
AUDIO IN 00-09
J3

B
BUS TALLY
J5

PWR
E
200858-2
14 PIN
AMP
J8

VID IN

A
19 18 17 16 15 14 13 12 11 10
A

VID. IN.

A
09 08 07 06 05 04 03 02 01 00
A

Z41 SN7445
Z42 SN7445
Z43 SN7445
Z44 SN7445
Z45 SN7445
Z46 SN7445
Z47 SN7445
Z48 SN7445
Z49 SN7445
Z4A SN7445

Z31 SN7475
Z32 SN7475
Z33 SN7475
Z34 SN7475
Z35 SN7475
Z36 SN7475
Z37 SN7475
Z38 SN7475
Z39 SN7475
Z3C SN7475

D
200858-2
2 PIN
AMP
T1 CONTROL

Y PROGRAM

Z29 SN7408
Z2C SN7408
Z2E SN7400
Z2F SN7400
Z30 SN7402
Z51 SN7400
Z24 SN74154

X PROGRAM

Z27 SN7445
Z21 SN7402
Z22 SN7402
Z23 SN7402

Z11 SN7475
Z12 SN7475
Z13 SN7475
Z14 SN7475
Z15 SN7475
Z16 SN7475
Z17 SN7475
Z18 SN7475
Z19 SN7475
Z1A SN74174

Z1 SN7445 OR 74LS74
Z2 SN7445
Z3 SN7445
Z4 SN7445
Z5 SN7445
Z6 SN7445
Z7 SN7445
Z8 SN7445
Z9 SN7445
Z0 SN7445

D
200858-2
20 PIN
AMP
J2
CONTROL

C
201358-1
50 PIN
AMP
J7
AUDIO OUT
00-09

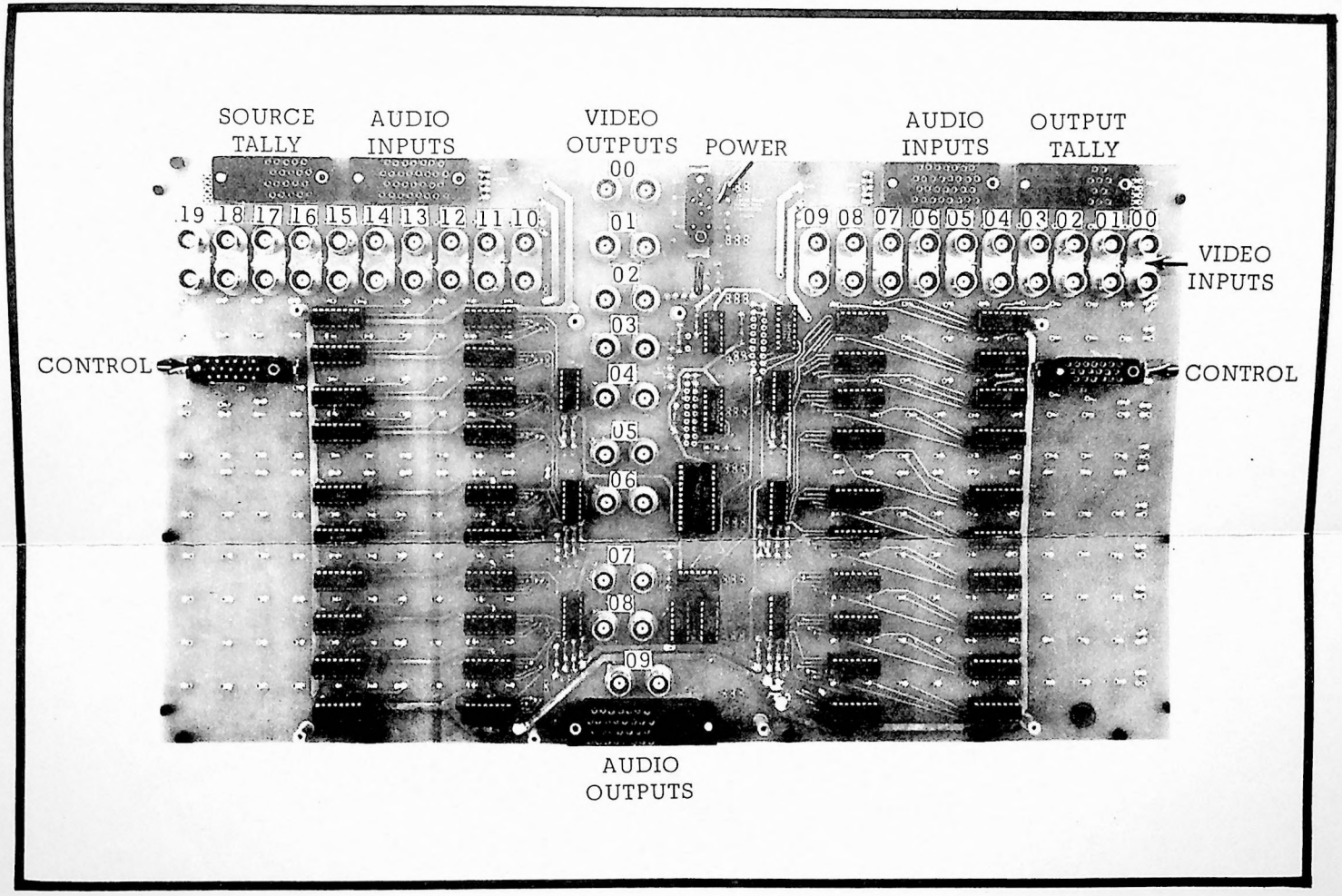
AMERICAN DATA CORPORATION
- ARPAH -

SCALE:	APPROVED BY	DRAWN BY: ET
DATE: 3/24/75		REVISED

COMPONENT ASSY.

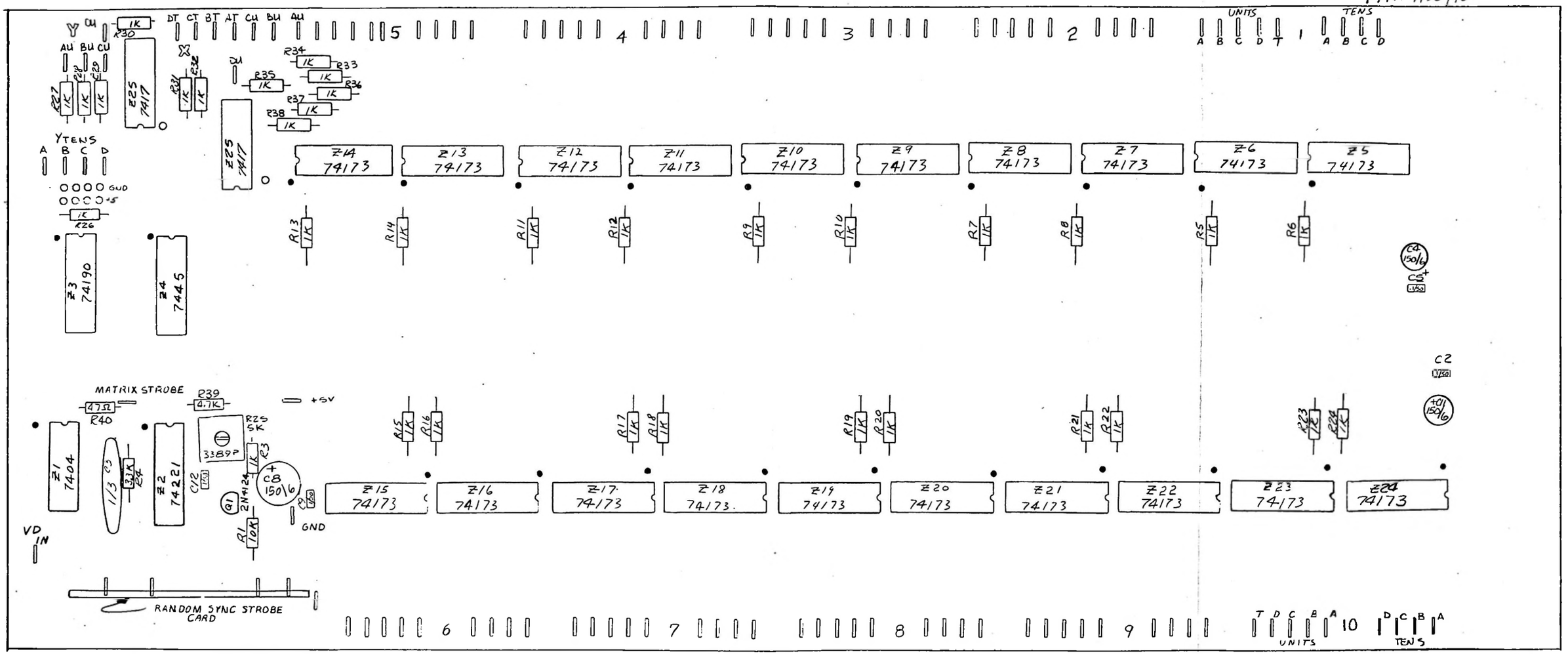
REAR PANEL — DRAWING NUMBER: 1059300003

(11) DENOTES BIFURCATED TERMINAL

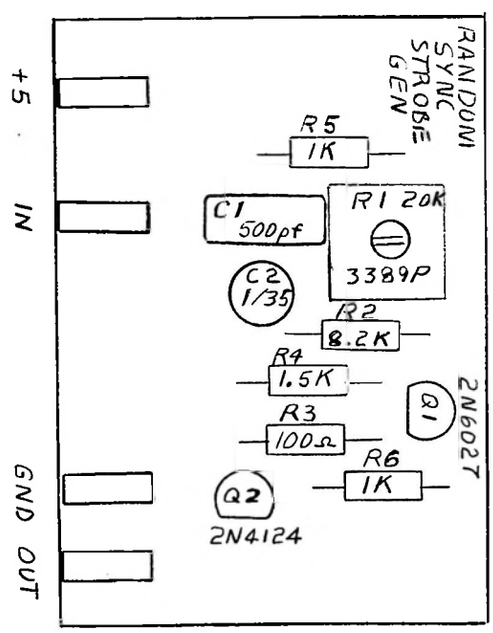


SERIES 900 REAR PANEL

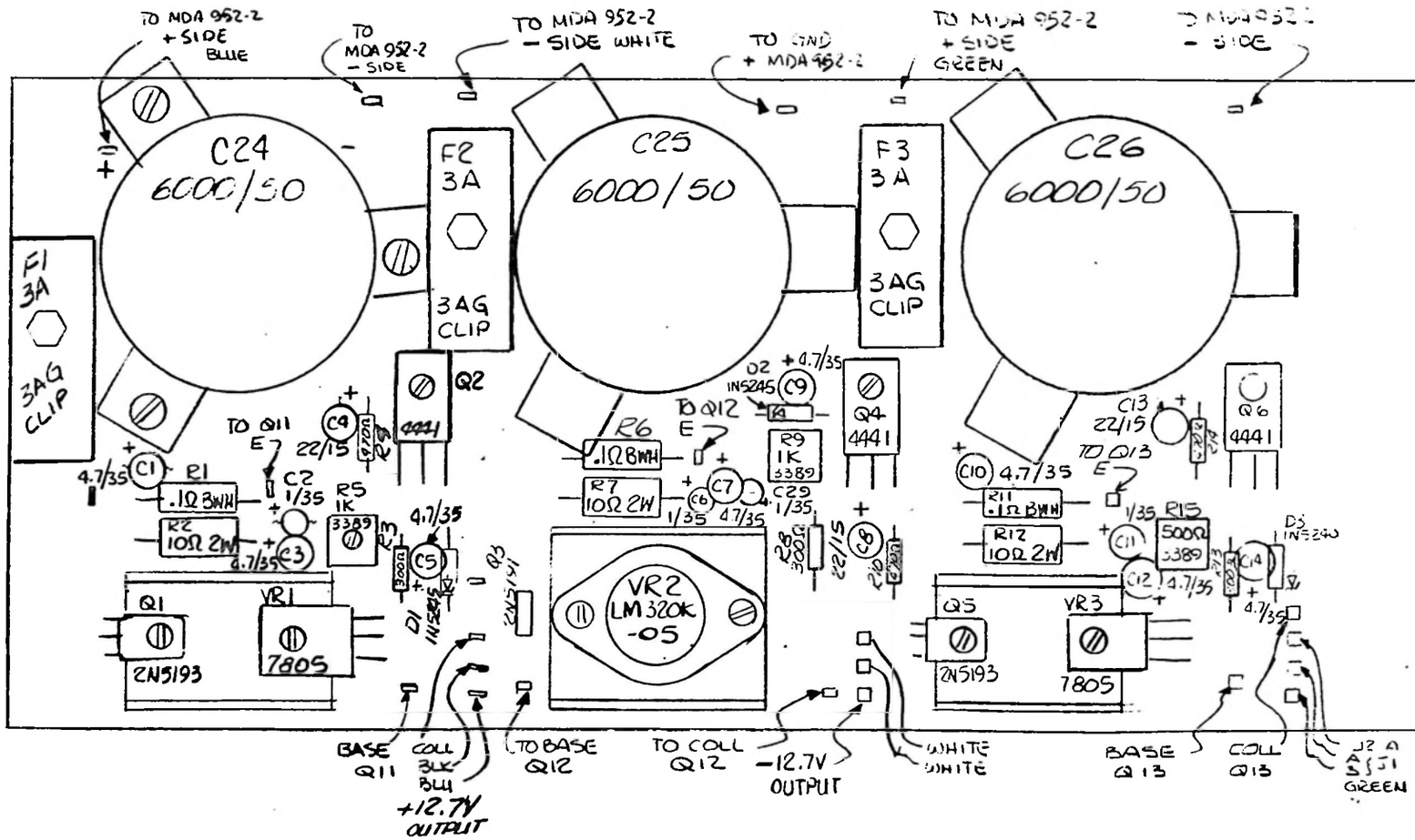
PMT: 7/20/76



AMERICAN DATA CORPORATION an AIRPAX company		
SCALE: ~	APPROVED BY:	DRAWN BY LDS
DATE: 3/31/75		REVISED C 4-23-76
STROBE CONDITIONING & CAN CONTROL ASSY		
MODEL 9107		DRAWING NUMBER D-7 [illegible]



AMERICAN DATA CORPORATION AN AIRPAX COMPANY		
SCALE: 2:1	APPROVED BY:	DRAWN BY LDS
DATE: 4/1/75		REVISED
RANDOM SYNC STROBE GEN ASSY		
		DRAWING NUMBER 1059300006



AMERICAN DATA CORPORATION
AN AIRPAX COMPANY

SCALE: 1:1	APPROVED BY:	DRAWN BY CHNAR
DATE: 4-9-75		REVISED

501 POWER SUPPLY ASSEMBLY

900 MATRIX

DRAWING NUMBER 109C140003

900 MATRIX

TITLE: Audio Input
CONN: 34 PIN AMP

PIN	DESCRIPTION		PIN	DESCRIPTION	
A	Red	1	T	Red	6
B	Black	1	U	Black	6
C	Shield	1	V	Shield	6
D	Red	2	W	Red	7
E	Black	2	X	Black	7
F	Shield	2	Y	Shield	7
H	Red	3	Z	Red	8
J	Black	3	AA	Black	8
K	Shield	3	BB	Shield	8
L	Red	4	CC	Red	9
M	Black	4	DD	Black	9
N	Shield	4	EE	Shield	9
P	Red	5	FF	Red	10
R	Black	5	HH	Black	10
S	Shield	5	JJ	Shield	10

900 MATRIX

TITLE: Audio Output
CONN: 50 Pin Amp

PIN	DESCRIPTION		PIN	DESCRIPTION	
A	Red	1	T	Red	6
B	Black	1	U	Black	6
C	Shield	1	V	Shield	6
D	Red	2	W	Red	7
E	Black	2	X	Black	7
F	Shield	2	Y	Shield	7
H	Red	3	Z	Red	8
J	Black	3	a	Black	8
K	Shield	3	b	Shield	8
L	Red	4	c	Red	9
M	Black	4	d	Black	9
N	Shield	4	e	Shield	9
P	Red	5	f	Red	10
R	Black	5	h	Black	10
S	Shield	5	j	Shield	10

NOTE: Only Audio Outputs 8 and 9 are used in this system.

MATRIX CONTROL

20 Pin Connector
J1 - Male (201356-1)
J2 - Female (200346-2)

		COLOR
A	X Tens 1	Brn
B	X Tens 2	Wht/Blk
C	X Tens 4	Wht/Red
D	X Tens 8	Wht/Orn
E	X Units 1	Wht/Yel
F	X Units 2	Wht/Grn
H	X Units 4	Wht/Blu
J	X Units 8	Wht/Vio
K	Y Tens 1	Wht/Gry
L	Y Tens 2	Wht/Blk/Brn
M	Y Tens 4	Wht/Blk/Red
N	Y Tens 8	Wht/Blk/Orn
P	Y Ones 1	Wht/Blk/Yel
R	Y Ones 2	Wht/Blk/Grn
S	Y Ones 4	Wht/Blk/Blu
T	Y Ones 8	Wht/Blk/Vio
U	Strobe	Wht/Blk/Gry
V	Ground	Blk
W	+5 (J2 Only)	Grn

MATRIX - AUDIO IN

Connector J3 and J4 - Female
300838-2

PIN #	DESCRIPTION J3	DESCRIPTION J4	COLOR
A	Audio In 1	Audio In 11	Vio
B	Audio In 1	Audio In 11	Gry
C	Audio In 1	Audio In 11	Blk
D	Audio In 2	Audio In 12	Vio
E	Audio In 2	Audio In 12	Gry
F	Audio In 2	Audio In 12	Blk
H	Audio In 3	Audio In 13	Vio
J	Audio In 3	Audio In 13	Gry
K	Audio In 3	Audio In 13	Blk
L	Audio In 4	Audio In 14	Vio
M	Audio In 4	Audio In 14	Gry
N	Audio In 4	Audio In 14	Blk
P	Audio In 5	Audio In 15	Vio
R	Audio In 5	Audio In 15	Gry
S	Audio In 5	Audio In 15	Blk
T	Audio In 6	Audio In 16	Vio
U	Audio In 6	Audio In 16	Gry
V	Audio In 6	Audio In 16	Blk
W	Audio In 7	Audio In 17	Vio
X	Audio In 7	Audio In 17	Gry
Y	Audio In 7	Audio In 17	Blk
Z	Audio In 8	Audio In 18	Vio
AA	Audio In 8	Audio In 18	Gry
BB	Audio In 8	Audio In 18	Blk
CC	Audio In 9	Audio In 19	Vio
DD	Audio In 9	Audio In 19	Gry
EE	Audio In 9	Audio In 19	Blk
FF	Audio In 10	Audio In 20	Vio
HH	Audio In 10	Audio In 20	Gry
JJ	Audio In 10	Audio In 20	Blk

MATRIX
OUTPUT TALLY

34 Pin Connector - Female
200838-2

J5

PIN #	DESCRIPTION	COLOR
A	Bus Tally 1	Brn
B	Bus Tally 2	Orn
C	Bus Tally 3	Vio
D	Bus Tally 4	Gry
E	Bus Tally 5	Wht/Blk
F	Bus Tally 6	Wht/Brn
H	Bus Tally 7	Wht/Red
J	Bus Tally 8	Wht/Orn
K	Bus Tally 9	Wht/Yel
L	Bus Tally 10	Wht/Grn

POWER CONNECTOR

14 Pin Connector - Male
201355-1

J8

PIN #	DESCRIPTION	COLOR
A	+5	Grn
B	+5	Grn
C		
D		
E	+12	Blu
F	+12	Blu
H	-12	Wht
J	-12	Wht
K		
L		
M		
N		
P	Gnd	Blk
R	Gnd	Blk

MATRIX
INPUT TALLY

34 Pin Connector - Female
200838-2

J6

PIN #	DESCRIPTION	COLOR
A	Row Tally 1	Brn
B	Row Tally 2	Orn
C	Row Tally 3	Vio
D	Row Tally 4	Gry
E	Row Tally 5	Wht/Blk
F	Row Tally 6	Wht/Brn
H	Row Tally 7	Wht/Red
J	Row Tally 8	Wht/Orn
K	Row Tally 9	Wht/Yel
L	Row Tally 10	Wht/Grn
M	Row Tally 11	Wht/Blu
N	Row Tally 12	Wht/Vio
P	Row Tally 13	Wht/Blk/Brn
R	Row Tally 14	Wht/Blk/Red
S	Row Tally 15	Wht/Blk/Orn
T	Row Tally 16	Wht/Blk/Yel
U	Row Tally 17	Wht/Blk/Grn
V	Row Tally 18	Wht/Blk/Blu
W	Row Tally 19	Wht/Blk/Vio
X	Row Tally 20	Wht/Blk/Gry

MATRIX - AUDIO OUT

Connector 3 - Female
201358-1

J7

PIN #	DESCRIPTION	COLOR
A	Audio Out 1	Red
B	Audio Out 1	Black
C	Audio Out 1	Shield
D	Audio Out 2	Red
E	Audio Out 2	Black
F	Audio Out 2	Shield
H	Audio Out 3	Red
J	Audio Out 3	Black
K	Audio Out 3	Shield
L	Audio Out 4	Red
M	Audio Out 4	Black
N	Audio Out 4	Shield
P	Audio Out 5	Red
R	Audio Out 5	Black
S	Audio Out 5	Shield
T	Audio Out 6	Red
U	Audio Out 6	Black
V	Audio Out 6	Shield
W	Audio Out 7	Red
X	Audio Out 7	Black
Y	Audio Out 7	Shield
Z	Audio Out 8	Red
a	Audio Out 8	Black
b	Audio Out 8	Shield
c	Audio Out 9	Red
d	Audio Out 9	Black
e	Audio Out 9	Shield
f	Audio Out 10	Red
h	Audio Out 10	Black
j	Audio Out 10	Shield

PARTS LIST

20 x 10 Routing Switcher Motherboard - 9103

ADC Part Number	Description	Quantity Per Unit
227 000 0270	20 x 10 Routing Switcher M.B.	1
251 722 0002	4.7/35 Capacitor	3
251 722 0005	68/15 Capacitor	6
354 111 0001	1N914 Diode	20
304 800 0006	5-583407-1 58 Pin Conn.	20
304 800 0010	2-583407 Connector	10
762 000 0012	583671-1 Card Guide	50
304 000 0006	Key Plugs	30

PARTS LIST

Rear Panel - 9104

ADC Part Number	Description	Quantity Per Unit
227 000 0276	9104 Rear Panel	1
213 275 0053	SN74L42 I.C.	14
213 27 0026	SN7475 I.C.	20
213 275 0051	SN74L02	6
213 275 0036	SN74154 I.C.	1
213 275 0032	SN74121 I.C.	1
213 275 0009	SN7404 I.C.	1
213 275 0004	SN7400 I.C.	2
213 122 0004	UGJ7805 V. REG.	2
251 372 0035	470 pF DM-15 CAP	1
251 722 0002	4.7/35 KEMET CAP	4
251 722 0005	68/15 KEMET CAP	2
251 525 0003	.1/10 UK10 CAP	3
778 127 0048	1K RESISTOR	21
778 127 0064	4.7K RESISTOR	1
778 127 0040	470 OHMS RESISTOR	2
778 127 0034	270 OHMS RESISTOR	1
304 400 0006	583640-3 24 PIN	1
304 400 0022	ME2-16-1-WGB	46
304 400 0019	ME2-14-1-WGB	10
304 700 0020	201298-1 14 PIN F	1
304 700 0021	201355-1 14 PIN M	1
304 600 0026	201378-2 SHIELD LG	1
304 600 0027	201360-2 SHIELD ST	1
304 700 0029	200289-2 G PIN M	4
304 600 0022	200390-2 G PIN F	4
304 600 0025	201921-1 LKNG SPG M	4
304 700 0030	201922-1 LKNG SPG F	4
304 700 0022	200346-2 20 PIN F	2
304 600 0017	201356-1 20 PIN M	2
304 600 0038	201380-2 SHIELD ST	4
304 700 0023	200838-2 34 PIN F	4
304 600 0018	201357-1 34 PIN M	4
304 600 0029	201571-1 SHIELD LG	4
304 600 0031	200517-2 SHIELD ST	4

Rear Panel - 9104...continued

ADC Part Number	Description	Quantity Per Unit
304 700 0033	200871-2 J SCR LG M	4
304 700 0028	200867-2 J SCR LG F	4
304 600 0019	200277-2 50 PIN M	1
304 700 0025	201358-1 50 PIN F	1
304 600 0030	202670-2 SHIELD LG	1
304 600 0020	202672-1 J SCR LG M	2
304 600 0021	202673-1 J SCR LG F	1
304 900 0003	UG1094-U BNC	60
304 900 0005	KS9-128 BNC	60

PARTS LIST

Strobe Conditioning & Scan Control

ADC Part Number	Description	Quantity Per Unit
227 000 0321	PC Card	1
213 275 0009	7404 Integrated Ckt	1
213 275 0019	7445 Integrated Ckt	1
213 275 0055	74221 Integrated Ckt	1
213 275 0056	74173 Integrated Ckt	20
213 275 0058	74190 Integrated Ckt	1
251 515 0003	1 uF/3V UK-105 Capacitor	1
251 533 0002	.1/50 Capacitor (Note: .1/50 replaces .1/10)	6
251 722 0006	150/6 Capacitor	4
778 127 0048	1K ohms RC07 Resistor	22
778 127 0060	3.3K ohms RC07 Resistor	1
778 127 0072	10K ohms RC07 Resistor	1
785 333 0014	5K ohms 3389P-1-502	1
891 211 0007	2N4124 Transistor	1

Random Sync Strobe Generator

227 000 0334	PC Card	1
251 722 0001	1/35 Capacitor	1
251 372 0036	500 pF DM-15 Capacitor	1
778 127 0026	100 ohm RC07	1
778 127 0048	1K ohm RC07	2
778 127 0052	1.5K ohm RC07	1
785 333 0016	20K 3389P-1-203 Pot.	1
891 211 0007	2N4124 Transistor	1
891 131 0002	2N6027 Put Unijunction	1

900 Matrix Power Supply

ADC Part Number	Description	Quantity Per Unit
227 000 0083	PC Card 501 Power Supply	1
213 123 0001	UGH 7805 Voltage Regulator	2
213 122 0001	LM-320K-05	1
251 722 0001	1/35 Capacitor	4
251 722 0002	4.7/35 Capacitor	8
251 722 0007	22/15 Capacitor	3
251 834 0008	6000/50 36D Capacitor	3
304 000 0001	SKT-5BC Test Point Black	1
304 000 0002	SKT-5BC Test Point White	1
304 000 0004	SKT-5BC Test Point Green	1
304 000 0005	SKT-5BC Test Point Blue	1
304 700 0020	201298-1 A Pin Connector Block	2
304 700 0029	200389-2 Guide Pin & Socket Male	2
304 600 0022	200390-2 Guide Pin & Socket Female	2
304 700 0030	201922-1 Locking Spring Female	4
354 091 0007	MDA-952-2 Diode Bridge	3
354 821 0015	1N5240 Zener Diode	1
354 821 0017	1N5245 Zener Diode	2
376 112 0004	3A 3AG SB 313003 Fuse	1
376 611 0001	342004 Fuse Holder	1
376 111 0008	3A 3AG 312003 Fuse	3
376 511 0001	3AG Fuse Clip	3
386 010 0002	VR8 Mounting Clamp	3
	Heat Sink	3
	Chassis Assembly	1
778 127 0035	300 ohm RC07 Resistor	3
778 127 0040	470 ohm RC07 Resistor	3
778 157 0001	10 ohm 2W RC42 Resistor	3
778 657 0001	.1 ohm 2W BWH Resistor	3
785 333 0013	1K ohm 3389P-1-102 Pot.	2
785 333 0012	500 ohm 3389P-1-501 Pot.	1
891 321 0006	2N5193	2
891 311 0012	2N5191	1
891 321 0007	2N5879	2
891 311 0001	MJ3771 Power Transistor	1
835 200 0001	2N4441 SCR	3
870 000 0031	H-252 Transformer	2
948 000 0001	17237-B Line Cord	1
386 600 0001	Strain Relief SR5P4	1
841 111 0001	Switch MST-105-D	1