
instruction book

## BROADCAST EQUIPMENT GUARANTEE

The equipment described herein is sold under the following guarantee:
a. Except as set forth in paragraph b. of this section, Collins agrees with Buyer to repair or replace, without charge, any properly maintained equipment, parts oraccessories which are defective as to design, materials, or workmanship and which are returned in accordance with Collins instructions by Buyer to Collins factory, transportation prepaid, provided:

1. Notice of a claimed defect in the design, materials or workmanship of the equipment manufactured by Collins is given by Buyer to Collins within five (5) years from date of delivery, with exception of rotating machinery such as blowers, motors, and fans whereby notice must be given by Buyer to Collins within two (2) years from date of delivery.
2. Notice of a claimed defect in the design, materials or workmanship of the following described Collins manufactured equipment is given by Buyer to Collins within two (2) years from the date of delivery:

| $20 \mathrm{~V}-3$ | $26 \mathrm{U}-2$ | 81 M | $172 \mathrm{G}-2$ | $216 \mathrm{C}-2$ | $313 \mathrm{~T}-4$ | $642 \mathrm{~A}-2$ | $820 \mathrm{~F}-1$ | $830 \mathrm{D}-1$ | $830 \mathrm{~F}-2 \mathrm{~A}$ |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| $26 \mathrm{~J}-1$ | $42 \mathrm{E}-7$ | $144 \mathrm{~A}-1$ | $212 \mathrm{H}-1$ | $313 \mathrm{~T}-1$ | $356 \mathrm{H}-1$ | $786 \mathrm{M}-1$ | $\mathrm{~A} 830-2$ | $830 \mathrm{E}-1$ | $830 \mathrm{H}-1 \mathrm{~A}$ |
| $26 \mathrm{U}-1$ | $42 \mathrm{E}-8$ | $172 \mathrm{G}-1$ | $212 \mathrm{Z}-1$ | $313 \mathrm{~T}-3$ | $564 \mathrm{~A}-1$ | $820 \mathrm{E}-1$ | $830 \mathrm{~B}-1$ | $830 \mathrm{~F}-1$ | $830 \mathrm{~N}-1 \mathrm{~A}$ |

b. The above guarantee does not extend to other equipment, accessories, tubes, lamps, fuses, and tape heads manufactured by others which are subject to only adjustment as Collins may obtain from the supplier thereof.
c. Collins further guarantees that any radio transmitter described herein will deliver full radio frequency power output at the antenna lead when connected to a suitable load, but such guarantee shall not be construed as a guarantee of any definite coverage or range of said apparatus.
d. The guarantee of this section is void if:

1. The equipment malfunctions or becomes defective as a result of alterations or repairs by others than Collins or its authorized service center, or
2. The equipment is exposed to environmental conditions more severe than specified by Collins in equipment manuals.
e. NO OTHER WARRANTIES, EXPRESSED OR IMPLIED, INCLUDING WARRANTIES OF MERCHANTABILITY OR FITNESS FOR INTENDED PURPOSE, SHALL BE APPLICABLE TO ANY EQUIPMENT SOLD HEREUNDER.
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3. Notice of the sale of the F.C.C. license is given by Buyer to Collins in writing within thirty (30) days after the consummation of said sale; and
4. No greater rights are granted to the purchaser of Buyer's F.C.C. license than are granted herein to Buyer.

How to Return Material or Equipment If, for any reason, you should wish to return material or equipment, whether under the guarantee or otherwise, you should notify us, giving full particulars including the details listed below, insofar as applicable. If the item is thought to be defective, such notice must give full information as to nature of defect and identification (including part number if possible) of part considered defective. (With respect to tubes we suggest that your adjustments can be speeded up if you give notice of defect directly to the tube manufacturer.) Upon receipt of such notice, Collins will promptly advise you respecting the return. Failure to secure our advice prior to the forwarding of the goods or failure to provide full particulars may cause unnecessary delay in the handling of your returned merchandise.

ADDRESS:
Collins Radio Company
Customer Returned Goods, 412-023
1225 North Alma Road
Richardson, Texas 75080

## INFORMATION NEEDED:

(A) Type number, name and serial number of equipment
(B) Date of delivery of equipment
(C) Date placed in service
(D) Number of hours of service
(E) Nature of trouble
(F) Cause of trouble if known
(G) Part number (9 or 10 digit number) and name of part thought to be causing trouble
(H) Item or symbol number of same obtained from parts list or schematic
(I) Collins number (and name) of unit subassemblies involved in trouble
(J) Remarks

How to Order Replacement Parts When ordering replacement parts, you should direct your order as indicated below and furnish the following information insofar as applicable. To enable us to give you better replacement service, please be sure to give us complete information.

ADDRESS:
Collins Radio Company Service Parts, 412-024
1225 North Alma Road Richardson, Texas 75080

## INFORMATION NEEDED:

(A) Quantity required
(B) Collins part number ( 9 or 10 digit number) and description
(C) Item or symbol number obtained from parts list or schematic
(D) Collins type number, name and serial number of principal equipment
(E) Unit subassembly number (where applicable)


## instruction book

54N-1

## FM Frequency Monitor

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## glossary

AND: A coincidence circuit that provides a prescribed output when all of several possible input conditions are met.

FLIP-FLOP: A bistable multivibrator.
GATE: A circuit operating as a switch to pass or block a signal.
NAND: An AND circuit that provides phase inversion.
NOR: An OR circuit that provides phase inversion.
OR: A circuit that provides a prescribed output with one or more of severalpossible input conditions.

TOGGLE: Change of state. Reverse the outputs of a flip-flop.
TRUTH TABLE: Shows output conditions of a logic circuit element for all combinations of input conditions.


Figure 1-1. $54 N-1$ FM Frequency Monitor.

## general description

### 1.1 PURPOSE OF INSTRUCTION BOOK

This instruction book contains information for the installation, adjustment, operation, and maintenance of the $54 \mathrm{~N}-1$ FM Frequency Monitor. Instructions for all available optional equipment are included.

### 1.2 PURPOSE OF EQUIPMENT

The $54 \mathrm{~N}-1$ FM Frequency Monitor (figure 1-1) is a solid-state digital counter for remote, unattended monitoring of an FM broadcast transmitter carrier and, as an option, multiplex pilot carrier frequency drift. Frequency error is displayed, up to $\pm 2.0 \mathrm{kHz}$, in $1-\mathrm{kHz}$ increments, and local alarm indicators for errors greater than 1.0 kHz and 2.0 kHz are provided on the front panel. In addition, the frequency error in digital form, polarity of error, and contact closures for operation of remote indicators, alarms, or interlocks (to initiate transmitter shutdown), are provided on the monitor rear panel.

### 1.3 PHYSICAL DESCRIPTION

The monitor is assembled in a metal case $5-1 / 4$ inches high, 19 inches wide, and 14 inches deep, and weighs approximately 20 pounds. The monitor is of modular construction consisting of six fiberglass etched circuit cards, and a control and indicator module (with a power supply) that are removable from the front. The monitor contains a shield to prevent rf interference and emission. The rf input, pilot carrier input, $1-\mathrm{MHz}$ output (to check frequency standard operation), and remote readout connections are located on the rear panel.

### 1.4 FUNCTIONAL DESCRIPTION

The frequency monitor determines frequency error by converting the transmitter carrier to a pulse train and using the pulse train to clock a binary counter from a preset number to zero during a precise 1 - or 10 -second time period. During the 1 -second readout time, the count in the binary counter is read, decoded, and applied
to the monitor display and, if applicable, to the alarm circuits. The frequency error display is updated at the end of each count period and is displayed during the next sample period.

See figure 1-2. During monitor installation and setup, a binary number corresponding to the transmitter carrier frequency (divided by 100) is physically wired on the preset card. The preset card provides the binary counter with the binary number to start the counting. The 1 - or 10 -second sample time, 1-second off-time, and six timing pulses ( P 1 through P 6 ) are derived by dividing the $3-\mathrm{MHz}$ oscillator output. The rf transmitter carrier, containing from 0 to 100 percent frequency modulation ( $75-\mathrm{kHz}$ frequency deviation) is applied to the rf circuit where it is divided by 100 and shaped into a square wave. The shaped signal is applied to the count-gate matrix, but is not passed until the 1 - or 10second SAMPLE signal, from the divider network, is applied to the count-gate matrix. Prior to a count period, the binary counter is set at P1 time and preset to the transmitter frequency at P2 time. The decade counter is cleared at P1 time to ensure that the decade counter starts from zero and not an ambiguous number left from the previous count period. During a 10 -second sample time, the rf pulse train (divided by 100 in the rf circuit) is applied to the decade counter, where it is then divided by 10 and applied through the binary counter gate to the binary counter. The pulses, applied to the binary counter, cause the binary counter to count backwards from the transmitter carrier frequency (divided by 100) towards zero. During the 1 -second off-time (after the count period), the number in the binary counter is analyzed by the detector and storage circuits. The count remaining in the decade counter is examined by the round-off circuit, and if it is five or higher, adds another pulse to the binary counter, decreasing the count by one. If the binary counter counted more transmitter carrier frequency pulses than the assigned frequency, the detector and storage circuits add a pulse to the binary counter again to decrease the count by one. This pulse is added because the binary counter transition through zero requires an extra pulse from the rf input pulse
train. The detector and storage circuit's apply the count from the binary counter to the code converter and the alarm and inhibit circuits, and apply the polarity sign to the display circuits. The code converter decodes the binary input and applies a decimal equivalent to the display circuits. The code converter also applies the digital signals to the rear terminal connectors and the optional digital-to-analog converter. The inhibit circuit prevents the first error greater than 2.0 kHz from energizing the greater-than $-2.0-\mathrm{kHz}$ alarm relay. A TRANSIENT INHIBIT PULSE applied to the inhibit circuit also prevents the greater-than-$2.0-\mathrm{kHz}$ alarm circuit from operating if a momentary power loss or fluctuation interrupts the frequency count. If the transmitter rf carrier is lost or turned off, a SIGNAL PRESENCE signal inhibits both alarm circuits. The greater-than-$1.0-\mathrm{kHz}$ alarm is not inhibited for the first error count, and the first error greater than 1.0 kHz energizes the alarm.

Operation in the 1-second sample mode is similar to the 10 -second mode with the following differences. The counting period is 1 second. The rf pulse train, applied to the count-gate matrix, bypasses the decade counter and is applied directly to the binary counter gate and then to the binary counter. The round-off circuit is not used in the 1-second mode, but accuracy is not reduced because the carrier must be unmodulated for the 1 -second sample time.

Operation in the 19 KHZ PILOT mode is an option provided by Preset 3 or 4 Card. When operating in the 19 KHZ PILOT mode, monitor operation is similar to the 10 -second mode with the following exceptions: the $19-\mathrm{kHz} \mathrm{rf}$ input is applied to a shaper on the preset card where it is amplified, limited, and formed into a $19-\mathrm{kHz}$ pulse train, applied to the count-gate matrix and bypasses the decade counter.

The MODE switch supplies a constant $19-\mathrm{kHz}$ OPERATE signal to the rf circuit to enable the signal presence circuit, to the preset card to disable the transmitter frequency preset, to the count-gate matrix to disable the 10 -second count gate, and to the round-off circuit. The SIGNAL PRESENCE signal provides a logic 0 signal that enables the preset card, $19-\mathrm{kHz}$ preset circuit, and the $19-\mathrm{kHz}$ count gate. The MODE switch also enables the transient inhibit circuit, which inhibits the greater-than- $2.0-\mathrm{kHz}$ alarm. The $19-\mathrm{kHz}$ pulse train is sampled for 10 seconds, and the binary counter counts backwards from 190,000. The visual error readout in this mode is $\mathbf{- 2}$ to
+2 Hz in $0.1-\mathrm{Hz}$ increments. The greater-than-$1.0-\mathrm{kHz}$ alarm indicator actually means greater than 1.0 Hz , and the greater-than $-2.0-\mathrm{kHz}$ alarm indicator will not operate.

### 1.5 CUSTOMER OPTIONS

The following equipment options are available to tailor the monitor to customer requirements and provide checkout.
a. Preset 1 Card (CPN 770-7893-001). This card is supplied in monitor CPN 758-5742002 , and is used to set only the transmitter carrier frequency into the binary counter.
b. Preset 2 Card (CPN 770-7899-001). This card is supplied in monitor CPN 758-5742003, and is used to set the transmitter carrier frequency into the binary counter, and to provide digital-to-analog conversion for a remote analog frequency meter.
c. Preset 3 Card (CPN 774-6745-001). This card is supplied in monitor CPN 758-5742004, and is used to set the transmitter carrier and pilot carrier frequencies into the binary counter, to provide a $19-\mathrm{kHz}$ pilot carrier amplifier-shaper, and to provide digital-to-analog conversion for a remote analog frequency meter.
d. Preset 4 Card (CPN 781-1468-001). This sard-is provided in monitor CPN 758-5742005, and is used to set the transmitter earrier and pilot carrier frequencies into the binary counter, and to provide a $19-\mathrm{kHz}$ pilot carrier amplifier-shaper. NO NEMOTE.
e. 82U-1 Remote Analog Meter Panel (CPN 777-1390-001). The analog meter is a frequency meter mounted on a standard 19-inch rack panel and provides visual remotefrequency indications when using a monitor with Preset 2 or 3 Card installed.
f. 0782B-1 Self-Check Card (CPN 777-1439-001).
\% The self-check card is prewired to 1 MHz and contains a switch wired to preset errors of $-1.6,-.8,-.0,+.8$, and +1.6 into the binary counter. This card provides a functional check by comparing the preset error to the monitor $1-\mathrm{MHz}$ reference output.
g. Extender Card (CPN 781-5248-001). The extender card is used to provide access to monitor circuit card components for checkout.
h. RF Extender Cable (CPN 781-5252-001). The rf cable is used, when the rf circuit card is on the extender card, to connect the monitor rf input to the rf circuit card input connector.


### 1.6 TECHNICAL CHARACTERISTICS

Frequency Range:
Carrier
88 to 108 MHz
Pilot Carrier 19 kHz

Minimum Channel Spacing 100 kHz

RF Carrier Signal Input:
Voltage Level 3 to 9 vrms

Frequency Modulation 0 to $100 \% \max (100 \%$ modulation is defined as $75-\mathrm{kHz}$ frequency deviation)

Modulation Frequency 30 Hz to 75 kHz

19-kHz-Carrier Signal:
Input Impedance Greater than 15 K

Voltage Level 0.05 to 0.3 vrms

Frequency Standard: Stability
0.5 parts per $10^{6}$ from $-25^{\circ}$ to $55^{\circ} \mathrm{C}$

Aging
1 part per $10^{6}$ per year
Error Display:
Carrier -2.0 to +2.0 kHz . Inhibited above $\pm 2.0 \mathrm{kHz}$

19 kHz
-2.0 to +2.0 Hz . Inhibited above $\pm 2.0 \mathrm{~Hz}$
Carrier Alarm Presentation:
Visual alarm and contact closure when error exceeds +1.0 kHz
Visual alarm and contact closure, inhibited from transient activation, when error exceeds $\pm 2.0 \mathrm{kHz}$ for two consecutive samples
$19-\mathrm{kHz}$ Alarm Presentation:
Visual alarm and contact closure when error exceeds $\pm 1.0 \mathrm{~Hz}$
No visual alarm or contact closure when error exceeds $\pm 2.0 \mathrm{~Hz}$

Accuracy of Readout:
10-Second Sample Mode Modulated carrier $\pm 200 \mathrm{~Hz}$

1-Second Sample Mode Unmodulated carrier $\pm 200 \mathrm{~Hz}$
$19-\mathrm{kHz}$ Mode $\pm 0.1 \mathrm{~Hz}$

Resolution of Readout:
Carrier 100 Hz

19 kHz 0.1 Hz

Ambient Temperature Range:
$-25^{\circ}\left(-10^{\circ} \mathrm{F}\right)$ to $+55^{\circ} \mathrm{C}\left(+131^{\circ} \mathrm{F}\right)$
Ambient Humidity Range:
0 to $95 \%$
Altitude Range:
Up to 10,000 feet above msl
Shock and Vibration Conditions: Normal handling and shipping

Power Source:
$117 \mathrm{vac} \pm 10 \%$, single phase, $50 / 60 \mathrm{~Hz}$
Type of Service: Continuous

Alarm Relay Contact Rating:
At 24 vdc - 2 amperes resistive, 1 ampere inductive
At 115 vrms - 1 ampere resistive, 0.5 ampere inductive

External Readout Characteristics: Typically 3 ma at 1 vdc

## installation and adjustment

### 2.1 UNPACKING AND INSPECTING THE EQUIPMENT

Remove all packing material and carefully lift the unit from the package. Check the equipment against the packing slips. Visually inspect the units for damaged or missing components. Check for proper operation of controls. Any claims for damage should be filed promptly with the transportation agency. If such claims are to be filed, all packing material must be retained.

### 2.2 INSTALLATION

### 2.2.1 Mounting

Position the monitor in a standard 19 -inch rack, or cabinet, and secure.

### 2.2.2 Connections

Prior to connecting monitor primary power and external input and outputs, set POWER switch to OFF.

### 2.2.2.1 Alarm and Digital Readout Connections

Connect the desired digital readouts and alarms to terminal block on back of monitor (figure 2-1) as listed in table 2-1. Refer to paragraph 1.7 for alarm relay contact rating and external readout signal characteristics.

### 2.2.2.2 Remote Analog Frequency Meter Connection

If the remote-analog-frequency-meter option was purchased, verify that the monitor contains a Preset 2 Card (CPN 770-7899-001) or a Preset 3 Card (CPN 774-6745-001) in slot A6. Loop resistance of the connecting line to the remote meter must not exceed 15 K . Connect remote meter pin 1 to monitor terminal 19. Connect remote meter pin 2 to monitor terminal 20. Remove shorting spring from meter terminals. Retain shorting spring for future use. Replace shorting spring on meter
terminals before disconnection from monitor. To calibrate meter, refer to paragraph 2.2.3.

### 2.2.2.3 RF Cable, 19-kHz, and Primary Power Connection

Connect the monitor power cord to a 115 -vac, $50 / 60-\mathrm{Hz}$ source.

Note
The monitor will not operate properly if the rf inputs are not within the following limits.

Obtain the rf transmitter output signal from a point in the transmitter where the carrier signal is 3 to 9 vrms. Connect a 50 -ohm coaxial cable between the monitor rf input connector and the transmitter. Obtain the $19-\mathrm{KHZ}$ PILOT carrier signal from a point in the transmitter where the signal is 0.05 to 0.3 vrms . Connect the cable between monitor terminal 17 ( $19-\mathrm{kHz}$ input) and terminal 18 ( $19-\mathrm{kHz}$ ground) and the transmitter.

### 2.2.2.4 Preset Card Wiring

The monitor contains one of four types of preset cards in slot A6. Regardless of the type of preset card in the monitor, the card must be wired to correspond to the broadcast transmitter frequency that it will monitor. To wire a preset card, two 15 -inch lengths of pliable \#24 bus wire are required. The jumper wires are connected to the terminals by two or three tight wraps around each terminal. The column on the extreme left of table 2-2 lists transmitter frequency and the 18 columns progressing to the right on the table correspond to preset card terminals 1 through 18. Connect a jumper wire to preset card pin 19 and each terminal represented by a 0 in table $2-2$, columns 1 through 18 . Connect a jumper wire to preset card GRD terminal and each terminal represented by a 1 in table 2-2, columns 1 through 18.

Table 2-1. Alarm and Digital Readout Connections.

| SIGNAL NOMENCLATURE | TERMINAL NO. |
| :---: | :---: |
| Alarms <br> $>1.0-\mathrm{kHz}$ Contact Closure (greater than 1.0 kHz ) <br> Normally closed contacts <br> Normally open contacts <br> $>2.0-\mathrm{kHz}$ Contact Closure (greater than 2.0 kHz ) <br> Normally closed contacts <br> Normally open contacts <br> Readout Signals <br> NEGATIVE POLARITY (negative frequency error) <br> POSITIVE POLARITY (positive frequency error) <br> $2^{0}$ (binary 1) <br> $2^{1}$ (binary 2) <br> $2^{2}$ (binary 4) <br> $2^{3}$ (binary 8) <br> $2^{4}$ (binary 16 ) <br> ENABLE (10-second or 1-second) <br> SAMPLE 10 <br> $19-\mathrm{kHz}$ operate | 12 and 13 <br> 11 and 12 <br> 15 and 16 <br> 14 and 15 <br> 1 2 <br> 3 <br> 4 <br> 5 <br> 7 <br> 6 <br> 8 <br> 9 <br> 10 |

### 2.2.3 Remote Analog Meter Calibration

If the remote analog meter option was purchased and the meter is connected, calibrate meter as follows:
a. Remove logic 2 card and logic 4 card from locations A4 and A8.
b. Place preset card on extender cardin location A6.
c. Using jumper wire, connect collector of Q9 to GRD terminal on preset card.
d. Set POWER switch to ON.
e. Using adjustment located on remote meter panel, adjust remote meter reading to 18. The polarity depends on the signal stored in A1A5A53 when the logic 2 card is removed.
f. Set POWER switch to OFF.
g. Remove jumper wire from Q9 and GRD terminal.
h. Remove extender card and place preset card back in card cage.

### 2.2.4 Installation Checks

## Note

The following procedure does not check calibration of the monitor frequency standard. Refer to calibration procedure for oscillator adjustment.

If a self-check card has been purchased, check monitor operation after installation per the following procedure.
a. Remove preset card from location A6, insert self-check card in location A6, and remove rf card from location A1.
b. Connect jumper wire from logic 1, TP1, to logic 2, TP5.
c. Set POWER switch to ON and MODE switch to UNMOD CARR.
d. Rotate self-check card frequency error switch through each of the five positions and observe error display indications of $-1.6,-.8,-.0$, +.8 , and +1.6 .
e. Set MODE switch to MOD CARR and repeat step d.


Figure 2-1. Rear Panel Connections.

Table 2-2. Preset Card Wiring Table.

| TRANSMITTER FREQUENCY (MHz) | PRESET CARD TERMINAL NUMBER |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 |
| 88.1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 88.3 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 88.5 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 88.7 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 88.9 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 89.1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 89.3 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 89.5 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 89.7 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 89.9 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 90.1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |

Table 2-2. Preset Card Wiring Table (Cont).

| TRANSMITTER FREQUENCY (MHz) | PRESET CARD TERMINAL NUMBER |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 |
| 90.3 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 90.5 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 90.7 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 90.9 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 91.1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 91.3 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 91.5 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 91.7 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 91.9 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 92.1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 92.3 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 92.5 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 92.7 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 92.9 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 93.1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 93.3 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 93.5 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 93.7 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 93.9 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 94.1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 94.3 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 94.5 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 94.7 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 94.9 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 95.1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |

Table 2-2. Preset Card Wiring Table (Cont).

| TRANSMITTER FREQUENCY ( MHz ) | PRESET CARD TERMINAL NUMBER |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 |
| 95.3 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 95.5 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 95.7 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 95.9 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 96.1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 96.3 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 96.5 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1. | 0 | 1 | 1 | 1 | 0 |
| 96.7 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 96.9 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 97.1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 97.3 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 97.5 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 97.7 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 97.9 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 98.1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 98.3 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 98.5 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 98.7 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 98.9 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 99.1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 99.3 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 99.5 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 99.7 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 99.9 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 100.1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |

Table 2-2. Preset Card Wiring Table (Cont).

| TRANSMITTER FREQUENCY ( MHz ) | PRESET CARD TERMINAL NUMBER |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 |
| 100.3 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 100.5 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 100.7 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 100.9 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 101.1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 101.3 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 101.5 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 101.7 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 101.9 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 102.1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 102.3 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 102.5 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 102.7 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 102.9 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 103.1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 103.3 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 103.5 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 103.7 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 103.9 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 104.1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 104.3 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 104.5 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
|  |  | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 |

Table 2-2. Preset Card Wiring Table (Cont).

| TRANSMTTTER FREQUENCY (MHz) | PRESET CARD TERMINAL NUMBER |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 |
| 104.7 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 104.9 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 105.1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 105.3 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 105.5 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 105.7 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 105.9 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 106.1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 106.3 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 106.5 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 106.7 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 106.9 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 107.1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 107.3 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 107.5 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 107.7 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 107.9 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |

## section

### 3.1 PANEL CONTROLS AND INDICATORS

This section locates, illustrates, and describes the function of each front panel control. Refer to figure 3-1 and table 3-1.

### 3.2 OPERATING INSTRUCTIONS

To operate monitor, set POWER switch to ON. There is no delay or warmup time required; however, disregard the first one or two error displays to allow the counting circuits to stabilize. Set MODE switch to MOD CARR. This is the normal mode of operation for the monitor when the transmitter signal is modulated. The error readout is updated every 11 seconds. The UNMOD CARR mode of operation, with a 2 -second update time, is usually used when adjusting transmitter frequency. The $19-\mathrm{KHZ}$ PILOT mode of operation, with an 11 -second update time, is used to check multiplex pilot-carrier frequency drift. When switching the monitor mode of operation, disregard the first one or two error displays to allow the counting circuits to stabilize. The greater-than-$2.0-\mathrm{kHz}$ alarm is protected from transient operation when switching monitor mode of operation or when turning power on.

## Note

Do not use the MODE switch $19-\mathrm{KHZ}$ PILOT position if there is no $19-\mathrm{kHz}$ input. If the monitor MODE switch is
inadvertently set to the $19-\mathrm{KHZ}$ PILOT position without a $19-\mathrm{kHz}$ pilot carrier present, the greater-than $-1.0-\mathrm{kHz}$ alarm indicator will light; however, the error display and greater-than $-2.0-\mathrm{kHz}$ alarm will be inhibited.

### 3.3 TRANSMITTER FREQUENCY ADJUSTMENT

If the transmitter frequency drifts, the transmitter frequency may be adjusted.

### 3.3.1 Unmodulated Carrier Adjustment

a. Set MODE switch to UNMOD CARR position for 2-second update time.
b. Observe display and adjust transmitter frequency until display indicates zerofrequency error.

### 3.3.2 Modulated Carrier Adjustment

a. Set MODE switch to MOD CARR position for 11-second update time.
b. Observe display and adjust transmitter frequency until display indicates zerofrequency error.

### 3.4 19-kHz PILOT CARRIER ADJUSTMENT

Adjust the pilot carrier by setting the MODE switch to $19-\mathrm{KHZ}$ PILOT and adjusting pilot carrier frequency until monitor display indicates zero frequency error.

Table 3-1. Controls and Indicators.

| NAME | PANEL <br> MARKING | FUNCTION |
| :---: | :---: | :---: |
| Power switch <br> Mode switch | $\begin{aligned} & \text { POWER } \\ & \text { ON } \\ & \text { OFF } \\ & \text { MODE } \end{aligned}$ | Turns monitor on and off. |
| Mode switch | MOD CARR <br> UN MOD CARR <br> 19 KHZ PILOT | Selects 10 -second sample mode. Selects 1 -second sample mode. Selects 10 -second sample mode for $19-\mathrm{kHz}$ pilot carrier. |
| ```Frequency-error- greater-than-1-kHz indicator lamp``` | FREQUENCY ERROR $>1.0 \mathrm{kHz}$ | Indicates frequency error of more than 1 kHz in MOD or UMOD CARR position, or more than 1 Hz in 19 KHZ PILOT position. |
| ```Frequency-error- greater-than-2-kHz indicator lamp``` | FREQUENCY ERROR $>2.0 \mathrm{kHz}$ | Indicates frequency error of more than 2 kHz in MOD or UMOD CARR position, but does not operate in the 19 KHZ PILOT position. |
| Frequency-error readout screen | FREQUENCY ERROR KHZ | Displays frequency error from 0 to $\pm 2.0 \mathrm{kHz}$ in MOD or UNMOD CARR position, or 0 to $\pm 2.0 \mathrm{~Hz}$ in 19 KHZ PILOT position. |



Figure 3-1. Panel Controls and Indicators.

## section

principles of operation

### 4.1 GENERAL

The $54 \mathrm{~N}-1$ FM Frequency Monitor uses integrated circuits to perform the digital counting, decoding, readout, and gate functions.

The frequency monitor uses positive logic; that is, a logic 1 always more positive than a logic 0 . The logic states are represented by the following voltages:

Logic 1: nominally 1.0 vdc
Logic 0 : nominally 0.3 vdc

### 4.2 INTEGRATED CIRCUITS

The following paragraphs present a general description of the integrated circuits used in the frequency monitor.

### 4.2.1 Fairchild 923 JK Flip-Flop

The Fairchild Micrologic 923JK flip-flops are used as storage elements, counters, and dividers. Refer to figure 4-1 for schematic diagram, logic symbol, and truth table. The JK flip-flops differ from ordinary flip-flops in that no ambiguous output state can result from simultaneous logic 1 inputs. There are only two output conditions: pin 7 is logic 1 while pin 5 is logic 0 , and pin 7 is logic 0 while pin 5 is logic 1. The flip-flop changes state on the negative transition of a clock pulse (at pin 2), or a logic 1 applied at pin 6. Simultaneous logic 0 signals on the SET (pin 1) and CLEAR (pin 3) inputs allow the output at pins 5 and 7 to toggle (reverse) when the clock pulse is applied. With logic 1 inputs on the SET and CLEAR pins, the output at pins 5 and 7 will not change with the clock input. A logic 1 on pin 1 and logic 0 on pin 3 changes the output at pin 7 to logic 1, and pin 5 to logic 0 at the next clock pulse. A logic 0 on pin 1 and logic 1 applied to pin 6 presets the output at pin 7 to logic 0 regardless of the clock input or the logic levels on pins 1 and 3.

### 4.2.2 Dual 2-Input NOR Gate

The Fairchild Micrologic 914 is a dual 2 -input NOR gate. When any one or more inputs to a NOR gate is a logic 1, the output is a logic 0 . Refer to figure 4-2 for schematic, logic symbols, and truth tables. Each NOR gate may be used separately as a 2 -input gate, or the output pins ( 6 and 7 ) may be tied together to form a 4 -input gate. In the gate function operation, assume a logic-1 input at pin 2 and a squarewave input at pin 1 . The output at pin 7 remains at a logic 0 , because of the logic-1 input at pin 2, and blocks the square-wave input at pin 1. When the input at pin 2 changes to logic 0 , the square wave at pin 1 is passed by the gate. Any input pins not used are tied to ground (logic 0 ). The dual 2 -input gate is also used as a set/ reset flip-flop by external crosscoupling (pin 6 to pin 2 and pin 7 to pin 3). (The control pulses are applied to pins 1 and 5.)

### 4.2.3 Buffer Element

The Fairchild Micrologic 900 Buffer is an inverting driver capable of supplying 16 ma at 0.9 vdc . Refer to figure 4-2 for schematic, logic symbol, and truth table. The buffer is used as a line driver to increase fanout, as a buffer to provide isolation, or as an inverting amplifier. Fanout refers to the number of integrated circuits that a device can drive. A logic 1 at pin 3 produces a logic 0 output at pin 5 , and a logic 0 at pin 3 produces a logic 1 output at pin 5.

### 4.2.4 Sylvania JK Flip-Flop

The Sylvania SF53 and SF253 are AND input JK flip-flops used as frequency dividers in the rf section. Refer to figures 4-3 and 4-4 for schematics and truth tables. The JK flip-flops differ from ordinary flip-flips in that no ambiguous output state can result from simultaneous logic 1 or logic 0 inputs on the $J$ and $K$ inputs. Simultaneous logic 1 signals allow the flip-flop to toggle with the clock input, and simultaneous logic 0


| TRUTH TABLE |  |  |
| :---: | :---: | :---: |
| SET | CLEAR | OUTPUT |
| PIN I | PIN 3 | PIN 7 |
| 1 | 1 | $x^{n}$ |
| 1 | 0 | 1 |
| 0 | 1 | 0 |
| 0 | 0 | $\frac{X^{n}}{}$ |

$X$ IS THE OUTPUT STATE AT TIME $n_{1}$ $I=$ HIGH
$\mathrm{O}=\mathrm{LOW}$


Figure 4-1. Fairchild 923 JK Flip-Flop Schematic.
inputs inhibit toggling. Information is applied to the $J$ and/or $K$ terminals while the clock is at logic 0 . This new information is ANDed with the present state of the flip-flop and stored in the depletion region of a diode when the clock changes to logic 1. When the clock returns to logic 0 , the stored information is ANDed with the inverted clock, causing the cross-coupled NAND gates to set. Asynchronous SET, PRESET, and RESET inputs are used for setting the flip-flop independently of the clock. Unused J and/or K inputs may be tied to Vcc ( 2.0 to 5.0 vdc ) or to the clock. Unused SET and/or PRESET inputs may be tied to Vcc ( 2.0 to 5.0 vdc ) or to
the $\bar{Q}$ output. The unused RESET input may be tied to Vcc ( 2.0 to 5.0 vdc ) or to the Q output.

### 4.3 MONITOR PRINCIPLES OF OPERATION

The following paragraphs are keyed to the functional diagram in figure 7-1. When they are preset, the signals (figure 7-1) with a bar across the top are logic 0 and the signals without a bar are logic 1.

### 4.3.1 Frequency Divider Network

The $3-\mathrm{MHz}$ crystal oscillator output applied to the shaper is formedinto a square wave and applied

FAIRCHILD MICROLOGIC 914 DUAL TWO INPUT NOR GATE


TRUTH TABLE
PINS 6 AND 7 CONNECTED


TRUTH TABLE
PINS 6 AND 7

|  |  | OUTPUT PINS |
| :---: | :---: | :---: |
| 1 | 2 | 7 |
| 0 | 0 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |
| 0 | 1 | 0 |
| INPUT PINS |  | OUTPUT PINS |
| 3 | 5 | 6 |
| 0 | 0 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |
| 0 | 1 | 0 |




Figure 4-2. Fairchild 914 Dual 2-Input Gate and 900 Buffer Schematic.


Figure 4-3. Sylvania SF253 JK Flip-Flop Schematic.

| TRUTH TABLE |  |  |  |
| :---: | :---: | :---: | :---: |
| $J$ | $K$ | $Q_{n}$ | $Q_{n}+1$ |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

$Q_{n}=$ OUTPUT AT PIN K PRIOR TO CLOCK PULSE AT PIN $C$
$0_{n}+1=$ OUTPUT AT PIN K AFTER A CLOCK PULSE AT PIN $C$
$J=J_{1} \cdot J_{2} \cdot J_{3}$
$K=K_{1} \cdot K_{2} \cdot K_{3}$
$I=$ HIGH
$O=$ LOW
0 : LOW

Figure 4-4. Sylvania SF53 JK Flip-Flop Schematic.
to a divide-by-3 flip-flop network (figure 7-1) that produces two $1-\mathrm{MHz}$ outputs. One output, from the divide-by- 3 network, is fed to a buffer and then to an rf connector on the rear panel. The other $1-\mathrm{MHz}$ output is applied to a divide-by -4 flip-flop network. The resulting $250-\mathrm{kHz}$ signal is divided twice by 25 to obtain first a $10-\mathrm{kHz}$ signal, then a $400-\mathrm{Hz}$ signal. The $400-\mathrm{Hz}$ signal is applied to a divide-by-50 flip-flop network to obtain an $8-\mathrm{Hz}$ signal that is applied to a divide-by-8 network. The divide-by-8 network provides 4-, 2-, and $1-\mathrm{Hz}$ output signals to the timing pulse generator logic. The $1-\mathrm{Hz}$ signal is also applied to a divide-by-2-or-11 network that provides a 1or 10 -second sample time with a 1 -second readout time.

### 4.3.2 Timing Pulse Generator

The 8-, 4-, 2-, and 1-Hz signals, derived from the divider network (figure 7-1), are used to establish the 1 -second and $10-$ second sample, readout, and timing pulses required for the sampling and processing operation.

One output of the $1-\mathrm{Hz}$ signal is divided by 2 or 11 , depending on the MODE switch position, to produce a sample time of 1 (UNMOD CARR) or 10 (MOD CARR) seconds with a 1-second off-time for sample-count processing and display updating. The SAMPLE signal is applied to a count-gate matrix to control the rf-input sample time.

A second $1-\mathrm{Hz}$ signal, from the divide-by- 8 network, is combined with $4-, 2-$, and $1-\mathrm{Hz}$ signals to generate timing pulses that perform sequential operations during the 1 -second off-time. Refer to figure 5-2. These pulses, spaced over the 1 -second off-time, are 80 ms in duration, with 45 ms between pulses. The pulses are identified as P1, (P1), $\overline{\mathrm{P} 2}, \mathrm{P} 3, \mathrm{P} 4, \overline{\mathrm{P} 4}, \overline{\mathrm{P} 5}, \mathrm{P} 6$, and $\overline{\mathrm{P} 6}$ and are discussed in the following paragraphs as they are used.

### 4.3.3 RF Circuit

The rf input frequency (figure 7-7) (from the transmitter) is divided by 2 in the first parametric divider and, due to losses in the first divider, amplified by Q1 and Q2. The signal is again divided by 2 in the second parametric divider and, due to losses in the second divider, amplified by Q3 and shaped by Q4. Transistor Q4 provides the square-wave output required by the first integrated circuit divide-by-5 network. The output of the first divide-by-5 network is applied to the second divide-by-5 network. The signal, now
divided by 100 , is applied to transistor Q5, which conditions the divided rf pulse train to the monitor logic 1 and logic 0 levels.

The signal presence circuit prevents the monitor from activating an alarm when there is no transmitter rf input. An output signal from flip-flop A1 is applied to a voltage doubler consisting of diodes CR1 and CR2 and capacitors C14 and C15. This causes transistor Q6 to conduct and provide the logic 0 SIGNAL PRESENCE signal that is applied to the alarm and display circuits. Loss of the rf input shuts off transistor Q6 and provides a logic 1 that inhibits the alarm and display circuits. When the MODE switch is in the 19 KHZ PILOT position, a logic 1 is applied to the base of transistor Q6 through resistor R21 to supply a constant logic 0 SIGNAL PRESENCE signal. This prevents the loss of the signal presence signal, if the rf input is not present while monitoring the pilot carrier frequency.

### 4.3.4 Count-Gate Matrix

The count-gate matrix (figure 7-1) directs the SHAPED RF input through the 1 -second or 10 second gates as selected by the MODE switch position.

The MODE switch MOD CARR position applies a logic 1 to the count-gate matrix that disables the 1 -second gate A1A4A.2. The logic 1 applied to A1A4A1 causes a logic 0 output that enables the round-off circuit and the $10-$ second gate A1A4A13, and causes the divide-by-2-or-11 circuit to supply an 11 -second period (containing a logic 0 sample time of 10 seconds and a logic 1 read time of 1 second) to the count-gate matrix rf gates A1A4A3, A2, and A7. The decade counter output gate A1A4A13 is disabled during readout time by set/reset flip-flop A1A4A8. The MODE switch UNMOD CARR position applies a logic 0 to the count-gate matrix that enables the 1-second gate A1A4A2. The logic 0 applied to A1A4A1 causes a logic 1 output that disables the round-off circuit and decade counter output gate A1A4A13, and causes the divide-by-2 or-11 circuit to supply a 2 -second period (containing a logic 0 sample time for 1 second and a logic 1 readtime for 1 second) to the count-gate matrix rf gates A1A4A2, A3, and A. 7.

### 4.3.5 Decade Counter

The decade counter (figure 7-1) is a ring counter that produces one output pulse for every 10 input
pulses. The decade counter receives the rf pulse train from the count-gate matrix and applies the divided-by-10 output (from pin 7 of A1A4A25) to the output gate A1A4A13. Sampling the input pulses for 10 seconds and dividing by 10 permits frequency count round-off that reduces count-gate ambiguity. At the end of the sample period, the decade counter output is inhibited by a P3 pulse. During the readout time, the count remaining in the decade counter is examined by the round-off circuit; it if is five or more, another count is added to the binary counter. A count of five or more is logic 0 at A1A4A25 pin 5 . The decade counter is cleared (logic 0 at pins 7 and logic 1 at pins 5) prior to each sample period by a logic 1 on pins 6 at P1 time.

### 4.3.6 Round-Off Circuit

The round-off circuit (figure 7-1) rounds off the frequency count to the nearest whole cycle when the monitor is operating in the 10 -second sample mode. The round-off circuit is enabled by a logic 0 from A1A4A1, a logic 0 from the MODE switch, and a logic 0 (five or greater count) from the decade counter A1A4A25 pin 5. With the three ENABLE signals present during readout time, a logic 0 (from the timing pulse generator) at P4 time adds one count to the binary counter. The round-off circuit is disabled when the MODE switch is set to the UNMOD CARR position by a logic 1 from A1A4A1. In the 19 KHZ PILOT mode, a logic 1 applied from the MODE switch disables the round-off circuit.

### 4.3.7 Binary Counter Gate

The binary counter gate (figure 7-1) is a 4 -input NOR gate that supplies the binary counter with all count pulses. The four inputs are: 1 - or 10 -second rf count pulses, the round-off pulse, and the positive polarity pulse. To add a count to the binary counter, a logic 1 pulse is applied to the input, providing a logic 0 output pulse to the binary counter.

### 4.3.8 Binary Counter Preset

To count from a maximum of 1.08 MHz (the rf carrier is divided by 100 in the rf circuit) 21 flip-flops are required and 18 flip-flops are wired for preset (figure 7-1). The three lowest order flip-flops are always set to zero at P1 time by a logic 1 and are not wired to the preset card A1A6. The preset card is wired (by the customer) to the binary equivalent of the trans-
mitter frequency that it will monitor. Preset occurs at P2 time when a logic 0 is applied to A1A6 pin 19. This applies a logic 1 to pin 6 of all binary counter flip-flops that are connected to A1A6 terminal 19. For $19-\mathrm{kHz}$ operation, refer to paragraph 4.3.15.

### 4.3.9 Binary Counter

The binary counter (figure 7-1) counts backward from a binary number that represents the transmitter frequency during a precise time period. Prior to a sample period, the binary counter flip-flops are set at P1 time by a logic 1 pulse, and preset at P2 time to the binary number representing the transmitter frequency. During a sample period, each pulse from the binary counter gate decreases the number in the binary counter by one. At the end of a sample period, all flip-flops will be set to zero if the transmitter frequency is correct. A negative error results if the counter does not reach zero, and a positive error results if the counter passes zero. The error count and polarity of error are examined by the detector and storage circuits.

### 4.3.10 Detector and Storage Circuits

The detector and storage circuits (figure 7-1) analyze the states of all 21 flip-flops in the binary counter to determine polarity and magnitude of frequency error, and store the information for display during the next sample period. The polarity detector consists of two 16 -input NOR circuits with the outputs applied to polarity storage flip-flops A1A5A52 and 53 and the greaterthan -10 and greater-than-20 error detectors. Pins 5 of the last 16 flip-flops in the binary counter are connected to one 16 -input NOR gate. Pins 7 are connected to the other 16 -input NOR gate. When there is a negative frequency error, the 16 flip-flop outputs from all pins 5 are logic 1 and the outputs at all pins 7 are logic 0 . For a negative frequency error the following conditions exist: a logic 0 input to A1A5A52 pin 3 and a logic 1 input to A52 pin 1, a logic 1 input to A1A5A53 pin 3 and a logic 0 input to A53 pin 1. At P6 time flip-flops A52 and A53 are updated by a $\overline{\mathrm{P} 6}$ pulse. This provides a logic 1 from A1A5A54 pin 7 to transistor A1A9A2 Q9 lighting the negative-error display lamp, and a logic 0 from A1A5A51 pin 6 to transistor A1A9A2 Q4 inhibiting the positive-error display
lamp. When there is a positive frequency error, the outputs of the binary counter flip-flops are reversed (pins 5 logic 0 and pins 7 logic 1 ), the storage circuit outputs are reversed, the positiveerror lamp lights and the negative-error lamp is inhibited.

If the logic levels on pin 5 of the last 16 binary counter flip-flops are not the same, the frequency error is $3.2-\mathrm{kHz}$ or greater, and the outputs of both 16 -input NOR gates are logic 0 . The logic 0 outputs are inverted to logic 1 through A1A5A26 and are applied to the greaterthan $-1.0-$ and $-2.0-\mathrm{kHz}$ error detectors A1A5A31 and A36. The error detectors provide a logic 1 from A1A5A41 to the greater-than-1.0-and-2.0kHz alarm storage flip-flops A1A8A9 and A10.

The error signals for display (from the first five binary counter flip-flops) are applied to the display storage circuits. The error signals are also examined by NOR gates A1A4A16, 17, 18, and 19, which are part of the greater-than-$10-$ and $-20-\mathrm{Hz}$ error detectors. The display error signals are loaded directly into the storage flipflops by a logic 0 applied to the storage circuit NOR gates at P5 time. The output signals from the storage flip-flops are partially combined, buffered, and applied to the binary-to-decimal decode circuit.

For all positive errors, an additional pulse is added to the binary counter. This pulse is required because the counter transition through zero requires an extra pulse from the rf input pulse train. This pulse is added by clocking the binary counter at P5 time with logic 0 signals $\overline{P 5}$ and $\overline{P P}$, and storing the new number in the storage flip-flops during P5 time. The stored binary number, for positive frequency errors, is inverted for proper decoding in the code converter. This is accomplished by toggling the display storage flip-flops at P6 time with logic 0 signals $\overline{\mathrm{P}}$ and $\overline{\mathrm{PP}}$.

### 4.3.11 Decode Circuit

The decode circuit (figure 7-1) receives binary error signals from the storage circuits, decodes the signals, and lights the decimal equivalent lamp. Assume logic 0 on A1A8 input pins 5, 10, 12, and 14, and logic 1 on A1A8 input pins 1, 2, $3,4,6,15$, and 18 . The four logic 0 signals only enable 4 -input gate A1A8A36. The resulting logic 1 output of A1A8A36 is inverted twice by A38.

The logic 1 output from A1A8A38 pin 6 enables transistor A1A9A2 Q7 that lights the .5 (hundreds) lamp.

### 4.3.12 External Readout Signals

The external readout signals (figure 7-1) are digital and, as an option, analog. The binary digital signals are obtained directly from the storage circuits on A1A4 pins $9,24,26,25$, and 33 and applied to A1A10 logic for conditioning. The digital readout signals are: SAMPLE 10, ENABLE, $2^{0}, 2^{1}, 2^{2}, 2^{3}, 2^{4}$, POSITIVE POLARITY, NEGATIVE POLARITY, and $19-\mathrm{KHZ}$ OPERATE.

The analog output is derived by applying the digital signals to the analog output converter. The analog output signal is determined by the transistor that is enabled and the current flow through the collector resistor. If more than one transistor is enabled, the collector currents are added, which results in a larger analog meter indication. The polarity of error is controlled by a NEGATIVE POLARITY STORED (NPS) signal that is logic 0 when frequency error is negative. When the frequency error is positive, the NPS signal changes to a logic 1 enabling transistor A1A6Q2, which energizes relay A1A6 K1. This changes the analog meter movement to indicate a positive-error signal. The analog output is inhibited during display update time by a logic 1 signal to transistor A1A6 Q3 that cuts off transistor Q1. If the error is greater than 2.0 kHz , the greater-than $-2.0-\mathrm{kHz}$ alarm signal enables transistor A1A6 Q10, which disables transistor Q1 and pegs the remote meter.

### 4.3.13 Alarm Circuits

The alarm circuits (figure 7-1) receive the greater-than-1.0-and $-2.0-\mathrm{kHz}$ error signals (refer to paragraph 4.3.10) from the greater-than-$1.0-$ and $-2.0-\mathrm{kHz}$ error detectors and at P 6 time, stores them in storage flip-flops A1A8A9 and A10. A logic 0 from flip-flop A1A5A9 pin 5, and a logic 0 SIGNAL PRESENCE signal from the rf circuit, produce a logic 1 from A1A8A14 pin 6 that enables transistor A1A9A2 Q5, which energizes relay A1A9A2 K1. A1A9A2 K1 relay contacts 6 and 7 light the greater-than $-1.0-\mathrm{kHz}$ alarm indicator, and contacts 9 and 10 close the greater-than-$1.0-\mathrm{kHz}$ external/remote alarm circuit. A logic 1 from flip-flop A1A8A9 pin 5 inhibits the greaterthan $-1.0-\mathrm{kHz}$ alarm relay by providing a logic 0 from A1A8A14 pin 6.

LAMP INHIBIT during display update is provided by a logic 1 signal at P4 time to A1A8A15 pin 3, which sets the output of A1A8A15 pin 7 to logic 1. This produces a logic 1 from A1A8A34 pin 5 that inhibits all readout signals. At P6 time, the set/ reset flip-flop A1A8A15 is reset by a logic 1 applied to A1A8A15 pin 2. The output at A1A8A15 pin 7 changes to logic 0 and provides a logic 0 at A1A8A34 pin 5 that enables all readout gates.

With an error of less than 2.0 kHz , the output of flip-flop A1A8A10 pin 5 is a logic 1 that inhibits the greater-than-2.0-kHz alarm signal from A1A8A14 pin 7, presets flip-flops A1A8A29 and A30 pins 5 through A1A8A19 and A24 to logic 1, and provides a logic 1 through A1A8A20 and A24 to pin 2 of flip-flop A1A8A29. With the first error count greater than 2.0 kHz , the output at pin 5 of flip-flop A1A8A10 changes, at P6 time, to logic 0. This enables one input of A1A8A14, removes the logic 1 preset at pins 6 of flip-flops A1A8A29 and A30, and applies logic 0 to A1A8A20 pin 1. At P2 time, a logic 0 applied to A1A8A20 pin 2 clocks flip-flop A1A8A29. With the second greater-than-$2.0-\mathrm{kHz}$ count, the output of flip-flop A1A8A10 pin 5 remains logic 0 , and the logic 0 P2 pulse clocks flip-flop A1A8A29, which then clocks flipflop A1A8A30. With the third greater-than-2.0kHz count, the output of flip-flop A1A8A10 pin 5 remains logic 0, and the logic 0 P2 pulse clocks flip-flop A1A8A29. This provides two logic 0 outputs from flip-flops A1A8A29 and A30 to A25 pins 3 and 5. The logic 1 output from A1A8A25 pin 6 disables the flip-flop input gate A1A8A20, and provides a logic 1 output (greater-than-2.0kHz alarm) from A1A8A14 pin 7 that enables transistor A1A9A2Q24, which energizes relay A1A9A2K2. A1A9A2 K2 relay contacts 6 and 7 light the greater-than $-2.0-\mathrm{kHz}$ alarm indicator, and contacts 9 and 10 close the greater-than-2.0kHz external/remote alarm/interlock circuit.

If a logic 1 SIGNAL PRESENCE and/or a TRANSIENT INHIBIT signal is applied to A1A8A19, the inhibit flip-flops preset to the zero state and remain in this state until the signal is removed. The greater-than- $2.0-\mathrm{kHz}$ logic 1 signal from A1A8A10 pin 7 provides a LAMP INHIBIT signal that inhibits all display circuits for errors over 2.0 kHz .

### 4.3.14 Power Supply

The power supply (figure 7 -8) provides regulated and filtered $3.7 \mathrm{vdc}, 20 \mathrm{vdc}$ and 5.1 vdc for
monitor transistor circuits, and unregulated 5.5 vdc for indicator and alarm display circuits.

The 20 -vdc power supply is a full-wave rectifier consisting of diodes CR10 and CR11 and capacitor C7. The voltage output is regulated at 20 vdc by VR12. The 5.5 -vdc power supply is a full? wave rectifier consisting of diodes CR8 and CR9 and capacitor $C 6$. The 5.1 -vdc power supply is a full-wave rectifier consisting of diodes CR4 and CR5 and capacitor C3, with the voltage regulated at 5.1 vdc by VR3. The 3.7 -vdc power supply is a full-wave rectifier with a series regulator. The rectifier consists of diodes CR6 and CR7 and capacitors C 4 and C 5 ; the series regulator consists of transistors Q3 and Q4, which are controlled by transistors Q1 and Q2. If the series regulator fails, VR2 limits the voltage to 5.1 volts to protect the integrated circuits.

### 4.3.15 19-kHz Pilot Operation

Monitor operation in the $19-\mathrm{KHZ}$ PILOT mode (figure 7-1) is similar to the MOD CARR mode. Only the differences in operation are explained in the following paragraphs. The visual display in this mode of operation is $\pm 2$ in $0.1-\mathrm{Hz}$ increments.

The MODE switch 19-KHZ PILOT position supplies two constant logic 1 levels that control monitor gate functions. A logic 1 from MODE switch S1 pin 7 applied to the count-gate matrix enables the $10-$ second sample mode of operation. The second logic 1 level from MODE switch S1 pin 1, applied to A1A9A2 CR6 and R19, performs the following gate switching: disables the round-off circuit and the decade counter output gate A1A4A13, disables the transmitter frequency preset gate A1A6A14, enables the $19-\mathrm{kHz}$ gate A1A4A7 after inversion to a logic 0 from A1A4A6 pin 7, and enables the $19-\mathrm{kHz}$ preset gate A1A6A7. The logic 1 19KHZ OPERATE signal applied to transistor A1A9A2 Q19 disables Q17, and applies a constant logic 1 TRANSIENT INHIBIT PULSE to the greater-than $2.0-\mathrm{kHz}$ inhibit circuit. This prevents transmitter alarm/interlock operation if the pilot carrier frequency is out of tolerance. The logic $119-\mathrm{KHZ}$ OPERATE signal applied to the rf circuit disables the signal presence circuit (refer to paragraph 4.3.3).

The $19-\mathrm{kHz}$ pilot carrier is applied to a shaper circuit consisting of A1A6 Q11 and Q12 that amplifies the carrier, and applies the carrier to a clamping and limiting circuit, consisting of diode A1A6 CR4 and transistor A1A6 Q13.

The $19-\mathrm{kHz}$ pulse train is applied to the $19-\mathrm{kHz}$ gate A1A4A7, and is gated to the binary counter gate during the 10 -second sample time. Logic circuits on the preset card preset the binary equivalent of $190,000 \mathrm{~Hz}$ into the binary counter by a logic 0 at P2 time.

### 4.3.16 782B-1 Self-Check Card

The self-check card (figure 7-9) checks the monitor counting circuits by presetting an error count
in the binary counter and counting a $1-\mathrm{MHz}$ reference signal. At P2 time, the self-check cardpresets the binary counter to 999,984; 999,992; $1,000,000 ; 1,000,008$; or $1,000,016$, depending on the error switch position. The $1-\mathrm{MHz}$ reference, jumpered between logic 1 card A1A2 TP1 and logic 2 card A1A4 TP5, clocks the binary counter. When the monitor is operating properly, the resulting error readouts will be $-1.6,-.8,-.0$, +.8 , or +1.6 KHZ , depending on the error switch position.

### 5.1 PREVENTVE MAINTENANCE

There is no preventive maintenance required for the monitor.

### 5.2 CORRECTIVE MAINTENANCE

Monitor corrective maintenance is limited to calibration and lamp replacement, unless a circuit card fails. Refer to paragraph 5.4 for monitor calibration data. Refer to paragraph 5.5 for indicator lamp replacement data. Refer to paragraph 5.6 for general trouble analysis procedures.

## Caution

The monitor POWER switch must be set to OFF prior to removing or installing any circuit card or component.

### 5.3 SPARE PARTS

Spare parts may be ordered from the following address:

> Collins Radio Company
> Service Parts, 412-024
> 1225 North Alma Road
> Richardson, Texas 75080

### 5.4 CALIBRATION

Adjust the $3-\mathrm{MHz}$ oscillator standard as follows:
a. Tune a communication receiver to WWV test frequency of $5,10,15$, or 20 MHz .
b. Connect a coaxial cable to the monitor $1-\mathrm{MHz}$ output jack A2P2.
c. Position the coaxial cable close to the communication receiver antenna terminal.
d. Observe S-meter on receiver, or listen for the beat note caused by the difference in frequency between the harmonic of the $1-\mathrm{MHz}$ monitor standard and the WWV carrier frequency. For example: If the $1-\mathrm{MHz}$ monitor standard frequency is $0.2-\mathrm{Hz}$ high and the $10-\mathrm{MHz}$ WWV is tuned in, the beat note is 0.2 times

10 or 2 Hz . If the $20-\mathrm{MHz}$ WWV carrier is tuned in, the beat note is 0.2 times 20 or 4 Hz .
e. Adjust the monitor $3-\mathrm{MHz}$ oscillator until the $1-\mathrm{MHz}$ standard beat note is less than $1 / 2 \mathrm{~Hz}$. This adjusts the monitor to within $0.1-\mathrm{Hz}$ error when using the $5-\mathrm{MHz}$ WWV carrier reference. The $1-\mathrm{MHz}$ standard frequency can be adjusted closer when using the higher WWV carrier frequencies.

### 5.5 INDICATOR LAMP REPLACEMENT

### 5.5.1 Alarm Indicator Lamp Replacement

Remove alarm indicator cover and replace lamp.

### 5.5.2 Readout Assembly Lamp Replacement

The lamps are mounted on two removable readout modules housed in the readout assembly. When the readout assembly (figure 5-1) in the control module is viewed from the back, the hundreds indicators are in the left-hand readout module, and the thousands, positive, and negative indicators are in the right-hand readout module. Each readout module is numbered with lamp and terminal designations. Determine which readout module to remove and which lamp to replace the table 5-1 before starting the replacement procedure. Replace indicator lamps as follows:
a. Remove two screws from readout module and carefully pull it straight back from readout assembly.
b. Replace lamp.
c. Replace readout module.

### 5.6 TROUBLE ANALYSIS

Circuit malfunctions can be isolated to a circuit card by using an oscilloscope and circuit card test points. Indicator lamp failures can be isolated by lamp substitution.
Use the functional diagram, figure 7-1, as an aid in localizing faults. Test points on the ends of the cards are accessible with the cards plugged into the monitor. The card extender provides access to components on individual cards.


Figure 5-1. Readout Assembly Rear View.

Circuit card test-point indications are listed in table 5-2. The signals are either logic 1 or logic 0 . The amplitude of a logic 1 is typically 1 vdc and the amplitude of a logic 0 is 0.3 vdc or less. These voltages are typical and will vary, but a logic 1 should never be below 0.85 vdc or a logic 0 be above 0.46 vdc. If the specified indication is not obtained at a test point, refer to the schematics in section 7 to isolate the malfunction. Some indications in table $5-2$ will be a different frequency for each monitor; however, the relationship given in the table will remain constant. To obtain total time between $P$ time pulses, add 1 -second or 10 -second sample time as indicated by the MODE switch position (UNMOD CARR position is 1 -second sample, MOD CARRposition is 10 -second sample, and 19 KHZ PILOT position is 10 -second sample). The amplitudes of waveforms in table 5-2 and figure 5-2 are logic 1 or logic 0 .

The following paragraphs present possible malfunction indications and general procedures to follow for malfunction isolation. If required, detailed troubleshooting is performed by using an oscilloscope, extender card, and by referring to the detailed schematics in section 7 .

## Caution

When making repairs on the circuit cards, do not use a soldering iron rated at more than 40 watts. Do not jar or strike a card to remove excess solder.

### 5.6.1 Error Display and Warning Indicators Not Lighted

a. Check rf cable input at rear of monitor for rf input (refer to paragraph 2.2.5 for parameters).
b. Check $19-\mathrm{kHz}$ pilot carrier input at rear of monitor.
c. Check $1 / 2 \mathrm{amp}$ fuse at rear of monitor.
d. Check 5 amp fuse in power supply module.
e. Check SHAPED RF and SIGNAL PRESENCE signals logic 2 card A1A4 (table 5-2).
f. Check power supply voltages (figure 7-8).

### 5.6.2 Greater-Than-2.0-kHz Alarm Lighted and Greater-Than-1.0-kHz Alarm Not Lighted

a. Check greater-than $-1.0-\mathrm{kHz}$ indicator lamp.
b. Check greater-than $-1.0-\mathrm{kHz}$ contact closure at terminals on rear of monitor terminal block pins 11 and 12.
c. Check greater-than $-1.0-\mathrm{kHz}$ STORED signal on logic 4 card A1A8 (table 5-2).

### 5.6.3 Greater-Than-2.0-kHz Alarm Lighted With Some Error Display

Check lamp inhibit circuit on logic 4 card A1A8 (figure 7-6).

### 5.6.4 Greater-Than-1.0-kHz Alarm Lighted With Error Display of 1.0 kHz or Less

a. Check logic levels in decoding circuit on logic 4 card A1A8 (figure 7-6).
b. Check lamp in thousands digit readout.

### 5.6.5 Error Display With No Polarity Indication

a. Check polarity signal on logic 4 card A1A8 (figure 7-6).
b. Check polarity lamps in readout assembly.

Table 5-1. Lamp-Number-to-Character-Display Conversion Chart.

| HUNDREDS INDICATORS |  | THOUSANDS, POSITIVE, AND <br> NEGATIVE INDICATORS |  |
| :--- | :--- | :--- | :--- |
| LEFT READOUT MODULE |  | RIGHT READOUT MODULE |  |
| LAMP NO. | CHARACTER | LAMP NO. | CHARACTER |
| TERMINAL | DISPLAY | TERMINAL | DISPLAY |
| 2 | .1 | 5 | + |
| 3 | .2 | 6 | - |
| 4 | .3 | 7 | 1 |
| 5 | .4 | 8 | 2 |
| 6 | .5 |  |  |
| 7 | .6 |  |  |
| 8 | .8 |  |  |
| 10 | .9 |  |  |
| 11 | .0 |  |  |



Figure 5-2. Control and Timing Pulse Waveforms.

Table 5-2. Test Point Indications.

| CIRCUIT CARD | $\begin{aligned} & \text { TEST } \\ & \text { POINT } \end{aligned}$ | INDICATION |
| :---: | :---: | :---: |
| RF card A1A1 | TP1 | $\overline{\mathrm{SP}}(\overline{\text { SIGNAL PRESENCE }})$, logic 0 with rf carrier present or $19-\mathrm{kHz}$ operating mode. |
|  | TP2 | Shaped and divided by 100 rf output |
|  | TP3 | SHAPED RF signal divided by 20. |
|  | TP4 | SHAPED RF signal divided by 4 |
|  | TP5 | Ground |
| Logic 1 <br> A1A2 | TP1 | $1-\mathrm{MHz}$ square wave |
|  | TP2 | $8-\mathrm{Hz}$ square wave |
|  | TP3 | $\overline{P 6}$ timing pulse (figure 5-2) |
|  | TP4 | ENABLE (figure 5-2) |
|  | TP5 | $1-\mathrm{Hz}$ square wave |
|  | TP6 | Ground |
| Logic 2 <br> A1A4 | TP1 | P3 timing pulse (figure 5-2) |
|  | TP2 | 881,000 to $1,079,000$ pulses in 1 second or 10 seconds, dependent on MODE selector switch position, or _190,000 pulses in 10 seconds in 19 KHZ PILOT position |
|  | TP3 | $\overline{\mathrm{P} 5}$ timing pulse (figure 5-2) |
|  | TP4 | SAMPLE 10 (figure 5-2) |
|  | TP5 | SHAPED RF, divided by $100,881 \mathrm{kHz}$ to 1079 kHz , depending upon transmitter frequency |
|  | TP6 | Ground |
| $\begin{aligned} & \text { Logic } 3 \\ & \text { A1A5 } \end{aligned}$ | TP1 | 881,000 to $1,079,000$ pulses ( 1 - or 10 -second time span) divided by 8 , or 190,000 pulses in 10 seconds divided by 8 |
|  | TP2 | P1 timing pulse (figure 5-2) |
|  | TP3 | Logic 1 when POSITIVE POLARITY is stored |
|  | TP4 | Logic 1 when NEGATIVE POLARITY is stored |
|  | TP5 | (P1) timing pulse (figure 5-2) occurs at the same time as P1 |
|  | TP6 | Ground |
| Logic 4 <br> A1A8 | TP1 | $>+10$ STORED, logic 1 when error is greater than 1.0 kHz (or 1.0 Hz for 19 KHZ PILOT) |
|  | TP2 | $\overline{>} \pm 20$ STORED, logic 0 when error is greater than 2.0 kHz (or 2.0 Hz for 19 KHZ PILOT) |
|  | TP3 | P 6 timing pulse (figure 5-2) |
|  | TP4 | SIGNAL PRESENCE, logic 0 when rf signal is present, or MODE switch is in 19 KHZ PILOT position |
|  | TP5 | Not used |
|  | TP6 | Ground |

### 6.1 GENERAL


#### Abstract

This section contains a list of all replaceable electrical, electronic, and critical mechanical parts for the $54 \mathrm{~N}-1$ FM Frequency Monitor (758-5742-XXX).

The manufacturers' codes appearing in the MFR CODE column of the parts list are listed in numerical order at the end of the parts list. The code list provides the manufacturer's name and address as shown in the Federal Supply Code for Manufacturers' Handbook H4-1. Manufacturers not listed in Handbook H4-1 are assigned a 5-letter code and appear first in the code list.


### 6.2 LIST OF EQUIPMENT

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Figure 6-1. 54N-1 FM Frequency Monitor.



Figure 6-2. FMRF Card A1 (Sheet 1 of 2).


Figure 6-2. FMRF Card A1 (Sheet 2 of 2).

| SYMBOL | DESCRIPTION | MANUFACTURER'S PART NUMBER | $\begin{aligned} & \text { MFR } \\ & \text { CODE } \end{aligned}$ | COLLINS PART NUMBER |
| :---: | :---: | :---: | :---: | :---: |
| R8 | RESISTOR, FXD, COMPOSITION 33K OHMS, 108 TOL, $1 / 4$ WATT | RCO7GF333K | 81349 | 745-0803-000 |
| R9 | RESISTOR, FXD, COMPOSITION 560 OHMS, 10\% TOL, $1 / 4$ HATT | RCO7GF561K | 81349 | 745-0740-000 |
| R10 | RESISTOR, FXD, COMPOSITION 150 OHMS, 108 TOL, $1 / 4$ HATT | RCO7GF151K | 81349 | 745-0719-000 |
| R11 | RESISTOR, FXD, COMPOSITION 6.8 K DHM, $10 \% \mathrm{TOL}, 1 / 4$ hatt | RCO7GF682K | 81349 | 745-0779-000 |
| R12 | RESISTJR, FXD, COMPOSITION <br> 1K OHYS, $10 \%$ TOL, $1 / 4$ WATT | RCO7GF102K | 81349 | 745-0749-000 |
| R13 | RESISTOR, FXD, COMPOSITION <br> 47 JHMS, 108 TOL, $1 / 4$ HATT | RC07GF470K | 81349 | 745-0701-000 |
| R14 | RESISTJR, FXD, COMPOSITION 270 DHMS, $10 \%$ TOL, $1 / 4$ hatt | RCO7GF271K | 81349 | 745-0728-000 |
| R15 | RESISTOR, FXD, COMPOSITION 22K OHMS, $10 \%$ TOL, $1 / 4$ hatt | RCOTGF223 K | 81349 | 745-0797-000 |
| $\begin{aligned} & R 16 \\ & \text { R17 } \end{aligned}$ | SAME AS R 7 <br> RESISTOR, FXD, COMPOSITION 2.26 JHMS, 108 TOL, $1 / 4$ HATT | RC07GF222K | 81349 | 745-0761-000 |
| $\begin{aligned} & \text { R18 } \\ & \text { R19 } \end{aligned}$ | SAME AS R5 <br> RESISTOR, FXD, COMPOSI TION 3. $\boldsymbol{K}$ JHMS, $10 \%$ TOL, $1 / 4$ WATT | RCO7GF392K | 81349 | 745-0770-000 |
| R20 R21 | S AME AS R7 |  |  |  |
| R22 | SAME AS R7 |  |  |  |
| $R 23$ $R 24$ | SAME AS R11 SAME AS R11 |  |  |  |
| TP1 | JACK, TIP WHITE | 4877-125-9 | 17117 | 360-0434-100 |
| $\begin{aligned} & \text { TP2 } \\ & \text { TP3 } \\ & \text { TP4 } \end{aligned}$ | same is Tpl SAME AS TPI SAME AS TPI |  |  |  |
|  | JACX, TIP BL ACK | 4877-125-0 | 17117 | 360-0434-010 |



Figure 6-3. Logic 1 Card A2 (Sheet 1 of 2).


Figure 6-3. Logic 1 Card A2 (Sheet 2 of 2).



Figure 6-4. Logic 2 Card A4 (Sheet 1 of 2).


Figure 6-4. Logic 2 Card A4 (Sheet 2 of 2).



Figure 6-5. Logic 3 Card A5.



Figure 6-6. Preset 1 Card A6-1.

| SYMBOL | PRESCRIPTION | MANUFACTURER'S <br> PART NUMBER | MFR <br> CODE | COLLINS <br> PART NUMBER |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | PRESET CARD AG |  |  |  |  |
|  |  |  |  |  |  |



Figure 6-7. Preset 2 Card A6.


Figure 6-8. Preset 3 Card A6.





Figure 6-10. Logic 4 Card A8.

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Figure 6-11. FM Control Module A9 (Sheet 1 of 2).

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Figure 6-11. FM Control Module A9 (Sheet 2 of 2).




Figure 6-12. Lampdriver Board A9A1 (Sheet 1 of 2).


Figure 6-12. Lampdriver Board A9A1 (Sheet 2 of 2).

| SYMBOL | DESCRIPTION | MANUFACTURER'S PART NUMBER | $\begin{aligned} & \text { MFR } \\ & \text { CODE } \end{aligned}$ | COLLINS <br> PART NUMBER |
| :---: | :---: | :---: | :---: | :---: |
|  | LAMPDRIVER BOARD A SA 1 |  |  | 774-7116-001 |
| C1 | CAPACITJR, FXD, ELEC TRDLYTIC 300 UF, PLUS $75 \%$ MINUS 10\%, 6 VDCW | 30036266 | 56289 | 183-1189-000 |
| C2 | CAPACITJR, FXD, ELEC TROLYTIC 40 UF, PLUS 208 MINUS 15\%, 30 VDCH | 1090406 C2030 F2 | 56289 | 184-7781-000 |
| C3 | CAPACITJR, FXD, CERAMIC 0.33 UF, 208 TOL, 25 VDCH SAME AS C3 | 567A | 56289 | 913-3806-000 |
| CR1 | NOT USED |  |  |  |
| CR2 | SEmicovductor device, diode | 1 N914 | 07688 | 353-2906-000 |
| THROUGH: | SAME AS CR 2 |  |  |  |
| K1 | relay, armature <br> 2C COYTACT ARRANGEMENT | TP154CC6 | 70309 | 970-2451-230 |
| K2 | SAME AS K1 |  |  |  |
| 01 | TRANSISTOR | 2 N3569 | 07688 | 352-0629-030 |
| 02 | SAME AS Ql |  |  |  |
| 03 | TRANSISTOR | 2 N3567 | 07688 | 352-0629-010 |
| 04 | TRANSISTOR | 2 N3569 | 07688 | 352-0629-030 |
| THROUGH | Same AS Q3 |  |  |  |
| Q8 | SAME AS Q3 |  |  |  |
| 09 | SAME AS Q4 |  |  |  |
| 010 |  |  |  |  |
| $\begin{aligned} & \text { THROUGH } \\ & \text { Q25 } \end{aligned}$ | SAME AS Q3 |  |  |  |
| R1 | RESISTOR, FXD, COMPOSITION 2200 JHMS, 108 TOL, 1/2 watt | RC20GF222K | 81349 | 745-1366-000 |
| R2 | SAME AS R1 |  |  |  |
| R3 | RESISTOR, FXD, COMPOSITION 680 OHMS, 102 TOL, 1 WATT | RC32GF681K | 81349 | 745-3345-000 |
| R4 | $\begin{aligned} & \text { RESISTOR, FXD, FILM } \\ & \text { S } 36 \text { OHMS, } 18 \text { TOL, } 1 / 2 \text { HATT } \end{aligned}$ | RN6505360F | 81349 | 705-7083-000 |
| R5 | $\begin{aligned} & \text { RESISTOR, FXD, FILM } \\ & 1470 \text { OHMS, } 12 \text { TOL, } 1 / 2 \\ & \text { WATY } \end{aligned}$ | RN6501471F | 81349 | 705-7104-000 |
| R6 | RESISTOR, FXD, COMPOSITION 330 OHMS, $10 \%$ TOL, $1 / 2$ WATT | RC20GF331K | 81349 | 745-1331-000 |
| R7 | RESISTOR, FXD, COMPOSITION 220 OHMS, 108 TOL, $1 / 4$ hatt | RCOTGF221K | 81349 | 745-0725-000 |
| $\begin{aligned} & \text { RB } \\ & \text { THROUGH } \end{aligned}$ | SAME AS R 7 |  |  |  |
| R19 | RESISTOR, FXD, COMPOSITION 680 OHMS, $10 \%$ TOL, $1 / 4$ hatt | RC07GF681K | 81349 | 745-0743-000 |
| R20 | SAME AS R19 |  |  |  |
| R21 | SAME AS R19 |  |  |  |
| R22 | RESISTOR, FXD, COMPOSITION <br> 1K OHMS, $10 \%$ TOL, $1 / 4$ HATT | RCO7GF102K | 81349 | 745-0749-000 |
| R23 R24 | SAME AS R19 |  |  |  |
| R24 R25 | SAME AS R22 |  |  |  |
| R26 | RESISTOR, FXD, COMPOSITION 3900 JHMS, 108 TOL, $1 / 44$ HATT | RCO7GF392K | 81349 | 745-0770-000 |
| R27 | NOT USED |  |  |  |
| R28 | NOT USED |  |  |  |
| R29 | SAME AS R19 |  |  |  |
| R30 R31 | SAME AS R26 SAME AS R19 |  |  |  |




Figure 6-13. Backplane Board With Connector Assembly A10.


Figure 6-14. Optional Equipment.


ILLUSTRATION NOT AVAILABLE TO BE SUPPLIED AT LATER DATE

Figure 6-15. 782B-1 Self-Check Card.

| SYMBOL | DESCRIPTION | MANUFACTURER'S PART NUMBER | $\begin{aligned} & \text { MFR } \\ & \text { CODE } \end{aligned}$ | COLLINS <br> PART NUMBER |
| :---: | :---: | :---: | :---: | :---: |
| 782B-1 SELF-CHECK CARD |  |  |  | 777-1439-001 |
| $\begin{aligned} & \text { Al } \\ & \text { Si } \end{aligned}$ | INTEGRATED CIRCUIT <br> SWITCH, ROTARY <br> 2 SECTIONS, 4 POLES, <br> 5 PJSITIONS | $\begin{aligned} & \text { SL3979 } \\ & 237966 \mathrm{K2} \end{aligned}$ | $\begin{aligned} & 07263 \\ & 76854 \end{aligned}$ | $\begin{aligned} & 351-7121-030 \\ & 259-2204-000 \end{aligned}$ |
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| SYMBOL | DESCRIPTION | MANUFACTURER'S <br> PART NUMBER | MFR CODE | COLLINS <br> PART NUMBER |
| :---: | :---: | :---: | :---: | :---: |
| MAVUFACTURERS CODES |  |  |  |  |
| CODE | mANUFACTURER <br> SHELEY ASSOCIATES IN: el SEGUNDO, CALIFORNIA SPRAGUE ELECTRIC CD OF WISCOYSIN GRAFTJN, WISCONSIN ALLIED CONTROL CO, INC PLAVTSVILLE, CONNECTICUT MOTORJLA SEM ICONDUC TOR PRJDUCTS, INC PHDEVIX, ARIZONA FAIRCHILD CAMERA AND instrument corp, SEYICJNDUCTDR DIVISION MOUVTA IN VIEW, CALIFORNIA |  |  |  |
| 00303 |  |  |  |  |
| 01939 |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |
| 02288 |  |  |  |  |
| 04713 |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |
| 07263 |  |  |  |  |
|  |  |  |  |  |
| 07688 |  |  |  |  |
|  | JOINT ELECTRON DEVICE evgiveering council |  |  |  |
|  |  |  |  |  |
|  | U S TERMINALS INC CINCIVNATI, OHIO |  |  |  |
| 12615 |  |  |  |  |
| 13327 | SOLITROV DEVICES INC TAPPAY, NEW YORK |  |  |  |
|  |  |  |  |  |
| 17117 | ELECTROVIC MOULDING CORP PAWTUCKET, RHODE ISLAND |  |  |  |
|  |  |  |  |  |
| 37942 | P R MALLDRY AND CO, INC INDIAVAPOL IS, INDIANA |  |  |  |
| 56289 |  |  |  |  |
|  | SPRAGUE ELECTRIC CO NORTH ADAMS, MASSACHUSETTS |  |  |  |
| 70309 | NORTH ADAMS, MASSACHUSETTS <br> ALLIED CONTRDL CO, INE <br> NEW YJRK, NEH YORK |  |  |  |
|  |  |  |  |  |
| 71400 | bUSSMAN MFG DIVISION OF MC GRAH-EDISON CO |  |  |  |
|  | St LJUIS, MISSOURI |  |  |  |
| 72619 | OIAL IGHT CORPBROJKLYN, NEW YORK |  |  |  |
|  |  |  |  |  |
| 75382 | BROJKLYN, NEW YORK KULKA ELECTR IC CORP mt VERNON, NEh YORK |  |  |  |
|  |  |  |  |  |
| 76854 | MT VERNON, NEH YORKOAK YAVUFACTURING COCRYSTAL LAKE, ILLINOIS |  |  |  |
|  |  |  |  |  |
| 80058 | CRYSTAL LAKE, ILLINOISJOINT ELECTRONIC TYPEDESIGVATION SYSTEM |  |  |  |
|  |  |  |  |  |
| 81349 | DESIGVATION SYSTEM |  |  |  |
| 83003 | VARO INC <br> GARLAVD, TEXAS |  |  |  |
| 87930 | GARLAVD, TEXAS <br> TOWER MANUFACTURING CORP PROVIDENCE, RHODE ISLAND |  |  |  |
|  |  |  |  |  |
| 93332 | SYLVAVIA ELECTRIC PRODUCTS IVC, SEM ICONDUC TOR |  |  |  |
|  |  |  |  |  |
|  | WOBURV, MASSACHUSETTS COLL IVS RADIO CO DALLAS, TEXAS |  |  |  |
| 95104 |  |  |  |  |
|  |  |  |  |  |
| 95691 | ARROH-HART AND HEGEMAN <br> E. ECTR IC CO <br> los aneeles, california <br> military specifications |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |

## section <br> illustrations





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Figure 7-1. Functional Diagram (Sheet 6 of 6).



Figure 7-3. Logic 1 Card A1A2 Schematic.







Figure 7-9. Self-Check Card Schematic.


Figure 7-11. Preset 2 Card A1A6 Schematic.

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Figure 7-13. Preset 4 Card A1A6 Schematic.

COLLINS

