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Panasonic

Technical Guide

Digital Audio Tape Deck

SV-3500

Audio Division
Matsushita Electric Industrial Co. Ltd.

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1. General

2. Major Blocks and Operation

1. Function of the SV-3500

2. Major Blocks and Operation

1. General

1-1. Function of the SV-3500

The SV-3500 is a full-fledged DAT (Digital Audio Tape) recorder with coaxial and optical digital I/O terminals, for input and output in addition to the analog LINE IN/OUT terminals.

A 30 mmφ cylinder head is used for signal recording and playback. Use of a DC motor and a DD (direct drive) capstan motor for tape loading and mode switching and mounting of the mechanism in a stainless steel chassis, result in stable tape transport. The main features are listed below.

(1) Use of level meters with a large 26 digit display. Furthermore, the direct display system, from digital signal to digital data decoder to digital display, assures error free level displays.

(2) The digital signal input and output terminals for fiber optic cables and coaxial cables permit digital copying of tapes. (To another DAT recorder with digital input and output compatibility).
Furthermore, the SV-3500 is compatible with broadcast satellite modes A and B (Japan only) permitting digital recording of the digital music signals from a broadcast satellite tuner.

(3) Post-recording function
The post-recording function for subcode data permits program numbers to be rewritten and skip ID's to be written.

4) **Basic Operation**

Increased use IC's in the power supply circuit of the SV-3500 has reduced the size of the PC board area.

5) **Added Function**

The post-recording function for subcode data has been added to permit the SV-3500 to change the following data.

(1) Renumber:
Renumbers the programes.

(2) Start ID:
Move the position of the start ID which is entered at the starting position of a program and automatically erases the old start ID.

(4) Skip ID:
Recording a skip ID at the beginning and end of an undesired part of a recorded tape enables that part to be skipped during playback. (When a skip ID is detected the tape is fast forwarded, and when the next start ID is detected the tape is played back).

(4) Auto (absolute time):
Writes the absolute time onto a tape which has been recorded on a recorder not capable of writing the absolute time.

Also compatible with 32 KHz digital recording, the SV-3500 is capable of digital recording the broadcast satellite modes A and B. (The SV-3500 is compatible only with mode B at 48 KHz).

The music scan (introduction search) function plays only the first 9 seconds of each program. The "cleaning" indicator function has been added to inform the user when the head requires cleaning. (Lights when the error rate exceeds 1000). In this guide, each block in figure 2-1 is described.

2. Major Blocks and Their Operation

1) Cylinder (head)

A 30 mmø cylinder head which helically scans the DAT tape is used. The tape has a wrap angle of 90 degree with respect to the cylinder and the cylinder is fitted with two heads, A and B.

2) RF Circuit (chapter 3)

The signal reproduced by the cylinder has a considerably distorted waveform (compared to the digital signal) when recording to the tape. The RF circuit contains a waveshaping circuit which amplifies and waveshapes the signal so that the signal can be processed easily at the data slice circuit in the next stage.

3) Signal Processing Circuit (chapter 4)

This circuit produces the format of the signal recorded on the tape during recording and interleaves the data and adds error correcting codes. During playback, reading of the music signal, error correction, error interpolation, and reading of the subcode data are performed. This circuit also generates the clocks used in the SV-3500.

4) Audio Circuit (chapter 5)

This circuit includes the A/D and D/A converters and mainly handles the music signal.

5) Panel Control Circuit (chapter 6)

This circuit perform input processing of the control keys, control the FL display and exchanges control data with the system control circuit.

6) System Control Circuit (chapter 7)

This circuit, the heart of the mechanism operation control, receives various types of data from the panel control circuit, signal processing circuit and servo circuit, and controls the overall operation of the system.

7) Servo Board (chapter 8)

This circuit monitors and controls the operation of the mechanism.

8) Loading Mechanism (chapter 9)

This mechanism is driven by a single DC motor and loads and unloads the tape.

9) Power supply Circuit (chapter 10)

This circuit supplies the AC and DC power required by the various circuits in the SV-3500.

10) Mechanism Block (chapter 11)

This mechanism is same as SV-D1000 (Technics 1st generation DAT).

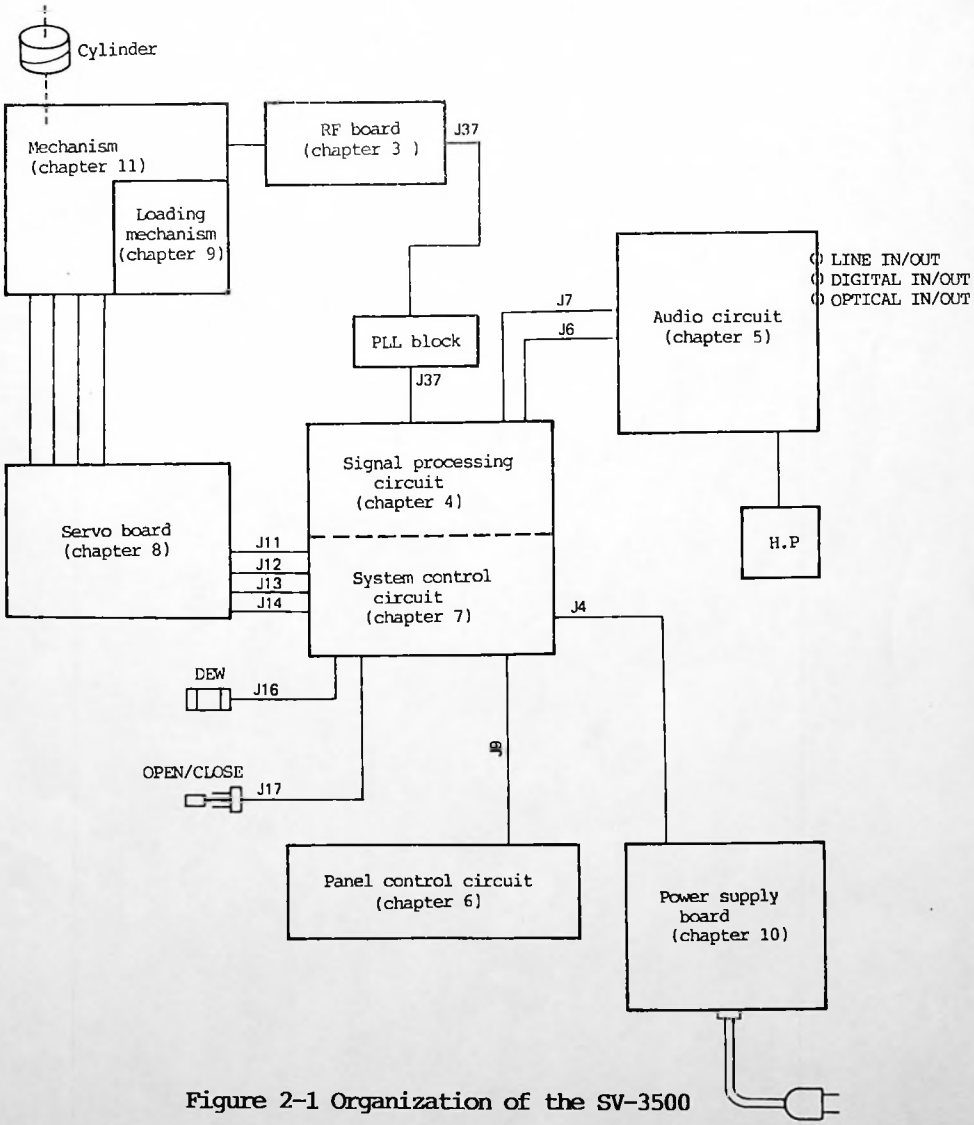


Figure 2-1 Organization of the SV-3500

3. RF Section

3-1. Block Diagram Description

3-2. Playback Circuit Operation

3-3. Recording Circuit Operation

3-1. Block Diagram Description

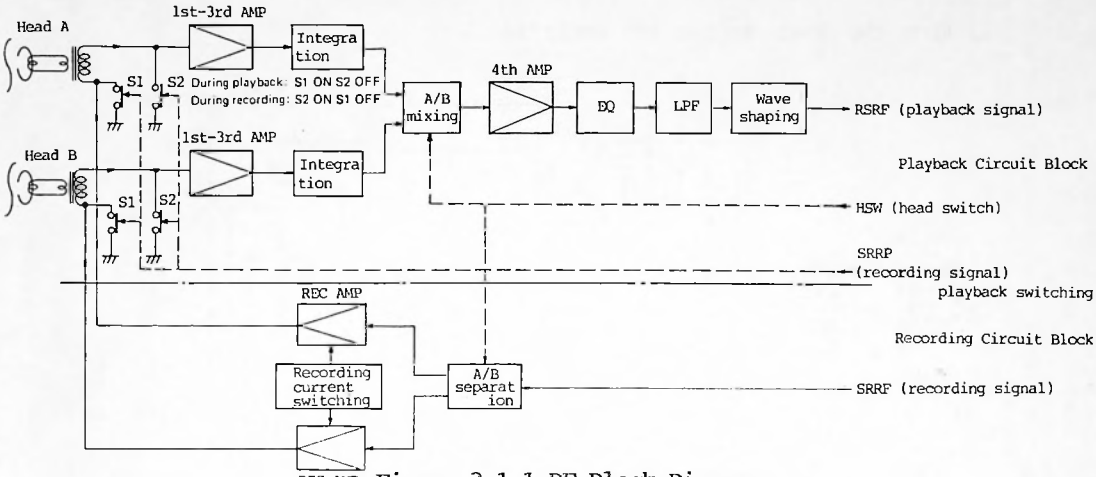


Figure 3-1-1 RF Block Diagram

1) Playback Circuit

(1) The RF signals picked up by head A and head B are sent through the rotary transformers to their respective three amplifiers and amplified by approximately 70 dB and then each signals is sent to the integrators.

(2) At the integrators, each signal is subjected to low frequency compensation and the result is sent to the A/B mixer. Based on HSW signal control, the A/B mixer converts the signals reproduced at head A and head B to a serial signal.

(3) The serial signal is amplified by approximately 20 dB at the 4th amplifier and sent to the equalizer for equalization.

(4) After the unwanted 8 MHz and above components are removed at the low-pass filter, the signal is sent to the waveshaping circuit. At the waveshaping circuit, the eye pattern of the equalized signal is waveshaped to a rectangular wave and then sent to the signal processing circuit as the RSRF signal (which is a digital data signal).

2) Recording Circuit

(1) The recording signal (SRRF) sent from the signal processing circuit is separated at the A/B separator, by HSW signal control, into RF signals for head A and head B.

(2) The separated signals are amplified at their respective amplifiers and sent to head A and head B. The recording current switching circuit is a gain switching circuit which changes the level of the PCM and ATF components of the RF signals for recording.

3-2. Playback Circuit Operation

1) From the Heads to the 4th Amplifier

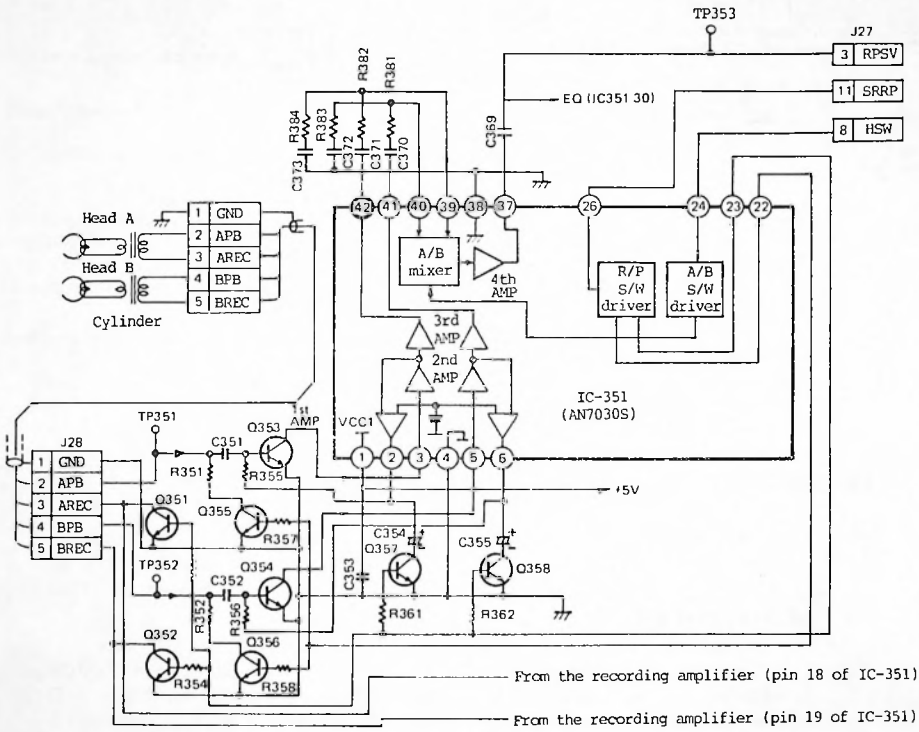


Figure 3-2-1 Playback Circuit Diagram

(1) When pin 11 of connector J27 goes low due to a command from the signal processing block, pin 26 of IC-351 goes low. Then, a high output appears at pin 23 of IC-531 and a low output appears at pin 22.

(2) Next, Q351 and Q352, which are connected to pin 23 of IC-351, turn on and this grounds the REC side of the heads. (At this time, Q355 and Q356 on the PB side are off). Thus, the RF signals picked up at the heads are sent to Q353 and Q354 (via the rotary transformers and pins 2 and 4 of connector J28). They are amplified and then sent to pins 3 and 5 of IC-531. Q357 and Q358 are provided to prevent C354 and C355 from discharging during recoeding.

(3) The RF signals input at pins 3 and 5 of IC-351 are amplified at the 2nd and 3rd amplifiers within the IC and output from pins 41 and 42. The output RF signals are subjected to low frequency compensation at the integrators, consisting of C370 through C373 and R381 through R384, and input to pins 39 and 40 of the IC-351.

(4) Based on HSW signal control at pin 8 of connector J27, The RF signals for head A and head B (which are input at pins 39 and 40) are mixed by the A/B mixer within the IC. The mixed signal is amplified by the 4th amplifier and output at pin 37 of IC-351. The RPSV signal from pin 37 passes C369 and is sent to pin 3 of connector J27 where it is used to operate the servo circuit in the servo block. The RF signals for head A and head B are mixed as shows in figure 3-2-2.

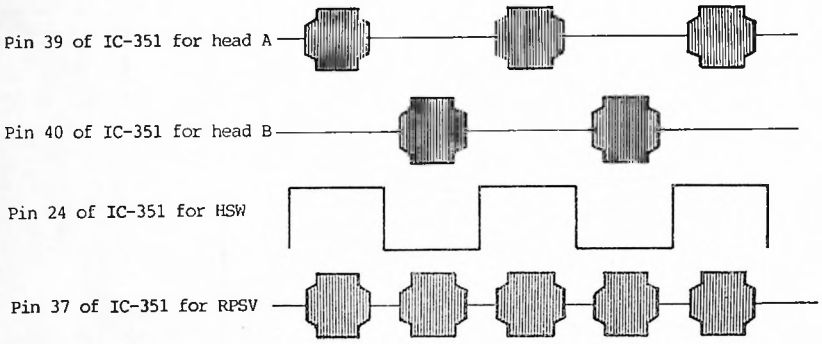


Figure 3-2-2

2) From the 4th Amplifier to the Equalizer Output (EQOUT)

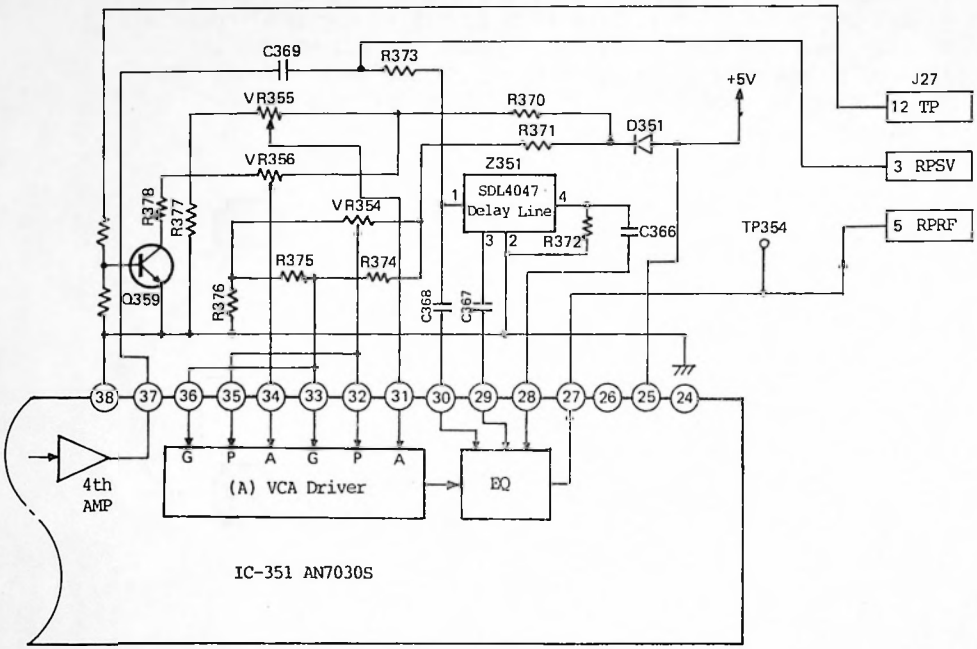


Figure 3-2-3

(1) The RF signal output from pin 37 of IC-351 is sent to pin 30 of IC-351 and pin 1 of Z351 (delay line). At Z351,signals, which are delayed by 100 nsec and 200 nsec, are output at pin 3 and 4, and sent to pin 29 and 28 of IC-351, respectively.

(a) Operation of the equalizer section and VCA (voltage control amplifier). The RF envelope signals input by pin 28, 29 and 30 of IC-351 are subjected to equalization by VR354 through VR356 (which are connected to the VCA drive circuit) as shows in figure 3-2-4.

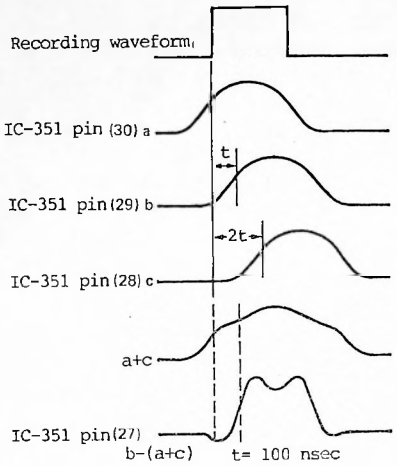


Figure 3-2-4

(b) Using CH.A as an example, VR356 varies the level of a+c to adjust the leading and trailing edges of the eye pattern waveform which is output from pin 27. VR354 adjusts the balance of the eye pattern by varying the level ratio of a and c.

VR355 varies the a+c level for CH.B, and together with VR354, adjusts the balance of the eye pattern waveform.

3) From the Low-Pass Filter (LPF) to the Signal Processing Circuit

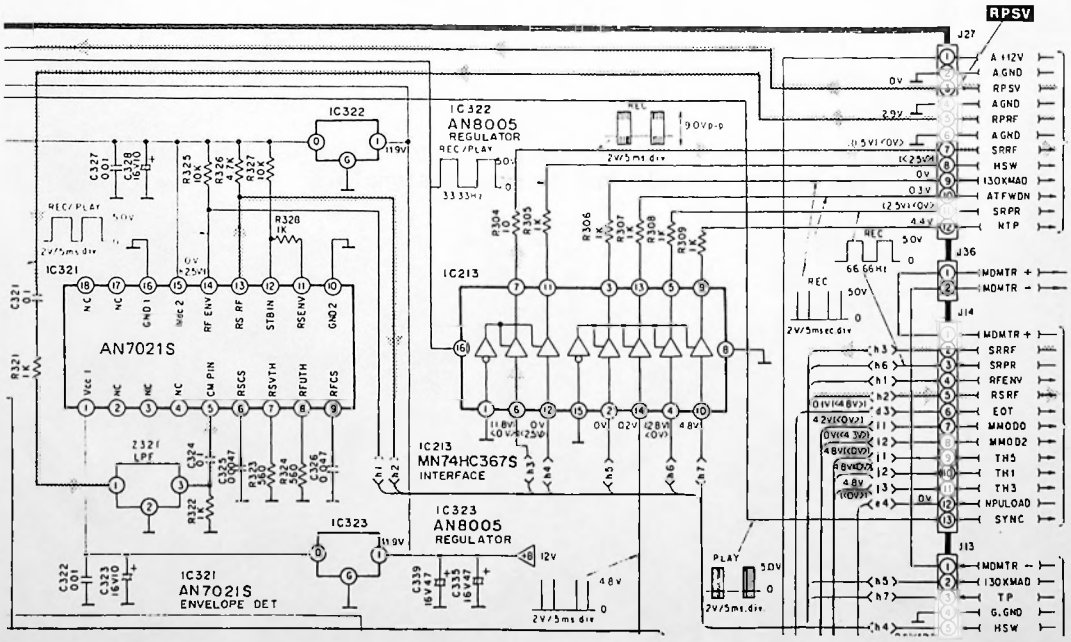


Figure 3-2-5

(1) The RF signal sent from pin 5 of J27 in the RF block is input by the Z321 LPF where unwanted components of 8 MHz and above are removed, and then input by pin 5 of IC-321.

(2) The RF signal input by pin 5 of IC-321 is waveshaped by a comparator, output from pin 13, and sent to the signal processing circuit through pin 5 of connector J14. At this time, the RF signal is out put to pin 14 only when pin 11 of IC-321 is high. This is done to prevent noise from being output when there is no signal. This operation is shows in figure 3-2-6.

(3) At the same time, the RF envelope signal, which is output from pin 14 of IC-321, is generated as it is used in the signal processing circuit to search for the beginning and end of tape. Its timing chart is shows in figure 3-2-7.

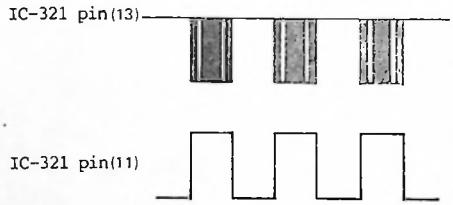


Figure 3-2-6

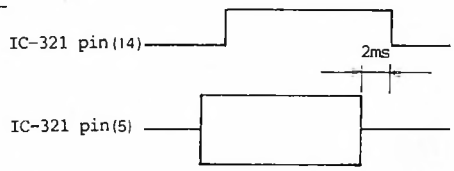


Figure 3-2-7

(4) The logic circuit consisting of IC-213 is used to buffer the timing signals and recording signals.

3-3. Recording Circuit Operation

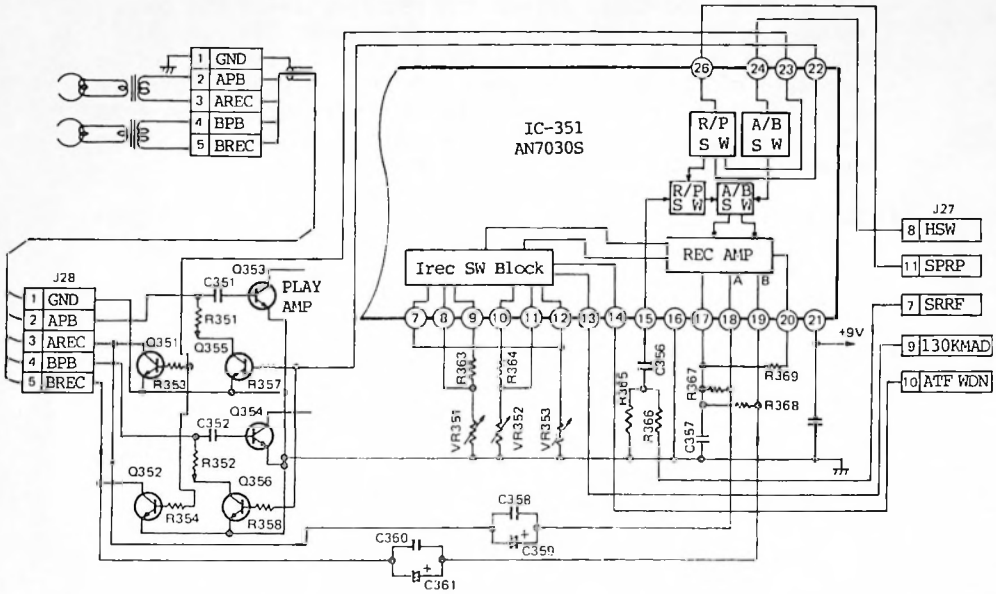


Figure 3-3-1 Recording Circuit Diagram

1) Recording Signal Flow

(1) The recording signal (SRRF signal) from the signal processing circuit is sent to pin 15 of IC-351 through pin 7 of connector J27.

(2) The recording signal input by pin 15 of IC-351 is sent to the A/B switch (A and B head switch) through the R/P HSW signal control, which is input by pin 8 of connector J27, the decision to send the input recording signal to head A or head B is made at the A/B switch. The signal is amplified at the REC amplifier and output from pin 18 of IC-351 for head A and from pin 19 for head B. The timing is shows in figure 3-3-2.

(3) The recording signals output from pins 18 and 19 of IC-351 are sent to pins 3 and 5 of connector J28 through C358, C359, C360 and C361. Since the recorder is in the record mode at this time, pin 11 of connector J27 is high. Thus,pin 26 of IC-351 is high and pin 22 is high (the opposite of the playback mode). This high signal turns on Q355 and Q356, through which the recording signal currents flow after passing through the rotary transformers. This means that current flows through heads A and B.

(4) Since pin 23 of IC-351 is low at this time, Q351 and Q352 are off.

2) I rec Switching Block within IC-351

This circuit varies the levels of the PCM signal and ATF signal found in the recording signal..

(1) The levels of the PCM signal and ATF signal in the recording signal are varied with VR351 through VR353 based on the timings of the 130 KMAD signal input by pin 13 of IC-351 and the ATFWDN signal input by pin 14. This is shows in figure 3-3-3.

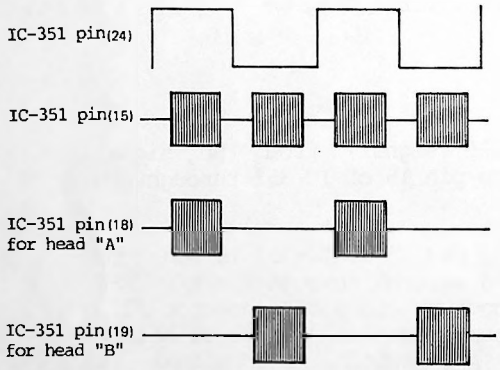


Figure 3-3-2

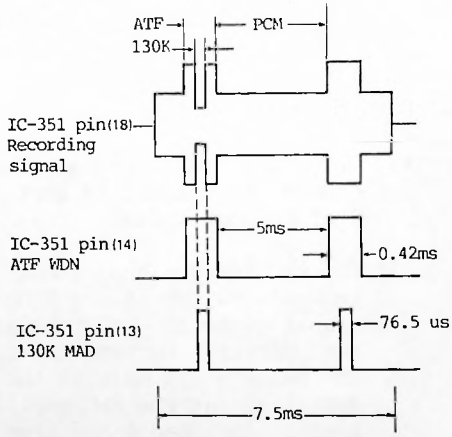


Figure 3-3-3

4. Signal Processing Circuit

4-1. Recording Data Format on Tape

1) Subcode Area

2) PCM Area

3) ATF Area

4-2. Signal Processing Circuit Operation

4-3. Reference Clock Generation

1) Playback PLL Circuit Operation

2) DF PLL Circuit Operation

3) Master Clock PLL Circuit Operation

4) DIN PLL

5) Clocks Generation by the Signal Processing Circuit

4-4. Subcode RAM

4-5. Level Meter Signal

4-6. Switching of Signal Flow

4. Signal Processing Circuit

4-1.Recording Data Format on Tape

The recording format of subcode data for the SV-3500 is shows in figure 4-1-1. The SV-3500 contains a post-recording function for subcode data. The post-recording function permits the following to be performed:

(1) Renumbering

Edits tape containing programs which have already been numbered (e.g. with the auto program numbering function). Also includes the auto renumbering function which automatically renumbers the entire tape for all programs after the point where a change was made.

(2) Writing the SKIP ID

The SKIP function undesirable sections (parts the user does not wish to listen to) of a tape, for example broadcast recording. While the tape is played back, the post-recording function is used to write the SKIP ID to any part that the user would like to SKIP. Once this has been done, the tape fast forwards during subsequent playback operations whenever the SKIP ID is detected and playback automatically resumes when the start ID is detected.

(3) Auto absolute time

Permits tapes (recorded on DAT sets which do not record the absolute time) to be automatically recorded with the absolute time. Once the absolute time is recorded onto the tape with this function, the repeat function.(e.g. between points A and B) can be used.

The post-recording function rewites only the subcodes during the playback mode under ATF control.

The figure below shows the recording format for one track on the DAT tape.

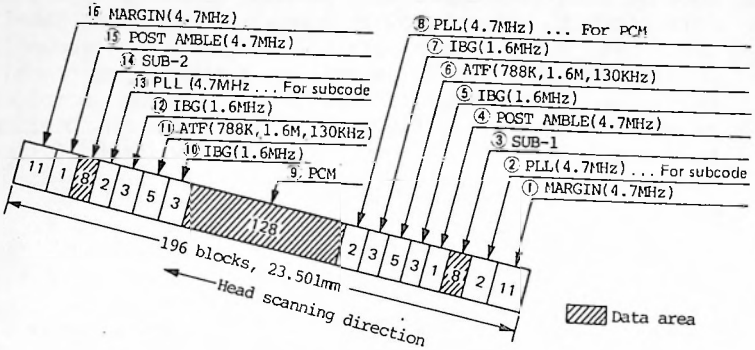


Figure 4-1-1

Each of data items shows above contain the signals shows in table 4-1.

		SIGNAL	ANGLE(deg)	Number of block	PERIOD(us)
(1)	MARGIN	1/2 f ch	5.051	11	420.9
(2)	PLL (SUB)	1/2 f ch	0.918	2	76.5
(3)	SUB-1		3.673	8	306.1
(4)	POST AMBLE	1/2 f ch	0.459	1	38.3
(5)	IBG	1/6 f ch	1.378	3	114.8
(6)	ATF		2.296	5	191.3
(7)	IBG	1/6 f ch	1.378	3	114.8
(8)	PLL (PCM)	1/2 f ch	0.918	2	76.5
(9)	PCM		58.776	128	4898.0
(10)	IBG	1/6 f ch	1.378	3	114.8
(11)	ATF		2.296	5	191.3
(12)	IBG	1/6 f ch	1.378	3	114.8
(13)	PLL (SUB)	1/2 f ch	0.918	2	76.5
(14)	SUB-2		3.673	8	306.1
(15)	POST AMBLE	1/2 f ch	0.459	1	38.3
(16)	MARGIN	1/2 f ch	5.051	11	420.9
	TOTAL		90	196	7500

Recording density ..... 61.0 KBPI
f ch 9.408MHz

*Calculated under the condition that 30 o - 90 deg wrap angle, 2000 rpm cylinder is used.

Table 4-1

1) Subcode Area

Figure 4-1-2 shows the data format of the subcode area which contains the data area (256 bits) called the "PACK" area. The subcode data is located in this pack area. In one track, the data format shows below is repeated 8 times in Sub-1 and 8 times in Sub-2 for a total of 16 times. A group of data consisting of 2 blocks is written 8 times (per track) and in one frame (two tracks) is written 16 times to complete a set of subcode data (see figure 4-1-3). For each rotation of the head cylinder, one group of data is written 16 times (2 blocks x 8 times) for two tracks.

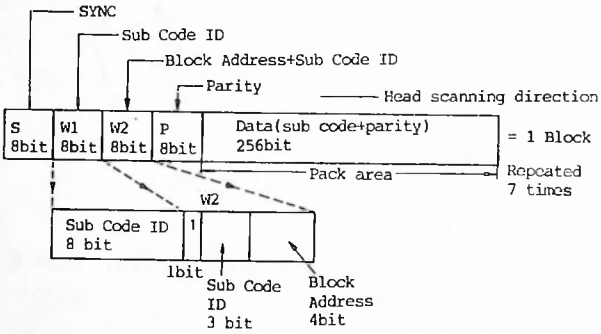


Figure 4-1-2

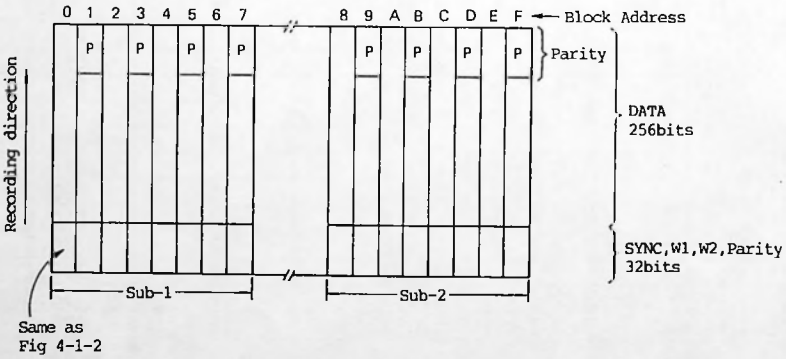


Figure 4-1-3

The contents of W1 and W2 are shows in the figure 4-1-4.

W1		W2			
Sub-Code ID			Sub-Code ID	Block Address	
Control ID	DATA ID	1	Format ID	X X X 0	← Even tracks
PNO ID (2)	PNO ID (3)	1	PNO ID (1)	1	← Odd tracks
MSB	LSB	MSB		LSB	

Figure 4-1-4

The contents of the control ID above are shows in the figure 4-1-5.

Control ID (DATA ID = 0000)

3	2	1	0

TOC-ID	1	This program is entered in the TOC
	0	This program is not entered in the TOC
Shortenning ID	1	The beginning of shortening play, 33 3 frames (the end of ghortening play is S-ID=1)
	0	Not the beginning of shortening play
Strat-ID (S-ID)	1	The start of a program, recorded 300 30 frames continuously
	0	Middle of program
Priority-ID	1	PNO-ID is recorded and is well defined program number where priority-ID=1
	0	PNO-ID is not recorded or is ambiguous

Figure 4-1-5

The contents of the data area for subcode data are shows in the figure 4-1-6.

Item	Mode	Contents
0000	No information	PC1 - PC8 all are "0"
0001	Program time	PNO,Index and continuous time code within program
0010	Absolute time	PNO,Index and continuous time code on a tape
0011	Running time	PNO,Index and continuous time code within one recording
0100	TOC	The table of contents
0101	Calender	Year,Month,Day, The day of the week hour,Minute,Second
0110	Catalog	The catalog number of the cassette
0111	ISRC	The international-standard-recording code
1000	Reserved	
1001	Reserved	
1010	Reserved	
1011	Reserved	
1100	Reserved	
1101	Reserved	
1110	Reserved	
1111	Reserved	Defined by the pre-recorded tape

Figure 4-1-6

The item code is located at the beginning of the subcode data area and identifies the block.

2) PCM Area

The data in the PCM area consists of the items shows in the figure 4-1-7. The data area contains the music data and the C1 and C2 error-correcting codes. The data shows in the figure below is found 128 times in one track. However, unlike the subcode data in which the same data is repeated, the track contains interleaved music data which is arranged in sequence. PCM-ID (W1) in the PCM area contains the PCM area format shows in figure 4-1-9.

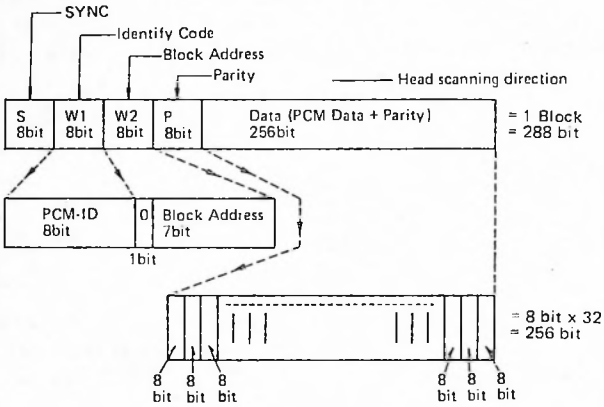


Figure 4-1-7

The figure below shows the organization of the data in the W1 and W2 area of figure 4-1-7. The following can be placed in the optional code areas.

(1) Program number
(2) Index
(3) Start flag
(4) Absolute time
(5) Program time
(6) Catalog number

W1 (PCM-ID)			W2 (Block Address)
ID-1	ID-2	Frame Address	0, X X X X 0 0 0
Optional Code			0, ↑ 0 0 1
ID-3	ID-4	Frame Address	0, ↑ 0 1 0
Optional Code			0, ↑ 0 1 1
ID-5	ID-6	Frame Address	0, ↑ 1 0 0
Optional Code			0, ↑ 1 0 1
ID-7	ID-8	Frame Address	0, ↑ 1 1 0
Optional Code			0, ↑ 1 1 1
MSB		LSB	MSB LSB

Figure 4-1-8

The ID-1 is format ID.
The ID-1 - ID-7 and the frame address must be recorded.
When no ID-8 is used, these codes are logical zero "0".
When no optional code is used, these code are logical zero "0".

The contents and meanings of ID-1 - ID-8 are given in figure 4-1-9.

ID-1 (format)	ID-2 ~ ID3	Connection
0 0 (Audio use)	ID-2 (Emphasis)	00: off 01: Pre-Emp 10, 11: Reserved (for orther Pre Emph)
	ID-3 (Sampling freq.)	00: 48 kHz 44.1 kHz 10: 32 kHz 11: reserved
	ID-4 (No. of CH)	00: 2 CH 01: 4 CH 10, 11: reserved
	ID-5 (Quantization)	00: 16bits linear 01: 12 bits non-liner 10.11: reserved
	ID-6 (Track pitch)	00: 13.6μm 01: 20.4μm 10: 11: reserved
	ID-7 (Copy inhibit)	00: Digital copy permitted 01: reserved 10: Digital copy prohibited 11: reserved
	ID-8	32 ID-8's constitute PACK.

Figure 4-1-9

3) ATF Area

The track positions (sequence) in the ATF area are organized as shows in the figure 4-1-10.

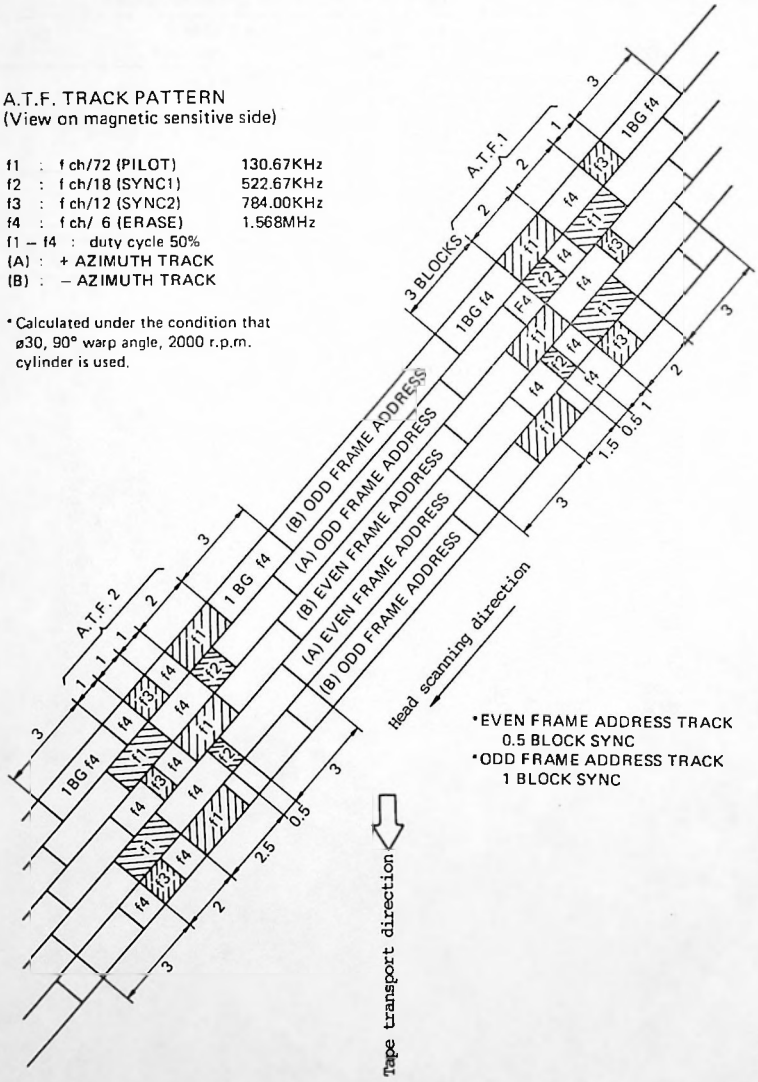


Figure 4-1-10

4-2. Signal Processing Circuit Operation

The operation of the signal processing circuit can be roughly divided into the following.

(1) Clock Generation

It is necessary for the various circuits in the SV-3500 (e.g. servo circuit, system control circuit, etc) to operate synchronously. Various types of clock pulese, which become the operating reference for the various circuits, are generated by the signal processing circuit and sent to the various circuits.

(2) Demodulation of the Playback Signal and Error Correction

The signals recorded on the DAT contains subcode data and error correction codes in addition to the music signal. These various types of information are read by the signal processing circuit, with the subcode data sent to the subcode processor and the music signal sent to the analog circuit where it is restored to an analog signal by the D/A converter.

The DAT system employs the dual Reed-Solomon error correction scheme which detects and corrects errors contained in the reproduced data. Error correction is performed in the following sequence.

C1 Correction → C2 Correction → (interpolation)* → Output
* Executed only when correction is impossible.

The cylinder in the SV-3500 is fitted with two opposing heads. Error correction enables playback to be performed even if one head becomes damaged. The SV-3500 contains a function for servicing which displays the error rate (error rate = x/10,000 frames). It is helpful in adjusting the RF circuit or determining whether the mechanism is faulty. If one head becomes dameged, the error rate becomes a minimum of 5000 (since half of the data is missing).

Checking the Error Rate

(a) Load the standard tape for rate measurement and set the TIMER switch to PLAY.

(b) While holding down the RECALL button, turn on the power switch and wait 5 seconds.

(c) Press the PLAY button to play back the tape.

Once the steps above have been performed, the error is displayed whenever the RECALL button is held down. This function can be cancelled by turning off the power switch.

(3) Data Format Generation During Recording

There are many types of data recorded onto the tape such as music signal data in the PCM area, subcode data, error correcting codes C1 and C2 etc. The operation to convert the data sent from the subcode CPU and A/D converter into the DAT format and then to send it to the RF circuit are performed by the signal processing circuit.

(4) Muting Command Generation

A muting command is issued to prevent the output of click noise which is generated at the moment when the operating mode of the DAT set is switched (e.g. STOP to PLAY, REC to PAUSE, etc). Control of the signal flow during playback and recording is also performed by the signal processing circuit.

(5) Digital I/O

The SV-3500 is equipped with digital I/O terminals for use with coaxial cables or fiber optic cables. These permit digital signal transfers using a standard interface format (Biø modulation, data rate 48 KHz x 2 ch x 32).

The digital I/O terminals are directly connected to the signal processing circuit. Modulation and demodulation of the standard format are performed by the signal processing circuit. The fiber optic I/O connectors use EIJA compatible connectors.

These functions are executed the SBR, DSP, DEM, ECC, and IFGA IC's in the signal processing circuit, peripheral PLL circuit, RAM, etc (see figure 4-3). The functions of the major IC's are described next.

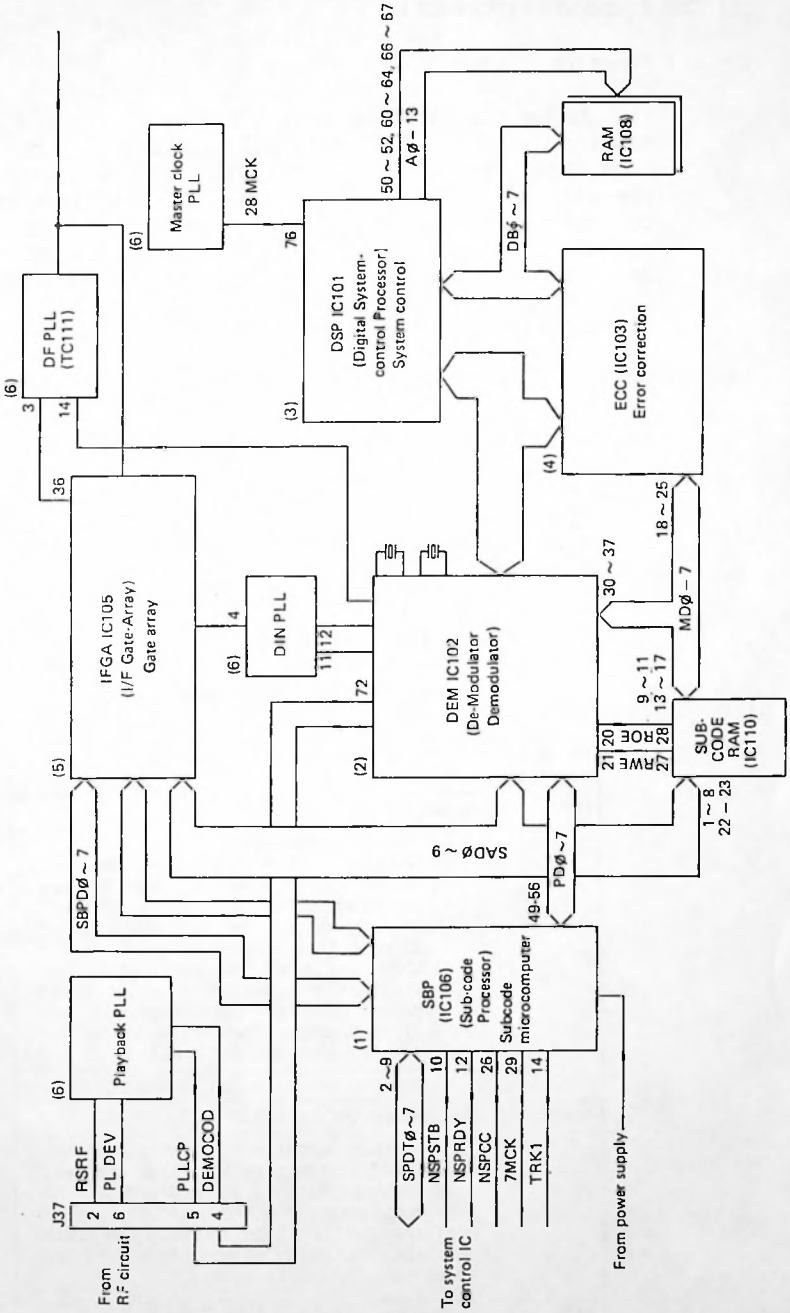


Figure 4-3 Block Diagram of the Signal Processing Circuit

1) SBP (Subcode Processor)

(1) Function

The major functions of this LSI chip during playback are sending the subcode data and pack data which have been separated from the playback signal to the system control circuit and transferring the control data from the system control circuit to the signal processing circuit. During recording, the SBP chip receives subcode data and pack data from the system control circuit and adds parity. The SBP chip also performs mode switching control for the overall signal processing operations.

(2) Signal Processing and Description

(a) Playback

Data Processed	Description
Frame address	Sampling of the frame address
	A/B track comparison values for track A and track B are compared. If they match, they are considered correct. If not, 1 is added to the former value.
	Muting and interpolation processing based on the frame address.
Block address	Sampling of the block address
PCMID	Sampling of the PCMID
	A/B track comparison. 1) When both track are valid, The last value of tracks A and B are compared. If they match, they are updated. If not, they are not updated. 2) When one track is not good. The PCMID at the beginning and the end of the good track are compared. If they match, they are updated. If not, they are not updated.
	Muting processing based on the PCMID
SUBID	Sampling of the SUBID
	A/B track comparison, Both tracks are compared if their parity flags are set. If they match, they are updated. If not, they are not updated. If the parity flags of only one track is set, the value of the track with the set parity flag is used.
PACK	Pack parity check
PLL frequency	Detection of the PLL frequency
	Correction of the PLL frequency. (A/B tracks)
Error rate output	C1 error rate is output every 39 frames.(BCD)

(b) Search

Data processed	Description
SUBID	Sampling of the SUBID
PACK	PACK parity check
PLL frequency	Detection of the PLL frequency
	Correction of the PLL frequency (A/B tracks)

(c) Recording

Data processed	Description
W1, W2	W1 and W2 generation in the PCM area
	W1 and W2 generation in the SUB area
	W1 and W2 parity generation
PACK	PACK parity generation

2) DEM (Demodulator)

(1) Function

The major functions of this LSI chip are demodulating the PCM signal from the playback signal and recording/playback of the subcode.

(a) Decoding of the playback signal (10-8 conversion, synchronization detection, ID parity check).

(b) Recording of the subcobe (ID code, recording of PACK, interface with SBP).

(c) DIO circuit (IEC format, Fs= 48KHz/32KHz) (44.1 KHz is for the CD format and thus can't be received).

(d) Generation of subcode C1 parity.

(e) C1 error rate (every 39 frames) counting.

(f) Digital part of the PLL for DIO is built-in.

(2) Built-in Functions

(a) Demodulation and ID Playback

I) Synchronization Detection
Detects the synchronization signal from the clock and playback signal from the playback PLL, and generates a clock for demodulation.

Synchronization protection
*During playback = 2 blocks
*During search = 1 block

II) 10-8 Conversion
Converts the playback signal from 10 bit units to 8 bits data.

III) ID Parity Check
Checks the parity of the ID code (W1, W2) of each block. Based on the ID code, the data and clock required to write playback data to the main memory are output. Also, the subcode PACK data is output to the subcode RAM, the SUBID is output to the parallel/ serial converter and the PCMID is output to the playback PCMID data register.

IV) SUBID Parallel/Srial Conversion
Converts the reproduced SUBID (parallel) to a serial data and outputs it from the data line (SIDDA) according to the clock (SIDSH) from the SBP. For the SUBID's the last correct value in each of the odd/even blocks is output. Whether the value is correct is determined from the validity flag at the SBP. (see the SBP function and SUBID) for the SID, the total number of SID's of one track is sent.

V) Playback PCMID Register
Latches ID1 - ID7 and frame addresses of the PCMID and outputs them serislly from the data line (MID-D) according to the shift clock (MID-S) from the SBP. For the frame addresses, majority processing is performed for each of the A and B tracks. (If the majority is no good, the previous value is held).

VI) Error Rate Counter
Counts the C1 flag from the ECC during playback and serially outputs the counted value every 39 frames from MID-D.

(b) ID Recording and Pack C1 Addition

I) SUBID Serial/Parallel Conversion
Converts the SUBID, which is sent from the SBP through the data line (SID-DA) during recording, to an 8 bits parallel data, adds the block address and parity and then outputs it.

II) C1 Addition (address counter for C1 calculation)
Adds the C1 parity for PACK during recording. The C1 parity is generated by ECC and sent through the data bus (IDB0 - IDB7). The address used when writing C1 to the subcode RAM and various control signals are generated for syndrome processing which is used in C1 generation.

III) Subcode MPX
Output the subcode data (SUBID, PACK) during recording through the data bus (SD0 - SD7) according to the shift clock (SUBOE) from the DSP.

(c) Subcode RAM Related

I) Recording/Playback Data Control
During recording, reads the data to be recorded from the subcode RAM output it to the MPX. During playback, generates the address and control signal which are used to write the reproduced data to the subcode RAM.

II) Subcode RAM Control (MPX)
Controls access to the subcode RAM. It uses the priority circuit to adjust the order of the RAM read and write requests from the various sections so that they do not overlap.

(d) SBP Interface and System Controller

I) PACK data Interface with the SBP
The pack data is written to the subcode RAM. During recording, the pack data is sent from the SBP to the subcode RAM, added to C1 and transferred to the DSP. During playback, it is sent from the demodulator to the subcode RAM and transferred to the SBP. The pack data is written to and read from RAM through the data bus (PD0 - PD7). The RAM address at this time is incremented by a request signal from the SBP.

II) System Controller
The system control signals (play/rec, post-recording, search, analog/digital, block shift correction, frame address) from the SBP are latched and various types of mode switching signals are generated.

(e) Digital I/O

I) DIO Control
Generates the DIO system clock. For DIN, the clock is generated with the timing of the detected synchronization signal. Here, the various clocks (DSIFT, DLOAD, LR) for the A/D and D/A converters and DF (digital filter) are generated.

II) Modulator
The DA data is output the DIO format after being added with the synchronization signal and various control signals, and BIO modulated. The category code is only in the 2-ch general format. (for 48/ 44.1/ 32 KHz).

III) Demodulator
During DIN, after the input signal has been BIO demodulated, the synchronization is detected and the parity is checked. Then, the 16 bits AD data is output from the CDCP terminal to the DSP. The phase comparator output which creates the VCO control voltage used for clock sampling in BIO demodulation is built in.

(f) Master Clock

I) MPX
The FS switching signal of the system controller switches the input of the crystal or VCO for the various DIN frequencies of 48 / 44.1 / 32 KHz, and output the master clock which is 128 times FS. (This signal is divided by 128 in the DIO control section and becomes the reference for the LR system).

3) DSP

(1) The major functions of the DSP are control the external RAM and conversion of the PCM signal to the DAT format during recording.

(a) Generation of the system control clock (control clock for symbol, block and frame).

(b) Recording signal generation (8 - 10 conversion, synchronization signal, addition of ID, ATF signal generation).

(c) Main RAM external address control (interleave, deinterleave, parity generation, address generation for error correction).

(d) Interpolation when error correction is not possible.

(2) Built-in Function

(a) Clocks

I) System Clock Generation
Divides the 28.224 MHz clock and generates the various clocks (main RAM control signal, ATF switching signal, drum synchronization signal TSCK 33.3 Hz).

II) Fs Division
Generates the various clocks (main RAM control signal, ATF switching signal, drum synchronization signal (TSCK 33.3 Hz) by dividing the 28.224 MHz clock.

(b) Recording

I) ATF Signal Generation
Generates the various ATF clocks to be placed on the recording signal.

II) PCM ID Generation
Adds the block address, frame address and parity to the PCMID which is sent from the DEM to terminal DIRQT based on the shift clock DCP.

III) Subcode Data Latch
Latches the subcode data (SUBID, PACK) which is input via the data bus (SD0 - SD7) from the DEM according to the SUBOE during recording.

IV) 8 - 10 Conversion
Converts the recording data, 8 bits at a time, to 10 bits. Also adds the synchronization signal.

V) Recording Signal MPX
Switches the converted (8 - 10) PCM signal which comprises the recording signal and the ATF signal according to the system clock. Also outputs the head amplifier switching signal (HEACH) during REC-PLAY and post-recording to must the recording signal.

(c) ECC Related

I) Address Counter for C1 and C2 Calculation
Generates the address for the main RAM to perform error correction based on C1 and C2 during playback and on C1 and C2 calculation during recording. Output the address for syndrome calculation and the address for the RAM read/write operation from the ECC to address bus A0 - A13, based on the control signal from ECC. Also output the synchrome latch clock SLACH for syndrome calculation, shift clock SSHIF, C1 and C2 switching signal RQKIR, ECC reset signal, etc.

II) ECC Buffer (latch)
The C1 and C2 parity from the ECC during recording and the error correcting data and flag data from the ECC during playback are input via the data bus (IDB0 - IDB7) and output through the latch to the data bus (DB0 - DB7).

(d) Main RAM Related

I) Address Counter for A/D and D/A data
Outputs, to the address bus, the address for writing the A/D data to the main RAM during recording and the address for reading the D/A data from the main RAM during playback.

II) Address Counter for Recording/ Playback Data
Generates the address for reading recording data from the main RAM and the address for writing playback data to the main RAM.

III) Buffer (latch) for Playback Data
Output the playback data DEMDAT to the data bus (DB0 - DB7).

(e) A/D and D/A Related

I) Output 16 bits data for D/A by reading the D/A data in two steps from the data bus (DB0 - DB7), 8 bits at a time, during playback. Also outputs the 16 bits A/D data in two steps, 8 bits at a time, to the data bus (DB0 - DB7).

II) Interpolation Circuit
Performs mean value interpolation on words which can't be corrected for A/D data for DIN in which a parity error occurred with a set error flag (DFAG) during recording or for D/A data read from the main RAM during playback.

4) ECC

Function

The ECC generates C1 (4 parity bits) and C2 (6 parity bits) during recording and performs C1 and C2 correction during playback according to the DAT error correction scheme (Reed-Solomon code).

(1) 8 bits Galois processing
(2) Parity generation based on Reed-Solomon codes
(3) Duplex error correction for C1 and C2
(4) 6 level erasure correction in C2 using the C1 flag
(5) Six built-in syndrome generators

4-3. Reference Clock Generation

1) Playback PLL Circuit

(1) Playback PLL Circuit

The timing chart for the playback PLL circuit is shows in figure 4-4. The circuit is shows in figure 4-5. In this circuit, IC-171 is the delay line IC and provides 50 ns and 80 ns delays in output 01 and 02, respectively, for the input signal I. IC-174 is an analog switch which transfers the voltage at pin 11 to pin 10 only when pin 12 is high.

The RC filter that follows IC-174 is an integrator. It produces a DC voltage, proportional to the width of the pulse output from pin 10 of IC-174, and serves as a control voltage for the oscillation frequency of the VCO IC-177.

IC-176 is a buffer amplifier.
IC-177 is a VCO for the center frequency of 9.408 MHz which is double RSRF (= 4.704 MHz).
The playback PLL performs the following functions to:

(a) Reads the data from the cylinder head during playback and restores it to the original data.

(b) Generates the clock signal (PLLCP) required to decode this data. Figure 4-4 is described next.

Original data. To represent this data during recording, a change from high to low corresponds to "1" data, and the previous state being held (high or low) is "0" data.

(1) Data (RSRF) read directly from the head is sent from the RF circuit. This signal is influenced by the mechanical vibrations of the mechanism during recording and playback and shifts to the left and right. The playback PLL circuit is provided to convert this signal into data correctly.

(2),(3) Output from IC-171. They are delayed by 30 ns and 80 ns with respect to the input signal ((1) above). These delay times, within a half cycle (1/4.7 MHz x 1/2 = 106 ns) of RSRF, are set to obtain the clock pulse (see figure 4-4 (6)) which is used to read the data. (The leading edge of (6) is at the middle of (1)).

(4) The result of the EX-OR of (2) and (3), it is high only when (2) and (3) do not match.

(5) Inverted polarity of signal (1).

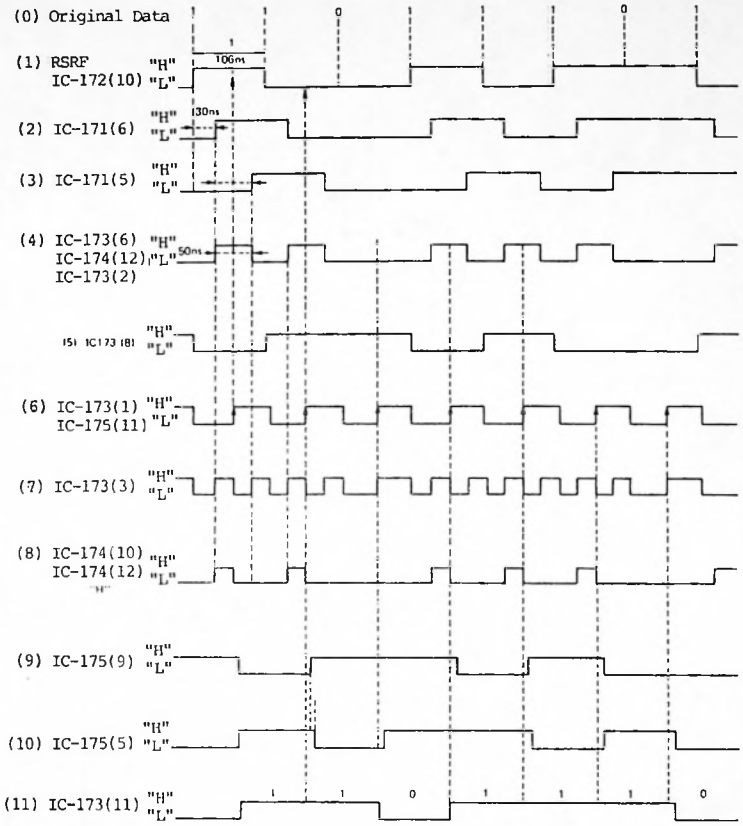


Figure 4-4 Playback PLL

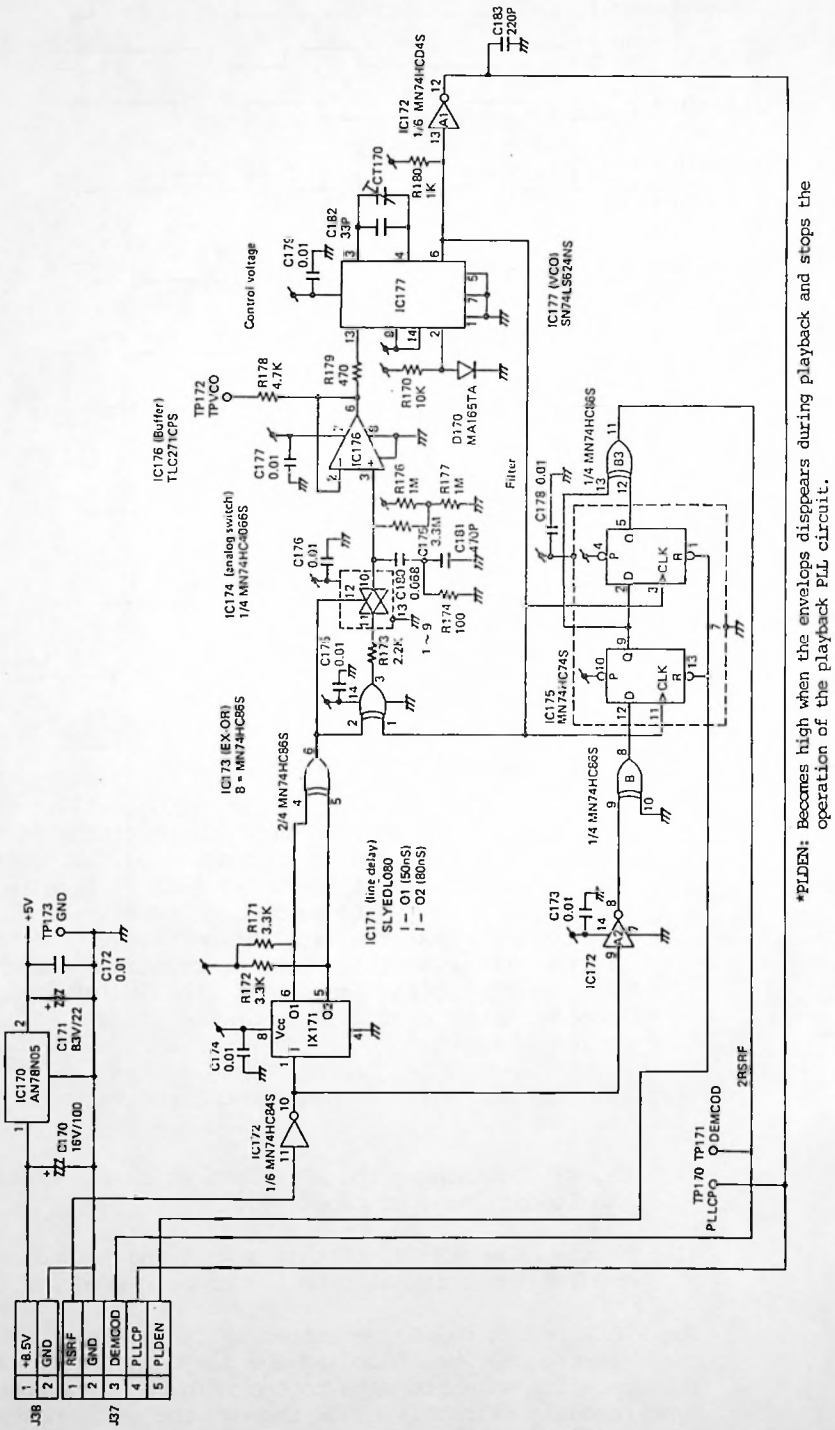
(6) Output clock pulse of the VCO IC-177 which determines the data read timing. The timing of this clock's leading edge is controlled by the control voltage at pin 13 of IC-177 so that it lies in the middle of the half period of RSRF. The PLL functions so that the oscillation frequency (phase) of the VCO is shifted when the relative phase of this clock shifts from RSRF, this maintains the leading edge of the clock in the middle of one period of RSRF.

(7),(8) Outputs which become the control voltages for the VCO.

(9) Signal containing the RSRF data which was read at the leading edge of clock (6).

(10) Taking the EX-OR of this signal and signal (9) enables the original data (0) to be reproduced.

The PLLCP (clock pulse) generated by the playback PLL is used in the DEM when decoding the playback data. Also the operation to write data to the main RAM is performed synchronously with this clock through the DSP. However, the reading of data from the main RAM and subsequent operations are performed using the system clock and are not synchronized with the PLLCP.



*PLDEN: Becomes high when the envelops disppears during playback and stops the operation of the playback PLL circuit.

Figure 4-5 Playback PLL Circuit

(2) Playback PLL Operation Command Circuit

This circuit is used to prevent the operation of the playback PLL circuit whenever the head is not in contact with the tape (e.g. STOP or PAUSE mode), as noise mayby generated.

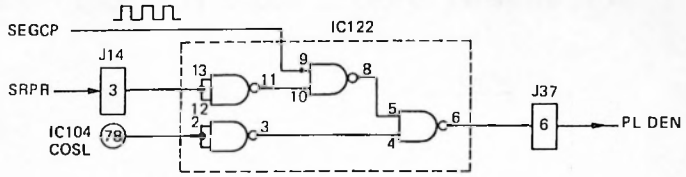


Figure 4-6

(a) Pin 9 of IC-122 is the input for SEGCP, which is 15 ms rectangular waveform signal from the signal processing circuit.

(b) Pins 12 and 13 of IC-122 are the input for SRPR (pin 3 of J14) from the signal processing circuit.

(c) COSL is input from pin 78 of the digital servo circuit IC-104.

(d) The operations are shows in figure 4-7.

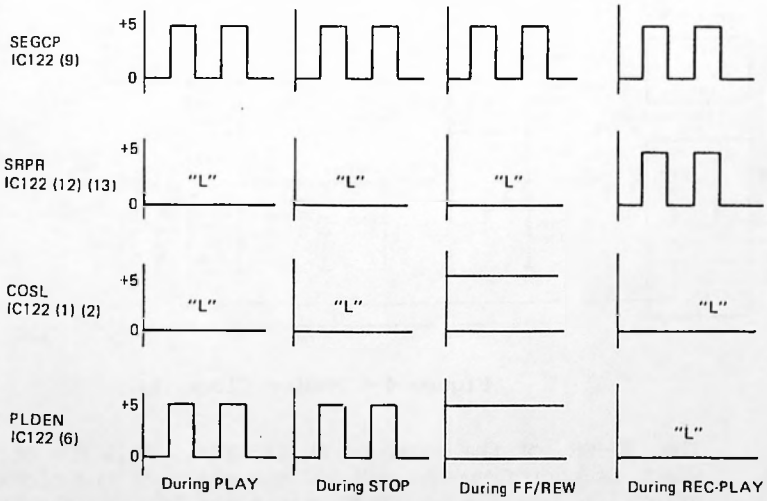


Figure 4-7 Timing Chart for the Various Operations

2) DF PLL Operation

The DF (Digital Filter) PLL generates the clock which is required by the digital filter in the audio circuit. The VCO has an fc of 18.432 MHz. Part of this output is divided by the 1/12 divider within the IFGA (IC-105) and fed back to the DF PLL (IC-111) where the phase is compared with DSIFT to control the VCO. PLL18M (an 18 MHz clock which is syncronized in phase with the DSIFT clock) is output from pin 4.

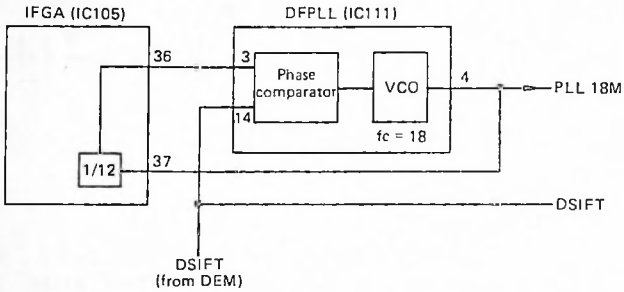


Figure 4-8 DF PLL Circuit

3) Master Clock PLL

This PLL generates a 28.224 MHz master clock which is phase syncronized with LR (= fs: sampling frequency). The master clock (28MCK) is divided in the DSP to provide various clocks required by the system control circuit and servo circuit.

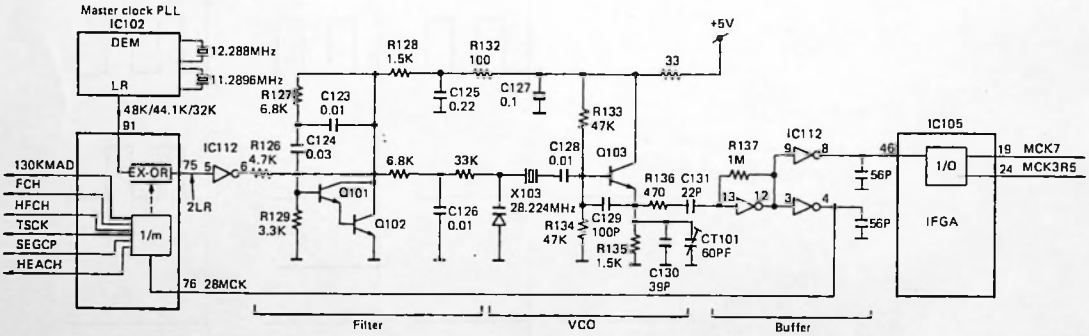


Figure 4-9 Master Clock PLL

The EX-OR of the phase of LR (48 KHz, 44.1 KHz or 32 KHz) which is sent from the DEM and the phase of the clock obtained after 1/m division of 28MCK within the DSP is taken to control the control voltage to the VCO. This produces the 28 MHz master clock which is synchronized with the LR clock.

4) DIN PLL Circuit

The DIN (Digital Filter) PLL operates only when the digital signal from the digital input terminal is applied and generates a clock (D24M = 24 MHz clock pulse) which is synchronized with the input digital signal.

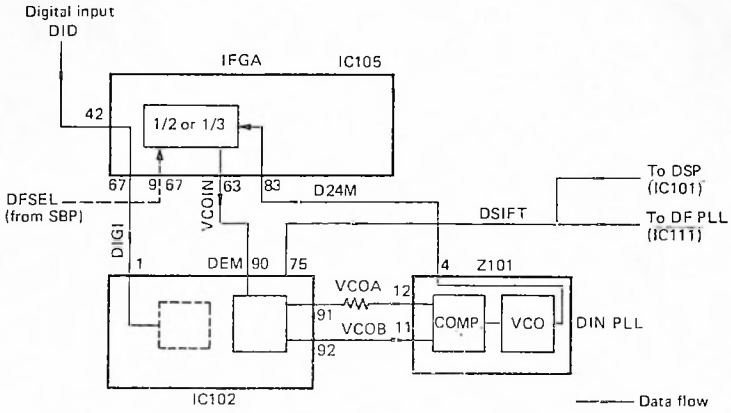


Figure 4-10 DIN PLL Circuit

5) Clock Generation

The flow of the clock generation during playback and recording is shows in figure 4-11 to 4-13.

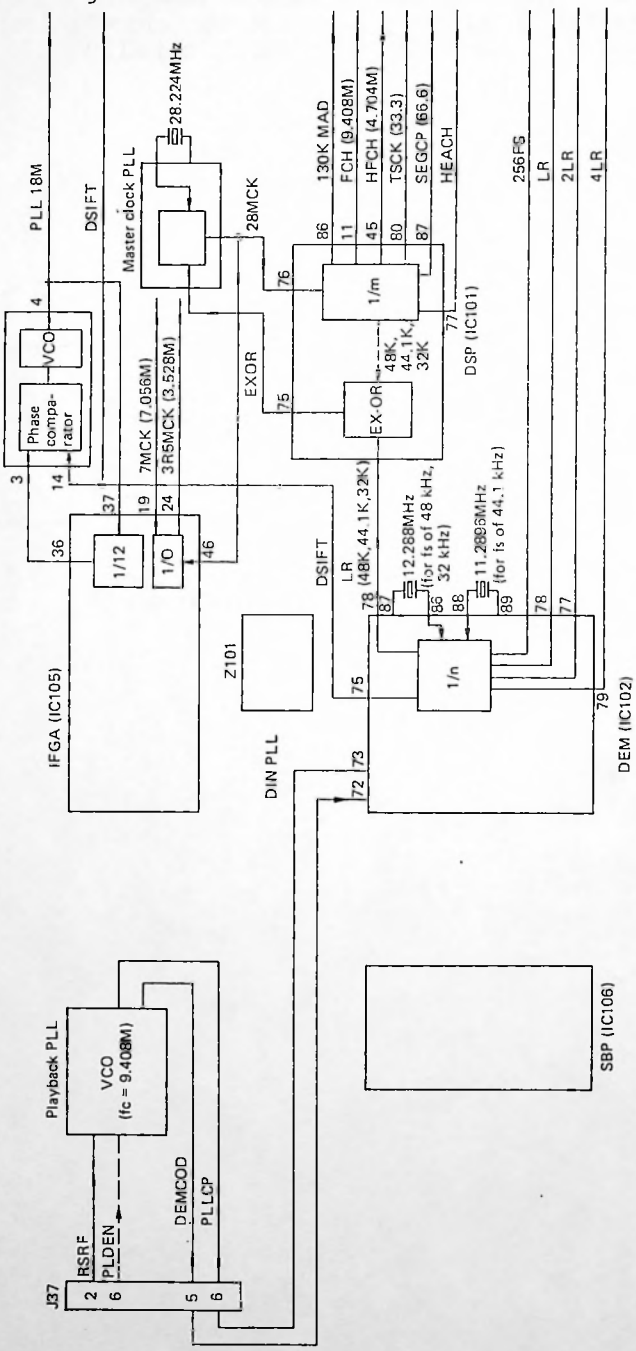


Figure 4-11 Clock Generation I: Playback

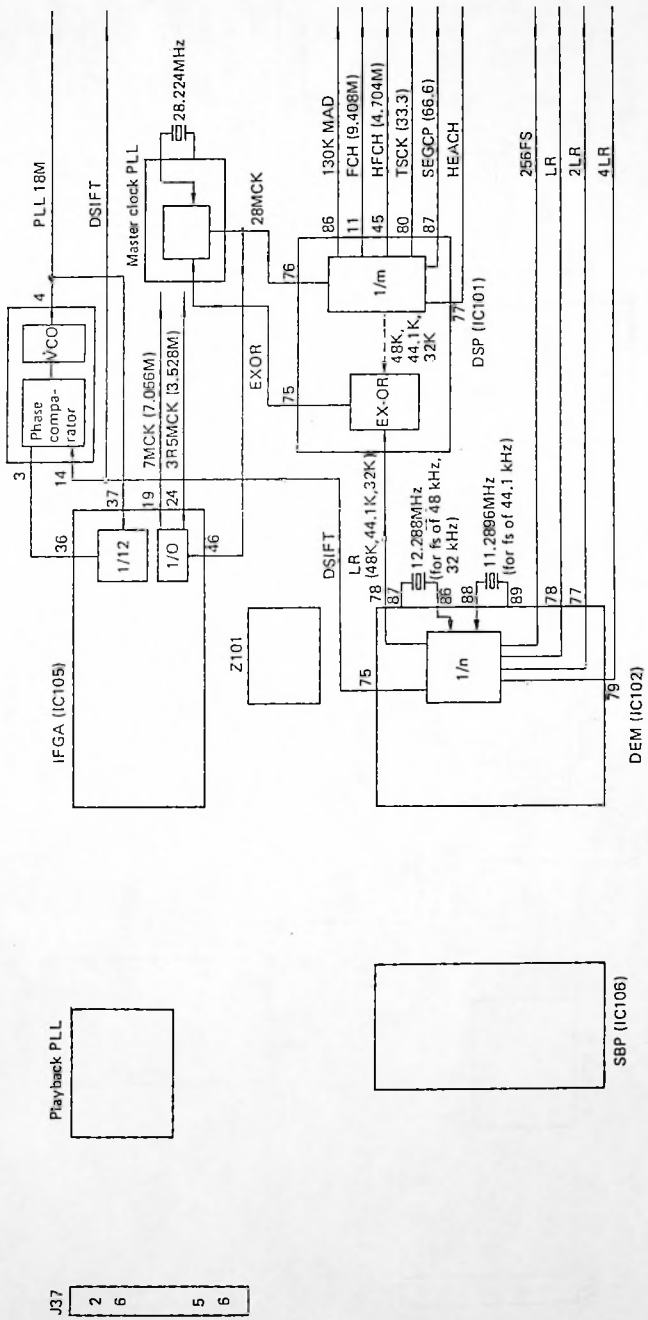


Figure 4-12 Clock Generation II: Analog Input Recording

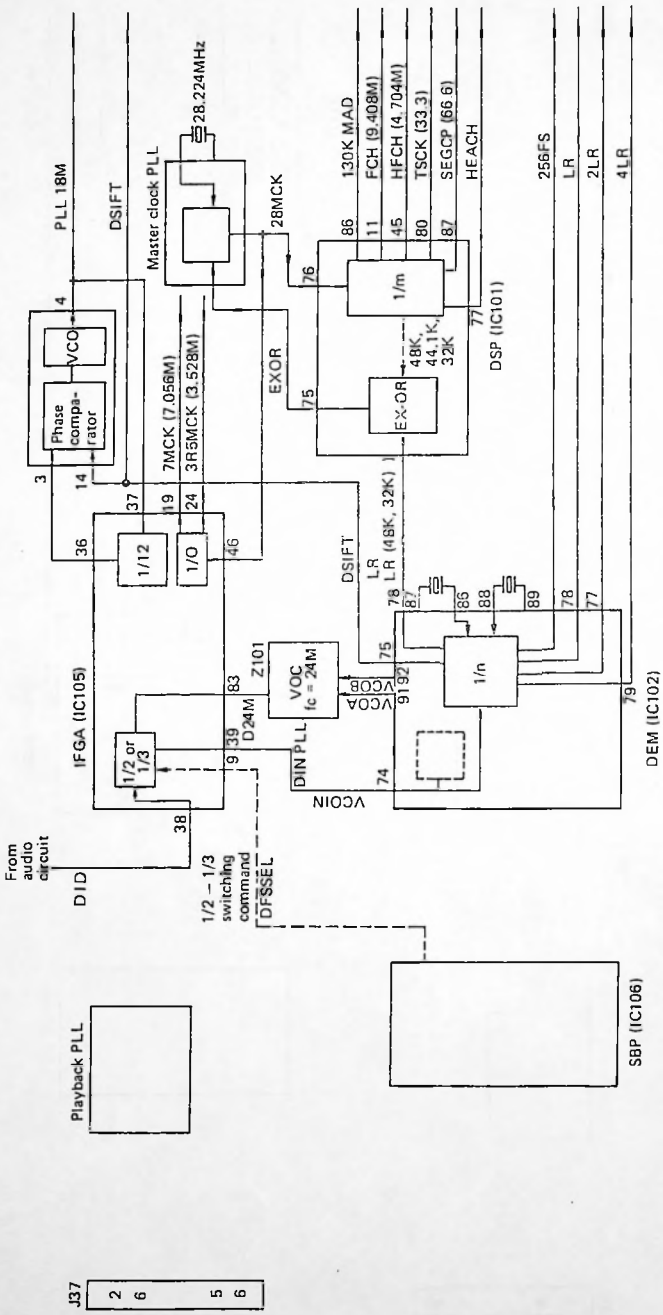


Figure 4-13 Clock Generation III: Digital Input Recording

6) Clocks Generation in the Signal Processing Circuit

Clock Name	Frequency	Mode			
		Playback	Analog Recording	Digital Recording	Application
PLLCP (PLL clock pulse)	9.408MHZ	o	-	-	For playback data read
PLL 18M (PLL 18MHz)	18.432MHz	o	o	o	For DF
130KMAD (130KHz window)	130 KHZ	-	o	o	
FCH (clock frequency)	9.408MHz	o	o	o	
HFCH (half FCH)	4.704MHz	o	o	o	
TSCK	33.3Hz	o	o	o	
SEGCP (segment clock pulse)	66.6Hz	o	o	o	
HEACH (head up switching)					Head up switching
256FS (sampling x 256)	12.288MHz 11.289MHz 8.192MHz	o	o	o	
LR (left/right switching	48KHz 44.1KHz 32KHz	o	o	o	Analog clock
DSIFT (data shift)		o	o	o	
7MCK	7.056MHz	o	o	o	System control clock
3R5MCK	3.528MHz	o	o	o	

Table 4-1

4-4. Subcode RAM

The data in the subcode area is read by the head during playback, separated by the DEM and sent to the SBP (subcode processor). During recording, the subcode data is sent from the system control circuit to the SBP. The subcode RAM is used to temporarily store the subcode data.

Reference Note

There is the possibility of error being generated as data is read from the tape by the head during playback. For this reason, parity codes are also recorded simulataneously with the data in the subcode area. If the parity codes do not match, the data is judged to contain an error and is not used. The subcode contains in one track, 8 blocks each of SUB-1 and SUB-2 for a total of 16 blocks. Furthermore, since one block contains 256 bits (= 32 symbols), the capacity is 4096 bits. Also the cylinder is fitted with two heads and rotates at 2000 rpm. Thus, one second of the subcode data area contains:

4096 (bits) x 2000 (rpm)×2 (heads) / 60 (seconds) = 273Kbits

When a set of data is received from heads A and B, the data within the RAM is transferred to the system control circuit.

Data is written to the RAM when RWE is low and read from the RAM when ROE is low.

Reference Note

The playback data received by the DEM IC-102 includes, in addition to the subcode data, various types of data in the PCM area such as music data and parity codes. Since the various types of data are recorded in a consistent sequence, the subcode data can be separated from the playback data if they are sorted according to the sequence.

Subcode RAM

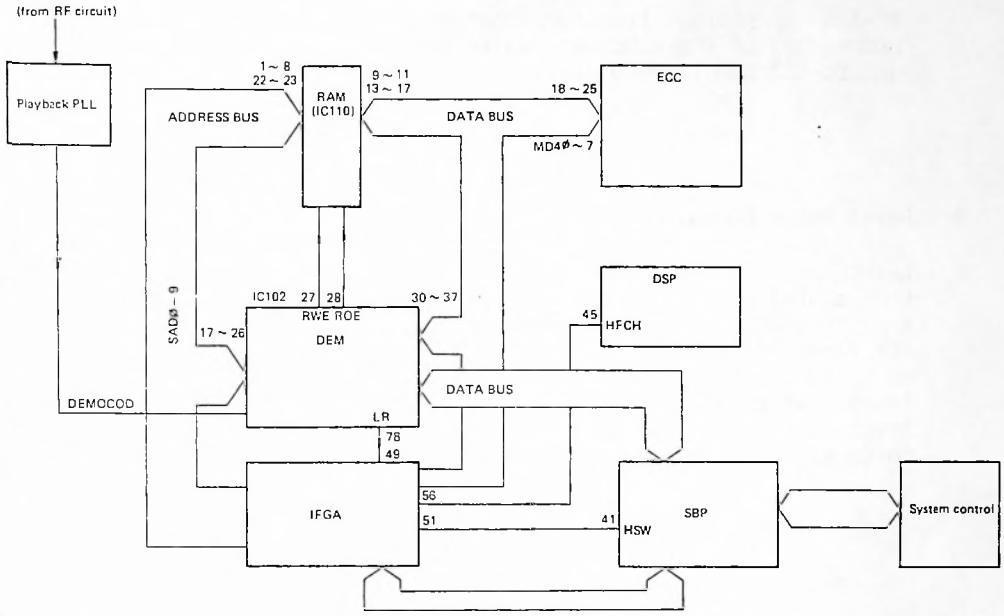


Figure 4-14

1) During Playback

The separated subcode data is first stored in the subcode RAM IC-110. The parity of the data is checked and, if there is an error, the data is ignored. If there is no error, the subcode data is sent to the SBP through the data bus and then transferred to the system control circuit. The system control circuit which receives the data controls the mechanism according to the set mode (search, A-B repeat, etc) changes the displayed time, and performs other operations. During playback, the contents of the RAM are cleared every 15 ms to prevent the old and new data from combining in the RAM.

2) During Recording

As shows in figure 4-3, there are many types of data that are written in the subcode area. The various types of data are assembled in the signal processing circuit based on the data input through the keyboard, data read previously from the tape for playback (previous program number, privious absolute time, etc), and commands sent from the system control circuit. After parity codes are added to the data in the subcode area and program addresses are added within the DEM, the data is sent to the RF circuit.

3) Subcode Data Processing

IC-106 performs transfer control for the SBP (subcode processor) of the subcode data between the system control CPU and IC-102 DEM (demodulator).

4-5. Level Meter Signal

Level meter signal consisting of digital data are sent from the signal processing circuit to the level meter circuit in the SV-3500. A/D converted digital music signals are sent to the level meters during recording and demodulated signals are sent to the D/A convertor during playback. As a result, the level meter indicates the level withouit any error since the level of the data (being recorded on tape or already recorded on tape) is directly decoded and displayed.

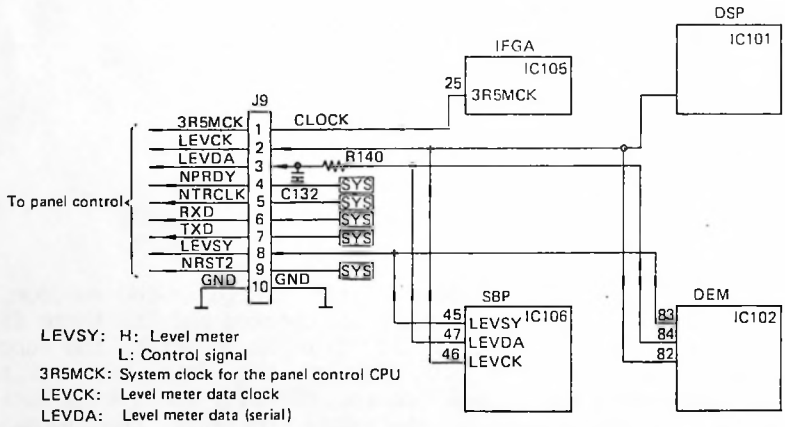


Figure 4-15

Part of the signal processing circuit related to the level meter indication is shows in figure 4-15. Described here are pins 4 to 7 and pin 9 of J9 which are data transfer lines between the system control circuit and the panel control circuit.

4-6. Switching of Signal Flow

It is necessary to switch the inputs, outputs, playback signals, recording signals and level meter signals in the SV-3500 according to its mode. Mode data is sent from the system control circuit to the SBP IC-106, and then from the SBP to the IFGA IC-105. Signals are muted at the IFGA according to the mode data.

CDCP1 : Data output for digital IN (during recording)
Shift clock for the ID in playback data.

HEACH : Head up switching signal H=REC , L=PLAY

ADD : Digital data during analog input recording

DIGO : Output signal for digital I/O

DID : Data decoded from the digital input

DADAT : Output of the DA data (DSP output)

SRPR : REC command

DIGI : Digital I/O

DSM : Digital filter output mute command

DOD : Digital output data

ADDAT : Recording data

DFD : Data which is sent to the digital filter circuit. After D/A conversion, this data becomes the music signal.

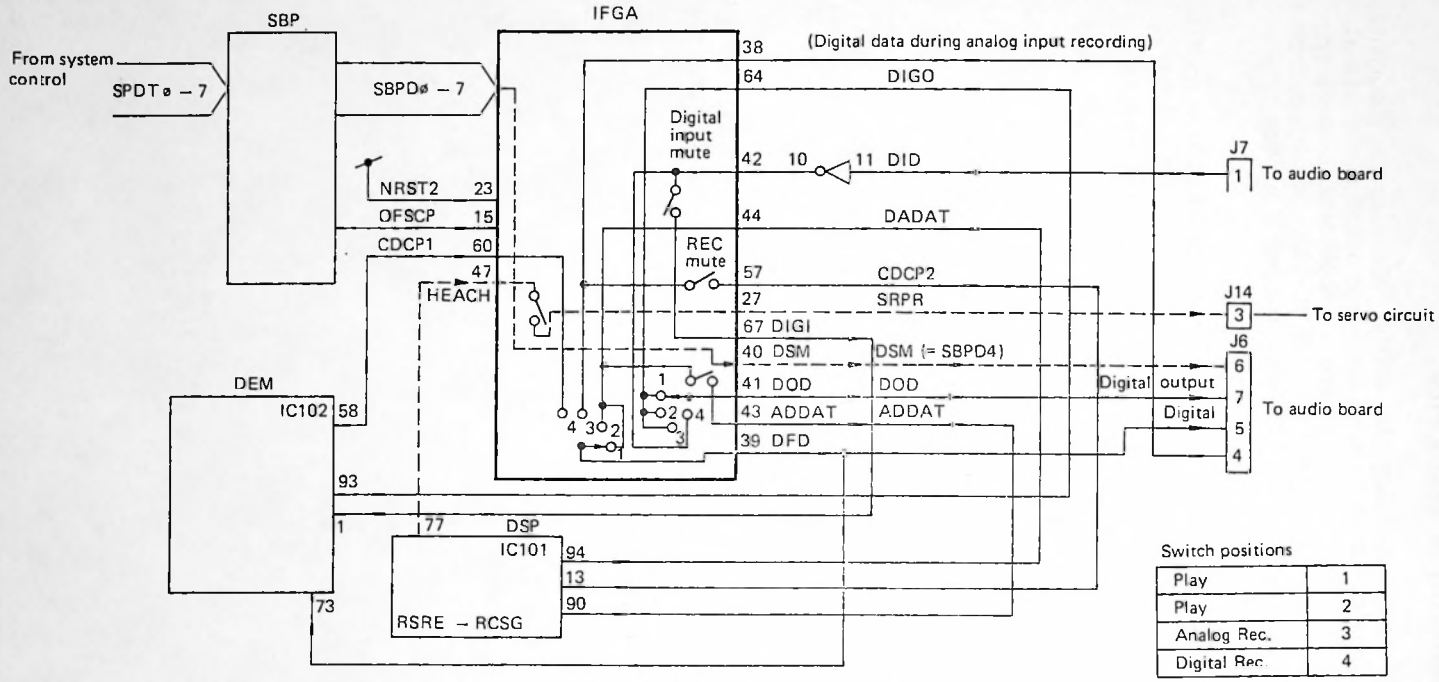


Figure 4-16 Signal Selector Circuit

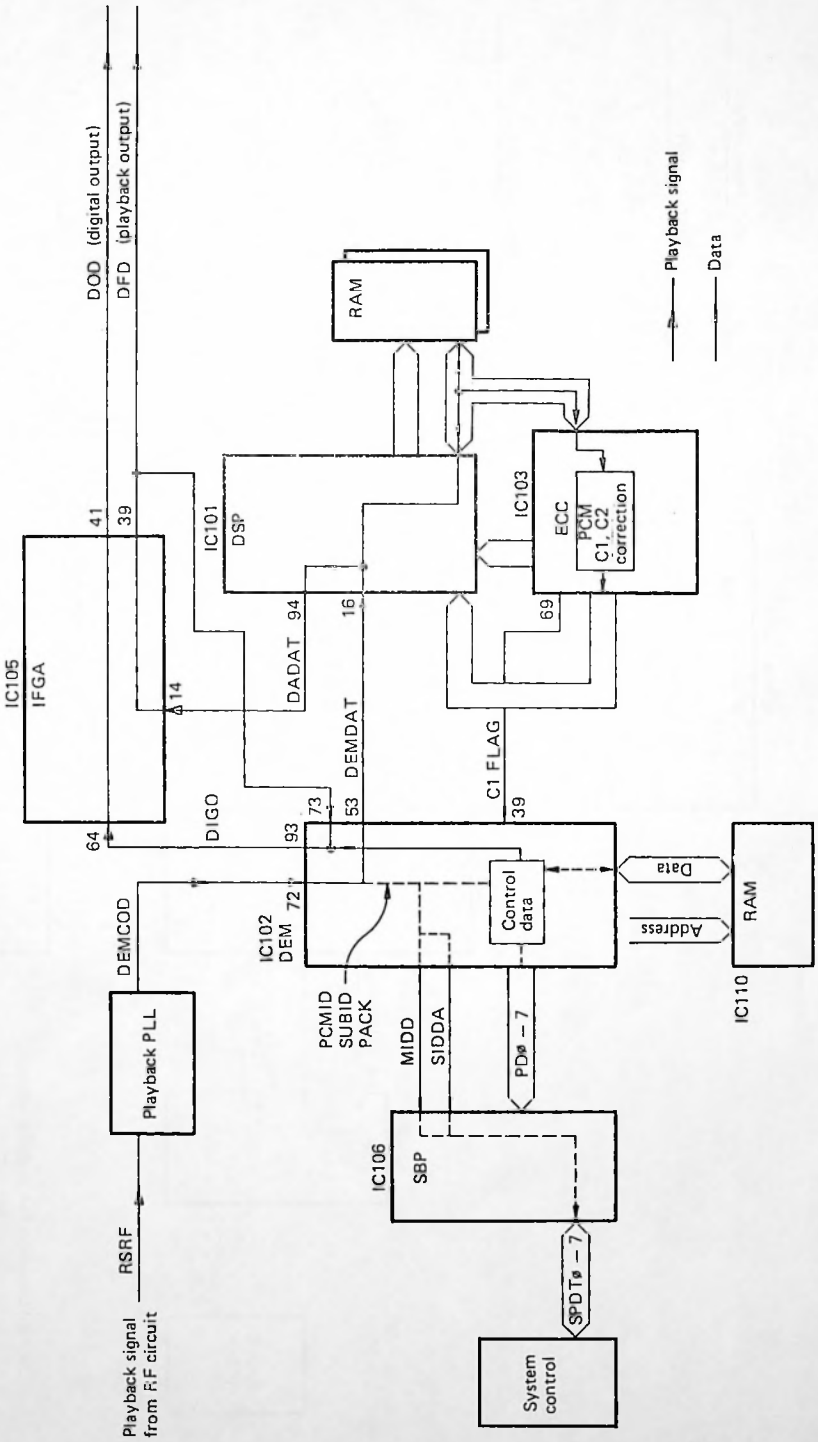


Figure 4-17 Signal Flow During Playback

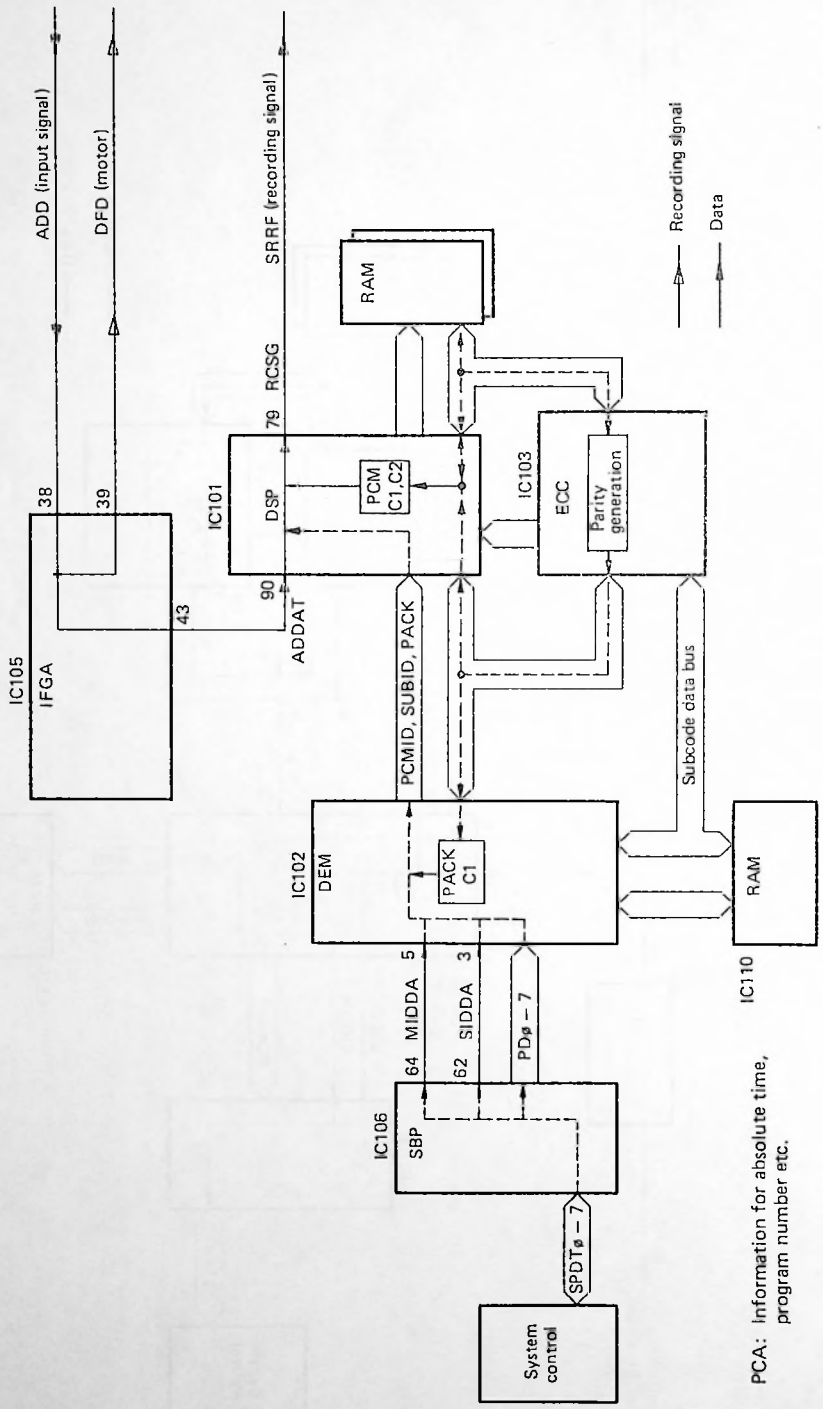


Figure 4-18 Signal Flow During Analog Input Recording

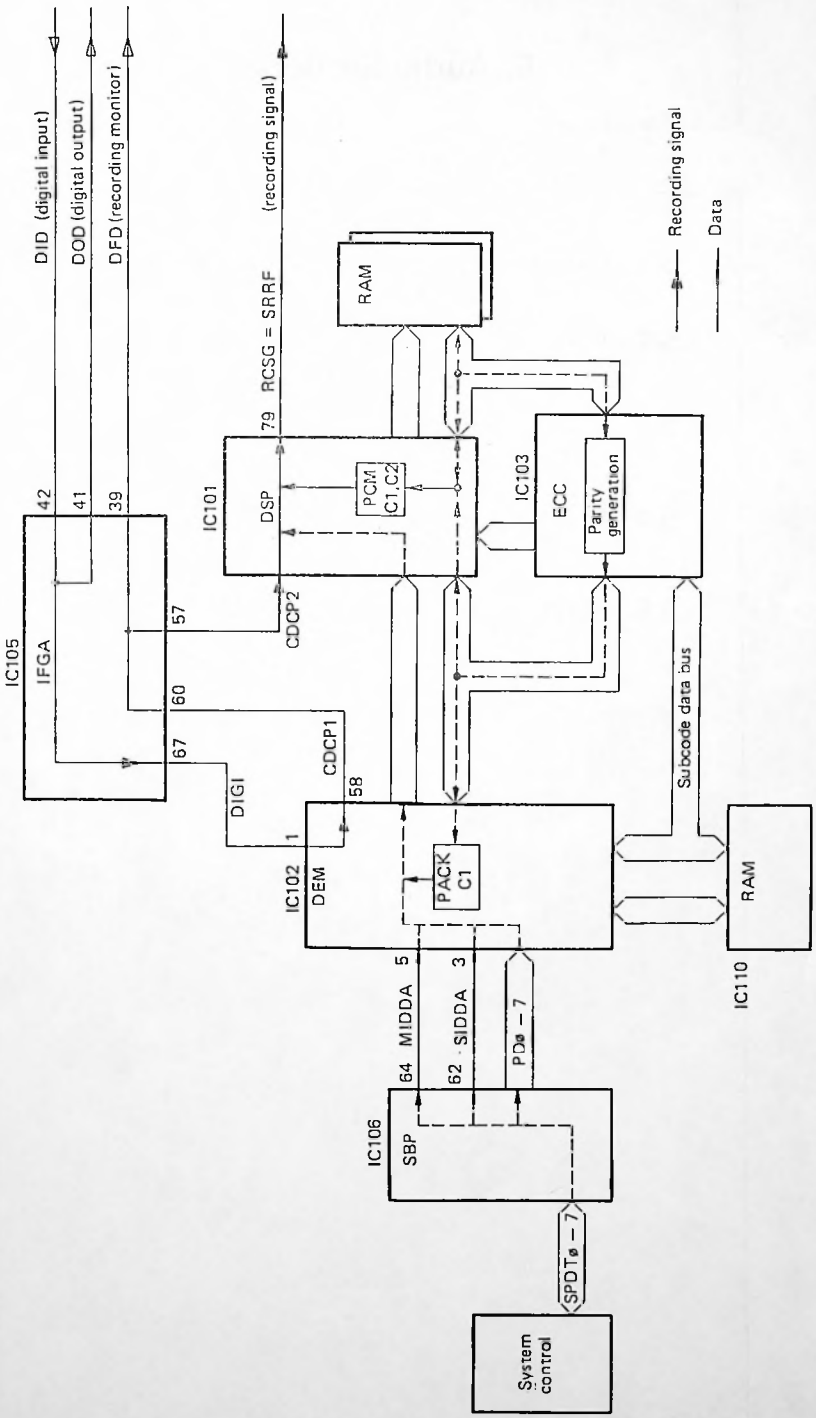


Figure 4-19 Signal Flow During Digital Input Recording

5. Audio Section

5-1. Recording Circuitry Block Description

5-2. Recording Circuitry Operation

5-3. Level Switching Circuit

5-4. Playback Circuitry Block Description

5-5. Playback Circuitry Operation

5-1.Recording Circuitry Block Description

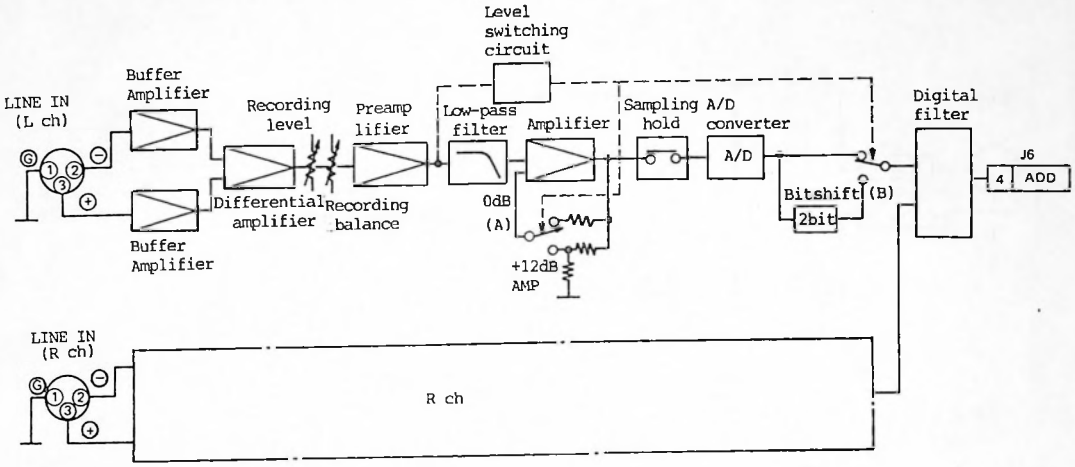


Figure 5-1-1

1) The music signal input through LINE IN passes the buffer amplifier, differential amplifier, level adjustment variable resistor and preamplifier,and is input to the low-pass filter where the components outside the audio frequency range are removed. The signal is then sent to the buffer amplifier in the next stage.

2) The level switching circuit inputs the preamplifier's output and detects if the recording level is higher than -12 dB. If the level is higher than -12 dB, switch A closes on the 0 dB side and switch B closes on the A/D converter side. If the level is lower than -12 dB, switches A and B close at the oppesite positions.

3) Next, the output from the buffer amplifier is sampled at the sampling hold circuit. The sampling frequency is 96 KHz.

4) The sampled signal is input by the A/D converter where it is quantized and then sent to the digital filter. The digital filter changes the sampling frequency to 48 KHz. It also converts the two data signals, which have each been A/D converted to the left and right channels, into a sigle data signal in which the left channel data is followed by the right channel data. The single data signal is sent to the signal processing circuit as A/D output data through pin 4 of J6.

5-2. Recording Circuitry Operation

1) From LINE IN to the Low-Pass Filter

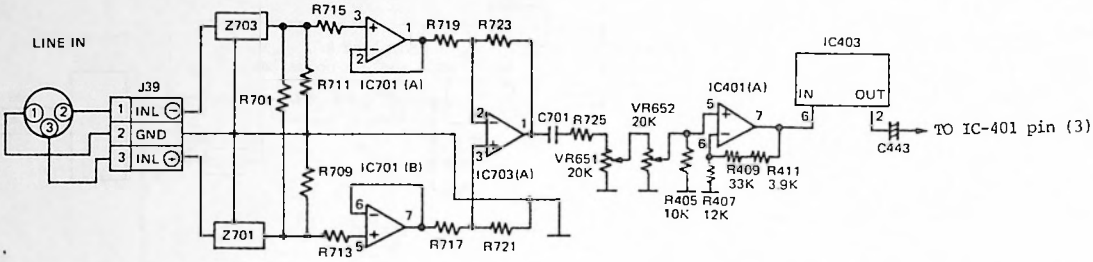


Figure 5-2-1

(1) The signal from LINE IN is input by pin 3 of IC-701(A) and pin 5 of IC-701(B) where its impedance is transformed, passes 2 and 3 of IC-703 where balanced amplification is performed. The output from pin 1 is further passes recording level variable resistor VR651 and balance variable resistor VR652, and is sent to pin 5 of peramplifier of IC-401(A).

(2) The signal amplified at IC-401(A) is output from pin 7 and sent to pin 1 of low pass filter of IC-403 where the unwanted components above the frequency range (22 KHz and higher) are removed to prevent loopback noise. The characteristics of the low-pass filter are shows in figure 5-2-2.

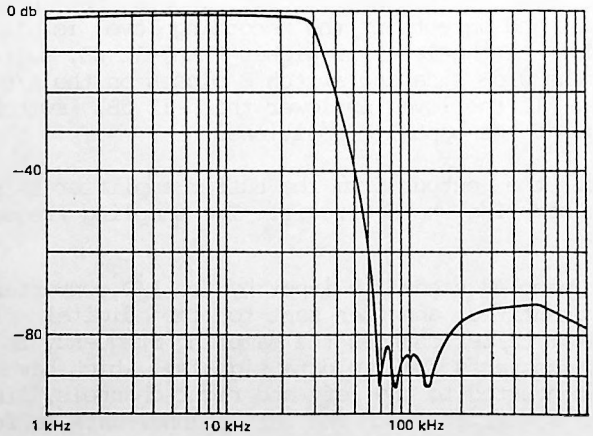


Figure 5-2-2

2) From the Low-Pass Filter (OUT) to the Sampling Hold Circuit

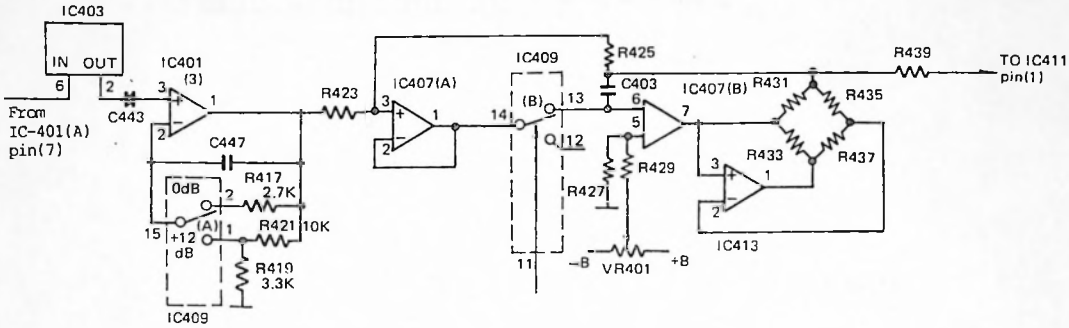


Figure 5-2-3

(1) The signal output from pin 2 of low pass filter IC-403 is input to pin 3 of amplifier IC-401(B). The gain of amplifier IC-401(B) is selected by analog switch IC-409(A).

(2) The analog switch IC-409(A) selects pin 1 or pin 2 depending on the level of the signal switch is input by LINE IN.

(3) The output from pin 1 of IC-401(B) is sampled at the sampling hold circuit composed of IC-407(A) and (B), IC-409(B) and IC-413. The C403 is a holding capacitor. VR401 is a veriable resistor used to adjust the offset for the A/D converter.

The timing chart for the sampling operation is shows in figure 5-2-4. The sampling frequency is 96 KHz or double the standard 48 KHz. This is used to smooth the frequency characteristics of the low-pass filter IC-403 (which reduces the ripple at the high frequency characteristics) and greatly improves the phase characteristics.

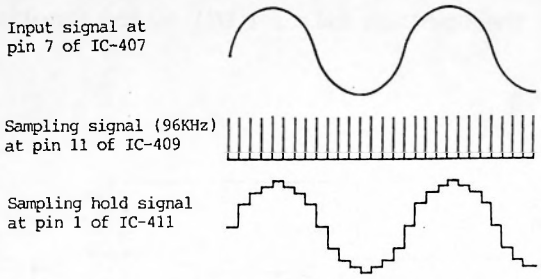


Figure 5-2-4

3) From the A/D Converter to the Digital Filter

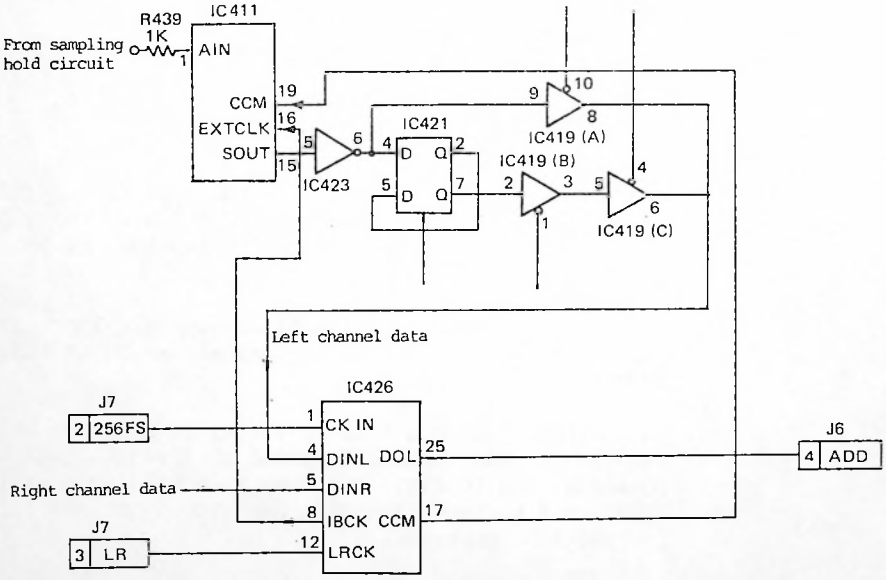


Figure 5-2-5

(1) The analog signal from the sampling hold circuit passes R439 and is input by pin 1 of A/D converter IC-411. It begins to be A/D converted according to the CCM signal which is input by pin 19 of IC-411. After the A/D conversion, it is output from pin 15 of IC-411 as a 16 bits serial data signal.

(2) When the recording level of the data signal input by pin 5 of IC-432 is higher than -12 dB, it is sent to pin 4 of digital filter IC-426 through IC-419(A). If it is lower than -12 dB, it is sent to pin 4 of IC-426 through IC-421 and IC-419 (B) and (C).

(3) At digital filter IC-426, the left channel data (input by pin 5) are rearranged into a serial signal. Simultaneously, the 96 KHz sampling frequency is converted (halved) to a 48 KHz sampling frequency, output from pin 25 of IC-426 and sent to the signal processing section through pin 4 of connector J6. The A/D conversion and left/right serial data conversion are shows in figure 5-2-6.

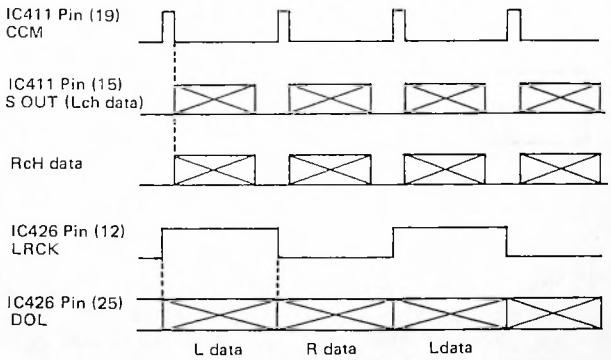


Figure 5-2-6

5-3. Level Switching Circuit

When a small input level is A/D converted, the noise generated after the low-pass filter becomes loopback noise and cannot be ignored. Further distortion is generated due to the small signal characteristics of the A/D converter since its linearity deteriorates. The level switching circuit is designed to improve these two characteristics.

1) Block Diagram Description

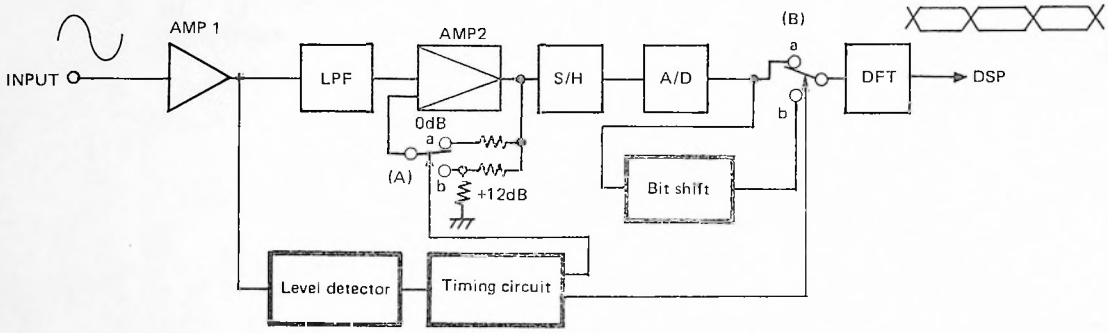


Figure 5-3-1

(1) The level detector determines whether the recording level of the signal output from amplifier 1 is higher or lower than -12 dB, and controls switches A and B through the timing circuit.

(2) If the signal is higher than -12 dB, the main circuit blocks are used and switches A and B shows in figure 5-3-1 are both set to position "a".

(3) However, if the signal is lower than -12 dB, switches A and B are both set to positions "b". The input signal has its level amplified by 4 times by selecting switch at "b" position. At the same time, the data signal after A/D conversion is shifted by 2 bits from the MSB to the LSB by the bit shift circuit. This decreases the signal by 1/4 and restores the gain (of the signal which was amplified 4 times by selecting switch at "b" position) to its original level.

(4) Next, the level detector, timing circuit and bit shift circuit are described in more detail.

2) Level Detector

This circuit determines whether the recording level is higher or lower than -12 dB.

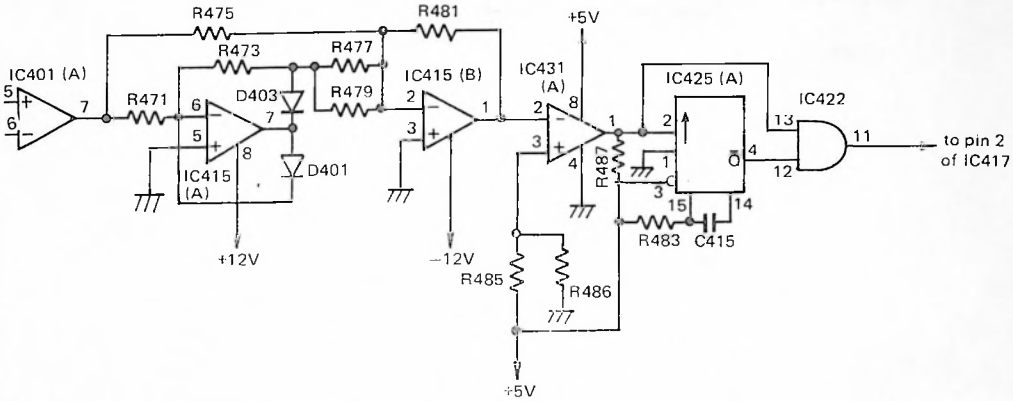


Figure 5-3-2

(1) The music signal output from pin 7 of IC-401 is rectified by a full-wave rectifier circuit composed of IC-415 (A and B), D401 and D403.

(2) IC-431 is a comparator which uses pin 3 for its reference. When the level of a signal which is input by pin 2 is higher than -12 dB, which is the reference value of pin 3, the output at pin 1 goes low. Conversely, if the level of the signal is lower than -12 dB, pin 1 goes high.

(3) IC-425(A) is a one-shot multivibrator with its time constant determined by C415 and R483. It prevents pin 1 of IC-431 from going high for a period of approximately 150 ms when the recording level drops to below -12 dB.

(4) When the recording level is higher than -12 dB, pin 13 of IC-422 is low and pin 12 is high. Thus, pin 11 is low. Conversely, when the recording level is lower than -12 dB, pin 13 is high which makes pin 11 also high. Figure 5-3-3 shows the signals when the recording level drops from above -12 dB to below -12 dB.

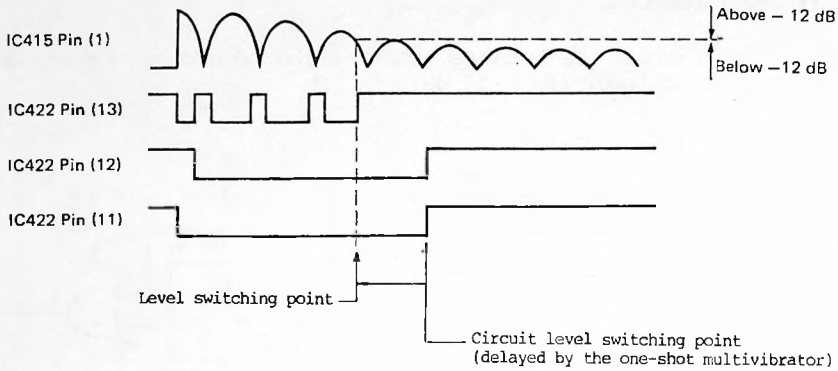


Figure 5-3-3

3) Timing Circuit

This circuit uses the SH signal and controls the timing for the switching for recording levels higher and lower than -12 dB.

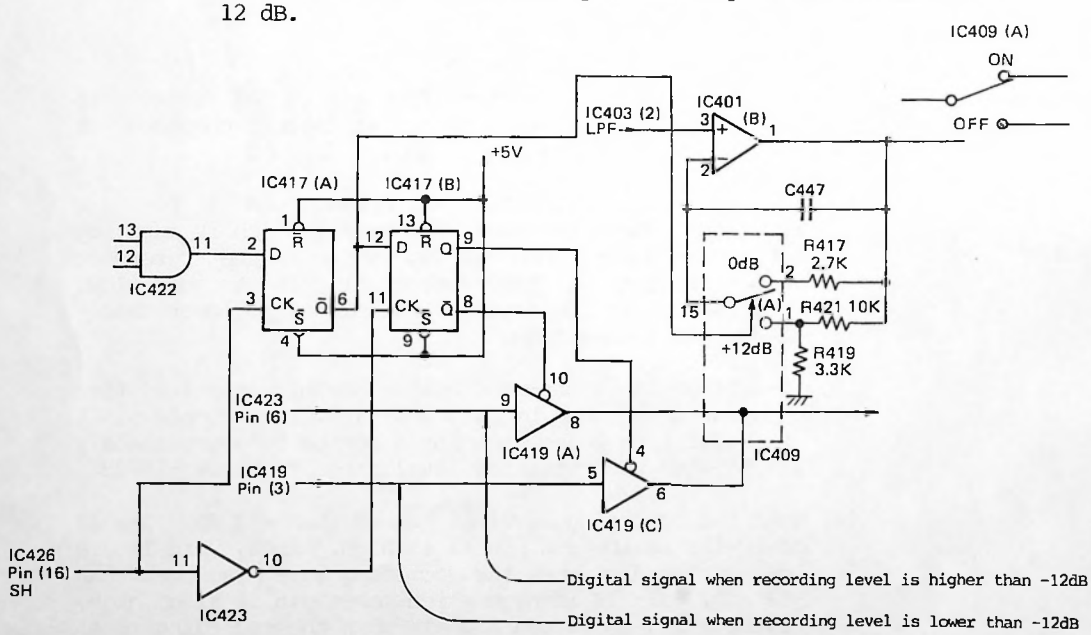


Figure 5-3-4

(1) When the input recording level is higher than -12 dB.

(a) Pin 11 of IC-422 is low. Thus, pin 6 of IC-417 goes high.

(b) The high input at pin 6 of IC-417(A) causes analog switch IC-409(A) to turn on. The music signal from the LPF then passes the amplifier of IC-401(B) and is output.

(c) At the same time, the high signal input by pin 12 of IC-417(B) is output as a low signal from pin 8 of IC-417(B) due to the operation of the D-type flip-flop. This output causes pin 10 of IC-419(A) to go high. The A/D converted digital data signal from pin 6 of IC-423 passes from pin 9 to pin 8 of IC-419(A) and is output.

(2) When the input recording level is lower than -12 dB.

(a) Pin 11 of IC-422 is high. Thus, pin 6 of IC-417 goes low.

(b) The low input at pin 6 of IC-417(A) causes analog switch IC-409(A) to turn off. The music signal from the LPF then passes the +12 dB (4 times) amplifier of IC-401(B) and is output.

(c) At the same time, the low input at pin 12 of IC-417(B) is output as a low signal from pin 9 of IC-417(B). This output causes pin 4 of IC-419(C) to go low. The digital data signal from pin 3 of IC-419(B) passes from pin 5 to pin 6 of IC-419(C). Figure 5-3-5 shows the timing when the level drops from above -12 dB to below -12 dB.

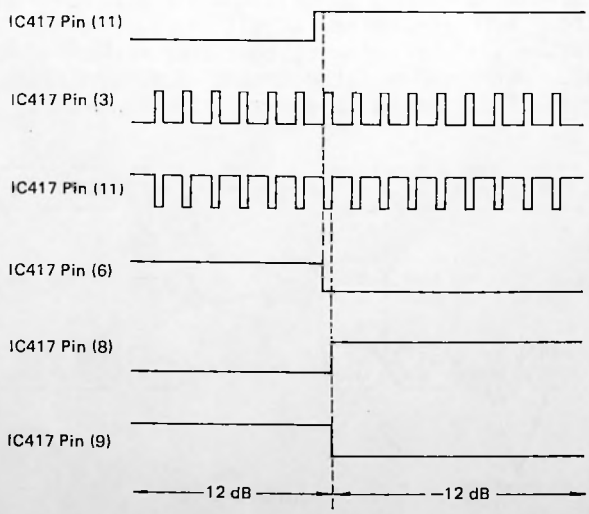


Figure 5-3-5

4) Bit Shift Circuit

The gain is 4 times the original when the recording level is lower than -12 dB. To reduce the gain, the signal is shifted two bits from the MSB to the LSB, with the two extra LSB bits truncated.

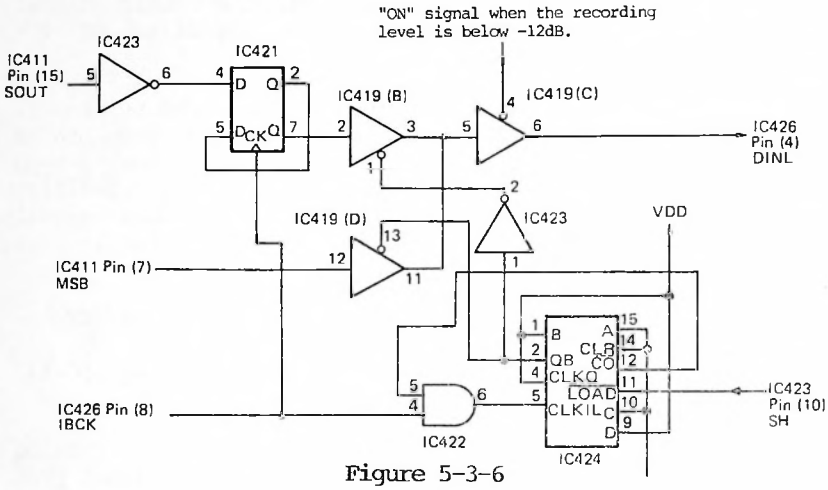


Figure 5-3-6

(1) The A/D converted digital signal input by pin 5 of IC-423 is inverted by IC-423, passes two D-type flip-flops within IC-421, is shifted two bits from the MSB to the LSB, and has the two extra bits truncated by the gate circuit in IC-419(B).

(2) Next, since two bits are shifted as described above in(1), the MSB side lacks two data bits. The gate circuit IC-419(D) inserts the two MSB data bits output from A/D converter IC-411 to pin 5 of IC-419(C). Further, the counter circuit composed of IC-424 and IC-422 synchronizes the timing when inserting the MSB bits. This timing is shows in figure 5-3-7.

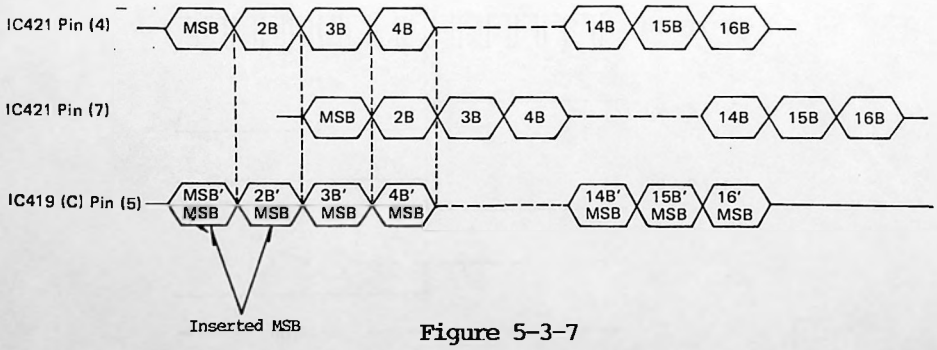


Figure 5-3-7

5-4.Playback Circuitry Block Description

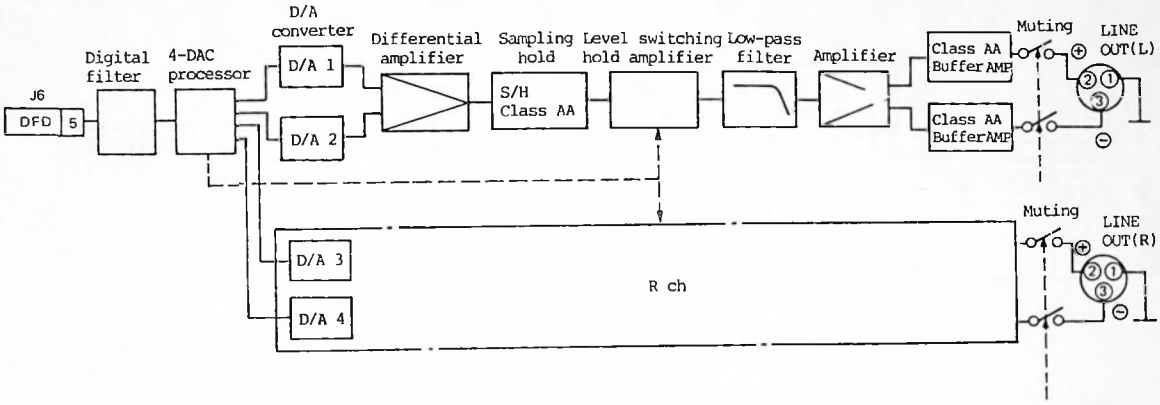


Figure 5-4-1

(1) The digital data signal which is input from pin 5 of J6 is subjected to 4 times over sampling and sent to the 4DAC processor.

(2) At the 4DAC processor, the input digital data signal is separated and distributed to four D/A converters according to the type of data signal.

(3) At the D/A converters, the PAM signal (which was D/A converted by D/A 1 and D/A 2) is generated. The PAM signals are combined amplified by differential amplifier.

(4) The combined signal is sent to the sampling hold circuit to recover the recorded music signal.

(5) During operation of the 4DAC processor, the level switching amplifier output the equivalent of 18 bits data when digital data with a recording level below -12 dB is input. The level switching amplifier is provided to decreaes the gain when the gain of the D/A converter increases 4 times.

(6) The music signal from the level switching amplifier is input to the low-pass filter where the components outside the audio frequency range are removed. The music signal is then sent to the amplifier in the next stage, passes the muting relay and is output from LINE OUT.

5-5. Playback Circuitry Operation

1) From the Digital Filter to the 4DAC Processor

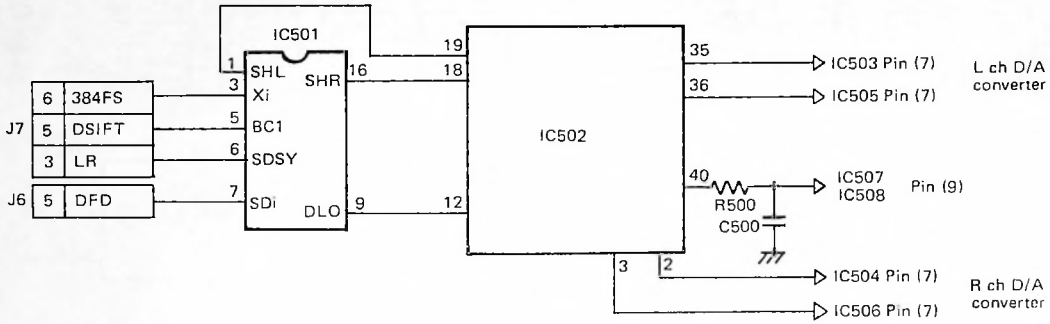


Figure 5-5-1

(1) The digital playback data signal from pin 5 of J6 is input by pin 7 of digital filter IC-501. It is input in sequence for the left channel and right channel with a period of 48 KHz. Based on processing operations within IC-501, it is output from pin 9 of IC-501 with the 4 times over sampling period of 192 KHz.

(2) The playback data signal from pin 9 of IC-501 is input by pin 12 of 4DAC processor IC-502. At IC-502, the operation changes according to the input level. The operation of IC-502 is described next.

(a) When the input is a playback data signal which is lower than -12 dB with respect to the full-scale level:
The data is determined to be either positive or negative. If positive, it is output to pin 35 and sent to D/A converter IC-503. If negative, it is phase inverted, output to pin 36 and sent to D/A converter IC-505.

(b) When the input is a playback data signal which is higher than -12 dB with respect to the full-scale level:
The data is output simultaneously to both pins 35 and 36, regardless of whether the data code is positive or negative. At this time, the phase at pin 36 is inverted.

2) From the D/A Converter to the Level Switching Amplifier

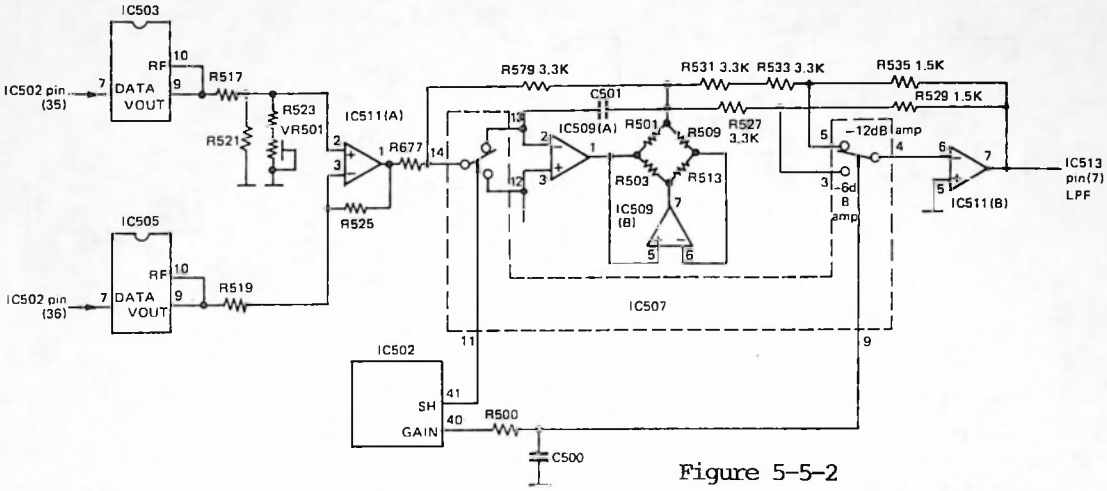


Figure 5-5-2

(1) The playback data signals which are input by pin 7 of IC-503 and pin 7 of IC-505 are D/A converted and output to pin 9 of IC-503 and pin 9 of IC-505 as PAM signals. The output PAM signals are input to pin 2 and 3 of IC-511(A) where they are combined and then sent to the sampling hold circuit.

(2) The circuit consist of IC-507, C501, IC-509 is sampling hold circuit. The output signal pass the bridge resistors in the class AA circuit and the sent to level switching amplifier IC-511(B) in the next stage. Figure 5-5-3(A) shows the PAM signals when the input playback data signals are lower than -12 dB with respect to the full-scale level and figure 5-5-3(B) shows the PAM signals when the input playback data signals are higher than -12 dB with respect to the full-scale level.

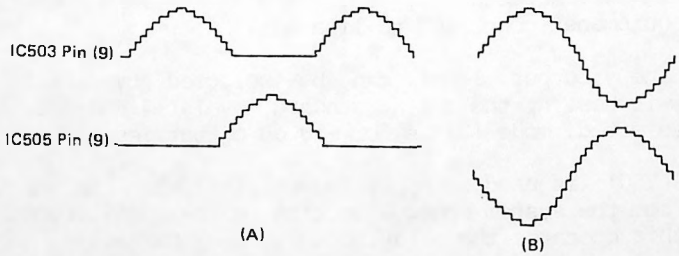


Figure 5-5-3

(3) Level switching amplifier IC-511(B) is controlled by 4DAC processor IC-502. When the 4DAC processor is activated by an input signal which is lower than -12 dB with respect to the full-scale level, pin 9 of IC-507 goes high and the gain of amplifier IC-511(B) becomes -12 dB. Further, when it is activated by an input signal which is higher than -12 dB with respect to the full-csale level, pin 9 of IC-507 goes high and the gain of the amplifier becomes -6 dB.

3) From the Low-Pass Filter to LINE OUT

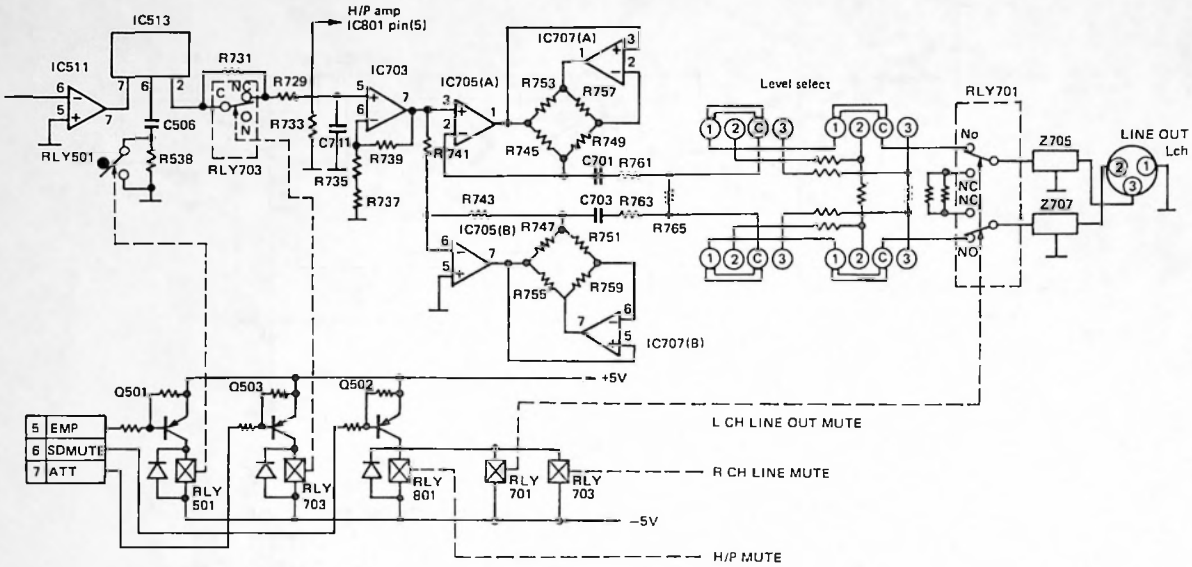


Figure 5-5-4

(1) The music signal, which is input to pin 7 of low-pass filter IC-513, has its components above 22 KHz removed, is output from pin 2 of IC-513 and sent to amplifier IC-703. The output from IC-703 pin 7 is separated and applied pin 3 of IC-705(A) and pin 6 of IC-705(B). The IC-705(A) and IC-707(A) functions a non inverting class AA amplifier, where as IC-705(B) and IC-707(B) functions an inverting class AA amplifier.

It is an extremely low distortion class AA amplifier which is not affected by any changes in impedance in the equipmenet connected to line out.

Line output level can be selected by level select switches. At the moment stndard level (+4 dB) mode (1) are selected. mode (2) is for -10 dB output level.

(2) RLY501 is used to apply deemphasis. When the EMP signal from the system control section is low, Q501 turns on and this operates the relay to apply deemphasis.

RLY703 is used to insert an attenuator into the circuit to protect the speaker during the cue and review modes by reducing the level of the music signal. When the ATT signal is low, Q503 turns on and the attenuator is inserted.

RLY701 is the muting relay, It is turned off except during the playback, recording, recording pause, cue and review modes, to mute the output from LINE OUT. When the SDMUTE signal is low, Q502 turns on which turns on the relay.

6. Panel Control

6-1. General

6-2. Signal Flow in the Panel Control Circuit and Peripheral Circuits

1) Signal Processing Circuit

2) System Control Circuit

3) Key Scan and Remote Control Input Circuit

4) FL Displays and LED Indicators

(1) FL Display
(2) LED Indicator
(3) Level Meter

6-3. Test Program Function

1) Procedure

2) Operation

(1) Display
(2) All Display Mode

6-1. General

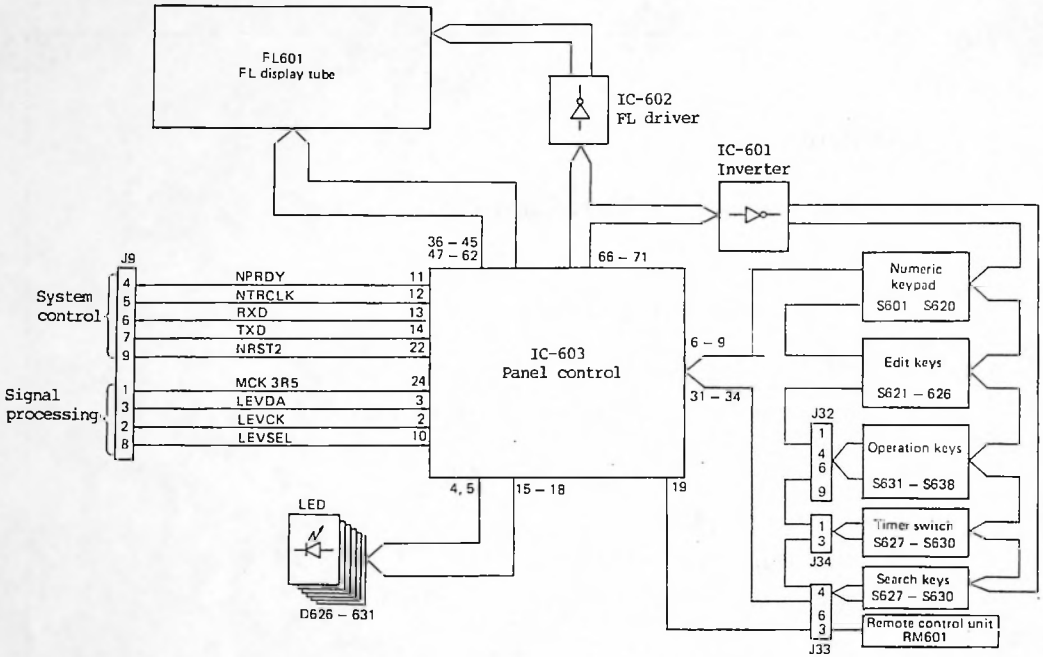


Figure 6-1-1 Block Diagram

The front panel keys, configured as key matrix, are scanned and signals from the wired remote control are received. The panel control circuit sends corresponding codes to, and receives data from, the system control circuit. Based on this data, the FL display tube and LED indicators are illuminated to indicate the current mode of the player.

Furthermore, level data from the signal processing circuit is read and indicated on the level meter, which is equipped with the peak hold function.

6-2. Signal Flow in the Panel Control Circuit and Peripheral Circuits

1) Signal Processing Circuit

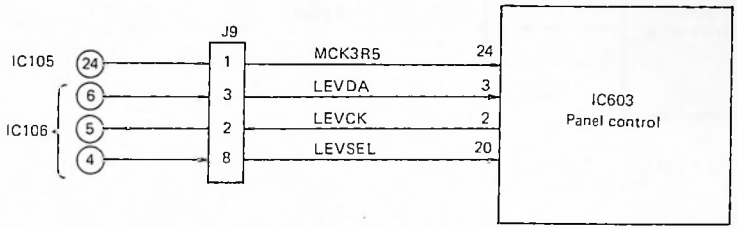


Figure 6-2-1 Connection with the Signal Processing Circuit

(1) MCK3R5 is 3.528 MHz clock.

(2) LEVDA is the 15 bits serial signal for the signal level data.

(3) LEVCK is the shift clock for the signal level data.

(4) LEVSEL is the read enable signal for the level signal.

(5) Input data for the level meter can be read as serial data from LEVDA as soon as 31 clock pulses from LEVCK are output from the leading edge of LEVSEL. LEVSEL must always be high when LEVCK is made low.

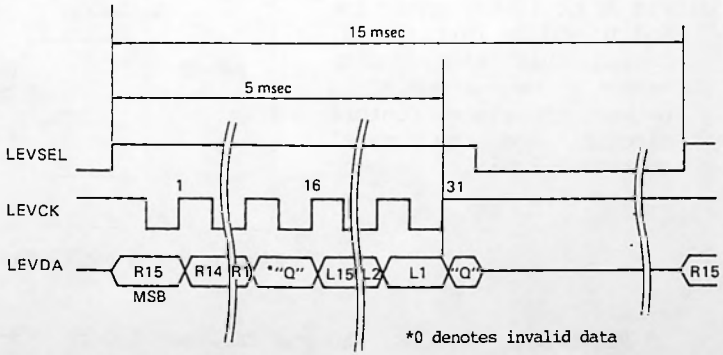


Figure 6-2-2 Input Data Timing Chart

2) System Control Circuit

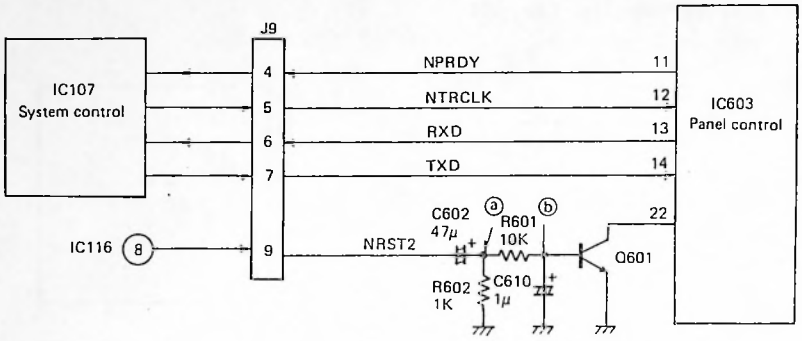


Figure 6-2-3 Connection with the System Control Circuit

(1) NRST2 is the system reset signal. When the power is turned on, a high signal is input from pin 8 of IC-116.

(2) C602 and R602 comprise a differentiator. A spike is generated at point (a), C610 changes and approximately 1 ms later a high level signal is generated at point (b) which turns on Q601.

(3) Pin 22 of IC-603 goes low and IC-603 is initialized. During this time, data cannot be transferred between the system contorl circuit and the panel control circuit.

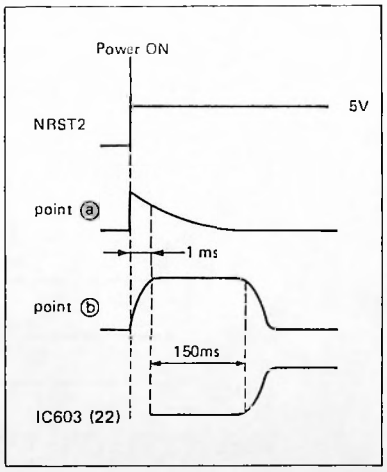


Figure 6-2-4 NRST2 Timing Chart

* For NPROY, NTRCLK, RXD and TXD, see figure 7-3-3 panel control.

3) Key Input Circuit

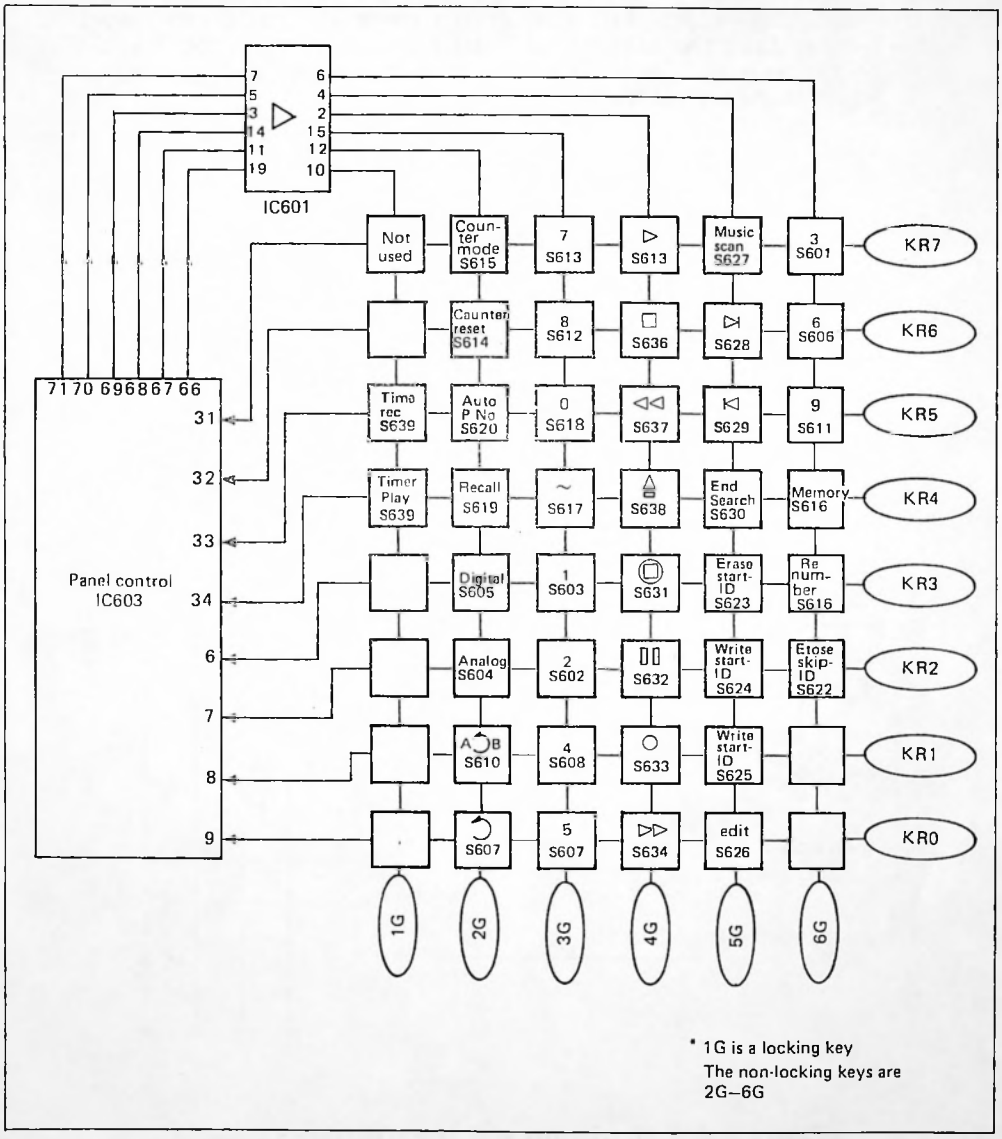


Figure 6-2-5 Key Matrix Assignment

(1) Pins 66 through 71 of IC-603 are sacn signals (and grid signals for the FL display tube) and are inverted by IC-601.

(2) Pin 6 through 9 and 31 through 34 of IC-603 are input terminals for the key scan data.

4) FL Display and LED Indicators

The FL displays and LED indicators are activated according to display data from the system control circuit and level data from the signal processing circuit. They are divided into mode and level displays. The display refersh timing is performed as follows:

* The FL and LED refreshed each time one block of display data from the system control circuit is received.

* Level meter data refreshes the level meter display on the FL during the next display period after both the left and right are sampled (every 15 ms)

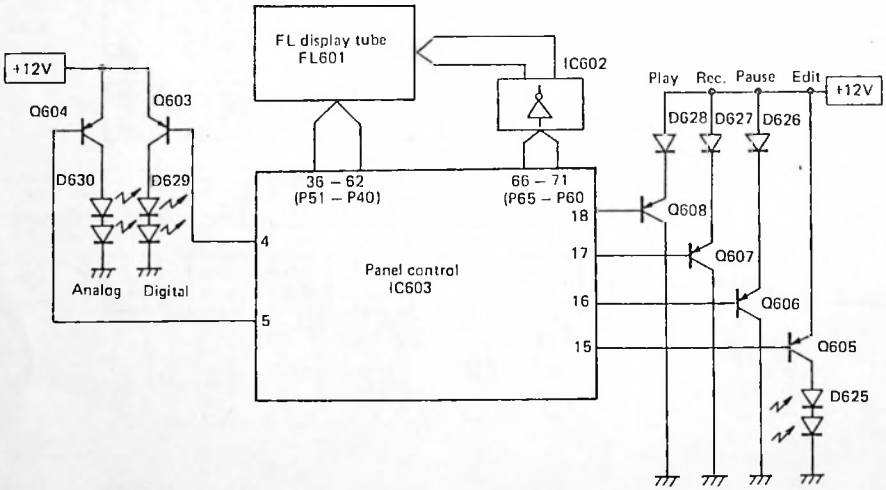


Figure 6-2-6 FL Display and LED Indicators

(1) FL display

(a) Pins 66 through 71 of IC-603 are grid scan signals which are inverted by IC-602 and sent to the grids of FL601.

(b) Pins 36 through 62 of IC-603 are output as segment data. The grids and segments are shows below.

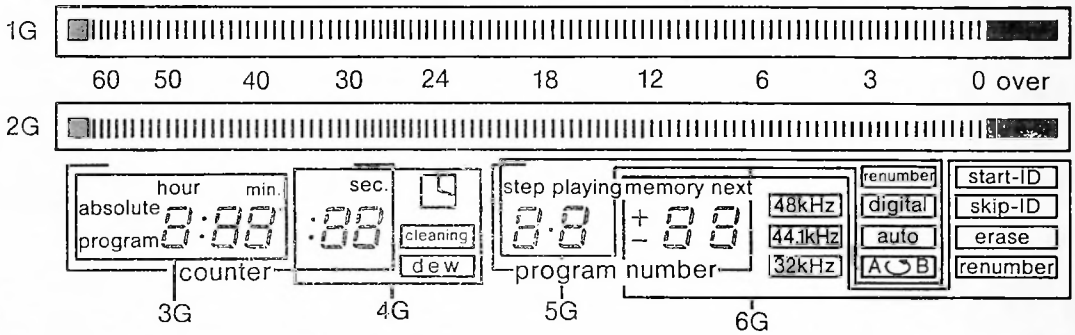


Figure 6-2-7 FL Display Tube Grid Assignment

IC603 grid signal output	IC603 segment signal output																										
	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64
	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q	r	s	t	u	v	w	x	y	z
②									Left level meter																	
1G	LOW																									HIGH
③									Right level meter																	
2G	LOW																									HIGH
④	Pro-gram	abso-lute					time												hour							
3G				a	b	f	g	c	e	d		a	b	f	g	c	e	d	min	a	b	f	g	c	e	d
⑤																										
4G												a	b	f	g	c	e	d	sec	a	b	f	g	c	e	d
⑥					ana log	digi tal	auto												play-ing							
5G								A		B		a	b	f	g	c	e	d		a	b	f	g	c	e	d
⑦	—	+		start -1D	skip -1D	48Hz	cra'l	44Hz	re-num ber	32k Hz	mem-ory								next							
6G												a	b	f	g	c	e	d		a	b	f	g	c	e	d

* a, b, c, ... g: Segments of the 7-segment display

Table 6-2-1 FL Display Tube Illumination

(2) LED indicator

Low outputs at pins 4, 5, 15, through 18 of IC-603 corresponding to pressed front panel keys turn on the transistors and illuminate the LEDs.

(3) Level meter

The level meter used in this player features the peak hold function described below.

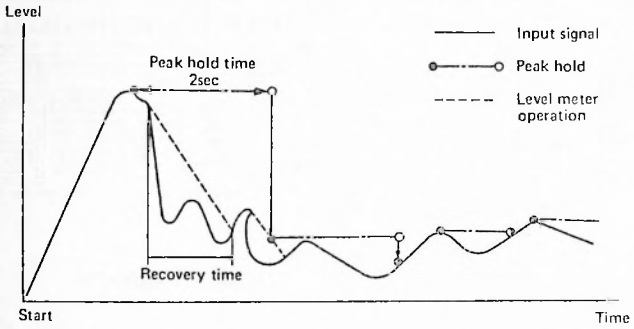


Figure 6-2-8 Level Meter Display

(a) An input signal like that shows in figure 6-2-6 is sent from the signal precessing circuit every 15 ms. (The maximum value during the 15 ms is held by the signal processing circuit).

(b) Operation of the level meter consists of lighting the segments according to the input signal from the starting point. The peak value is held on the display for approximately 2 s. This level is memorized by panel control IC-603.

(c) The input signal also varies during the peak hold display. Level display is performed according to the real time signal level. However, if a large signal suddenly changes to a small signal, the indication on the level meter decreases by one segment every 45 ms (recovery time).

6-3. Test Program Function

This function is provided to self-test the panel control circuit in two ways: "display" and "all display".
The test procedure and operation are described below.

1) Procedure

Test points TP601 to TP603 are used. Short circuiting TP601 to TP603 or TP601 to TP603 activates the "display" or "all display" function.
Be sure the power is off before short circuiting the test points and then turn on the power again after the points are short circuited.

2) Operation

(1) Display (short circuiting TP601 to TP603)
The display sequence is shows on the right.

Table 6-3-1 Test Program Display Sequence

Sequence	Operation	Remark
1	A segment from a to z of 1G (left channel level meter) is lit every 0.2 s. When completely lit they are all turned off after 0.2 s.	See Table 6-2-1 and Fig. 6-2-7.
2	2G (right channel level meter) is completely lit for 0.2 s.	
3	3G is completely lit (0.2 s) and turned off.	
4	4G is completely lit (0.2 s) and turned off.	
5	5G is completely lit (0.2 s) and turned off.	
6	6G is completely lit (0.2 s) and turned off.	

7	LEDs are lit (0.2 s) in sequence and then turned off. (1) digital (D629) (2) analog (D630) (3) edit (D631) (4) rec (D626) (5) pause (D627) (6) play (D628)	
End	1G and 2G turn off. 3G to 6G light as shown in Fig. 6-3-1. Analog LED (D630) lights.	See Fig. 6-3-1.

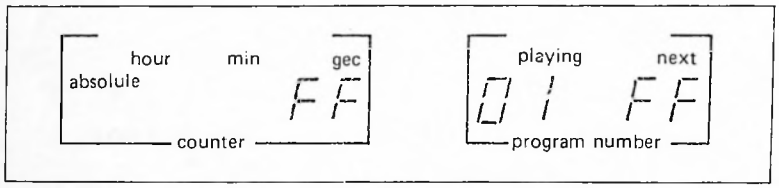


Figure 6-3-1 Final Display of Test Program

When an operating key is pressed while figure 6-3-1 is displayed, its key code is displayed in the sec numeric display for the counter. The key codes are shows table 6-3-2.

Operating key (Operating switch)	Key code	Operating key (Operating switch)	Key code	Operating key (Operating switch)	Key code	Operating key (Operating switch)	Key code
3 (S601)	07	9 (S611)	05	re number (S621)	03	(S631)	23
2 (S602)	32	8 (S612)	36	erase skip-ID (S622)	02	(S631)	22
1 (S603)	33	7 (S613)	37	erase start-ID (S623)	13	(S633)	21
analog (S604)	42	counter reset (S614)	46	write skip-ID (S624)	12	(S634)	20
digital (S605)	43	counter mode (S615)	47	write start-ID (S625)	11	(S635)	27
6 (S606)	06	memory (S616)	04	edit (S626)	10	(S636)	26
5 (S607)	30	(S617)	34	music scan (S627)	17	(S637)	25
4 (S608)	31	0 (S618)	35	(S628)	16	(S638)	24
(S609)	40	recall (S619)	44	(S629)	15	* Timer	11
A B (S610)	41	auto P No (S620)	45	end search (S630)	14	(S639)	21

Table 6-3-2 Test Program Key Codes

* When the timer switch (S639) is set to PLAY or REC, the key code is displayed in the playing number display for the program number.

(2) All display mode (short circuiting TP601 to TP603)

When the power is turned on, all FL displays and LED indicators (6 LEDs) light. Key codes are not displayed even if operating keys are pressed.

7. System Control Circuit

7-1 General

7-2 Mechanism Control Circuit

1) Tape Being/End Detection Circuit
2) Cassette Tape Information Detection Circuit
3) Mechanism Mode Detection Circuit
4) Motor Drive Circuit (for cassette loading and mechanism mode)
5) Power off Unload Circuit

7-3 Signal Flow in the System Control Circuit and Peripheral Circuits

1) Signal Processing Circuit
2) Servo Circuit
3) Panel Control Circuit
4) Analog Circuit (RF section, audio section)

7-4 Other Circuits

1) Dew Sensor and Heater
2) Reset Signal Generation Circuit
3) 130KMAD Control Circuit

7-1 General

The system control circuit and mechanism control circuit are both located on the digital board. As shows in figure 7-1-1, these circuits are connected to the peripheral circuits via cables.

This chaptor deals mainly with the system control circuit and mechanism control circuit and describes their signal and data transfer with the peripheral circuits.

The system control circuit contains the main CPU IC-701 which operates according to a program stored within IC-701.

The mechanism control circuit also uses IC-701 to control the operation of the mechanism.

IC-107 is a dual CPU chip containing one CPU for mechanism control and another for system control. Furthermore, since the RAM and I/O ports are used in common, a number of operation can be executed simultaneously.

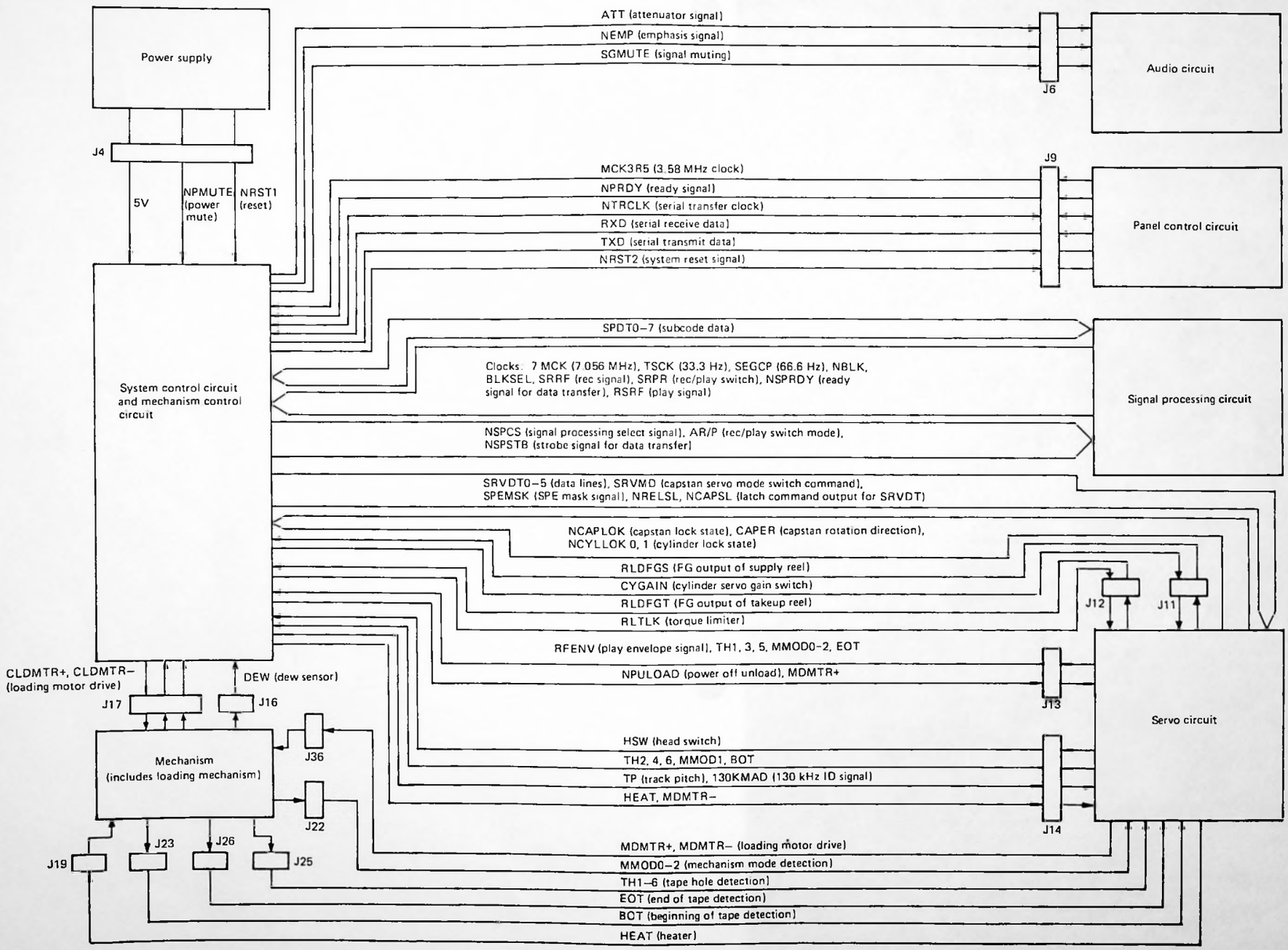


Figure 7-1-1 Connection Between the System Control Block and Other Blocks

7-2 Mechanism Control Circuit

1) Tape Being/End Detection Circuit

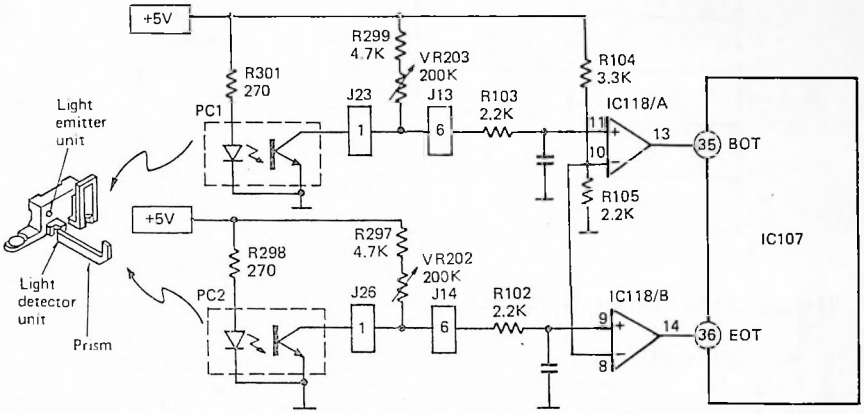


Figure 7-2-1 Tape Begin/End Detection Circuit

(1) PC1 detects the begining of the tape and PC2 detects the end of the tape.

(2) The leader tape at the begining of the tape is transparent and passes light which turns on the phototransistor on the light detector side. At this time, PC2 is located at a magnetic (opaque) portion of the tape where light does not pass and the phototransistor is off.

(3) At the start of tape takeup, this state passes comparators A and B of IC-118 in the form of tape being/end detection signals which are input by pins 35 and 36 of IC-107.

(4) Based on this input information, IC-107 stops the mechanism.

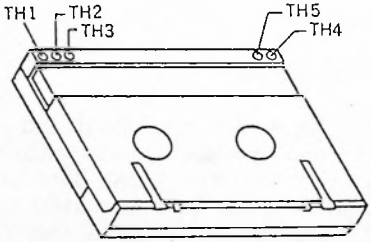
(5) VR202 and VR203 are used to adjust the sensitivity of the photocouplers since there are variations in the transmittances of the leader tape and prism.

Table 7-2-1 Tapw Begin/End Mode

IC107 Input Port		Mode
(35) BOT	(36) EOT	
L	H	Beginning of tape
H	H	Middle of tape
H	L	End of tape
L	L	Cut tape

2) Cassette Tape Information Detection Circuit

The cassette contains five holes as shows in the figure 7-2-2, which convey information on the tape (presence/absence of tape, presence/absence of erasure prevention tab, music tape or ordinary tape, metarial and thickness).



TH1, TH2, TH3 : For tape material and thickness detection
TH4 : For ordinary tape and music tape detection
TH5 : For erasure prevention tab detection

Figure 7-2-2 Hole Positions on Cassette

Switching and Hole Positions

S1 → TH1
S2 → TH2 Hole present : Switch off
S3 → TH3
S4 → TH4 Hole absent : Switch on
S5 → TH5
S6 → - (Turns on after the cassette is inserted and loading is completed).

(1) The cassette tape information detection circuit detects the tape mode according to the on or off states of mechanical switches S1 through S6 which correspond to cassette holes TH1 through TH5 and the presence or absence of the cassette.

(2) The detected information is input by pins 10 through 17 of IC-107.

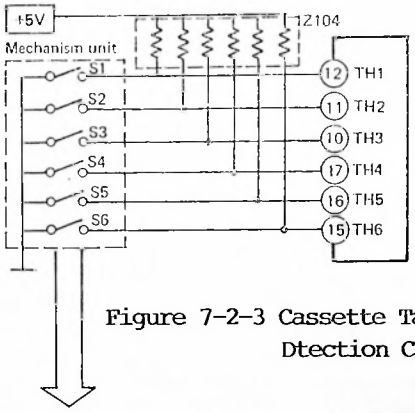


Figure 7-2-3 Cassette Tape Information Dtection Circuit

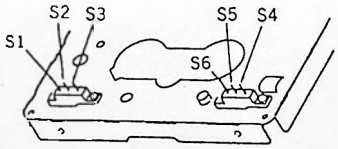


Figure 7-2-4 Detection Switch Mechanism Position

Table 7-2-2 Tape Material and Thickness

Hole present: High (switch off)
Hole absent: Low (switch on)

IC107 Input Port			Tape Material and Thickness Mode
(12) TH1	(11) TH2	(10) TH3	
L	L	L	13 μm thick metal tape for 2H
L	H	L	Thin metal tape for 2H or higher
L	L	H	1.5 wide track pitch, 13 μm thick
L	H	H	1.5 wide track pitch, thin
H	L	L	Not used

Table 7-2-3 Cassette Tape Mode

IC107 Input	Application	Cassette Tape Mode	
		L	H
(17) TH4	Tape type	Ordinary tape	Music tape
(16) TH5	Erasure prevention	Record enabled	Record inhibited
(15) TH6	Cassette detection	Cassette present	Cassette absent

3) Mechanism Mode Detection Circuit

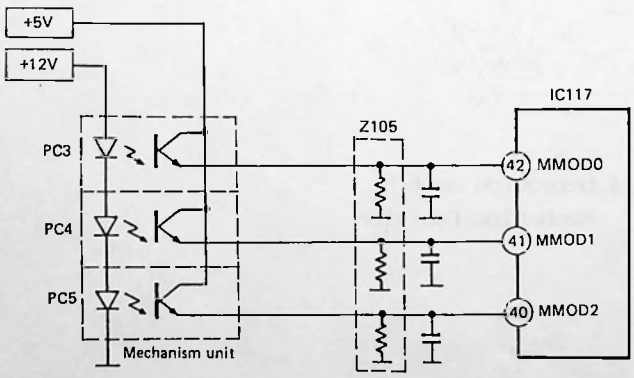


Figure 7-2-5 Mechanism Mode Detection Circuit

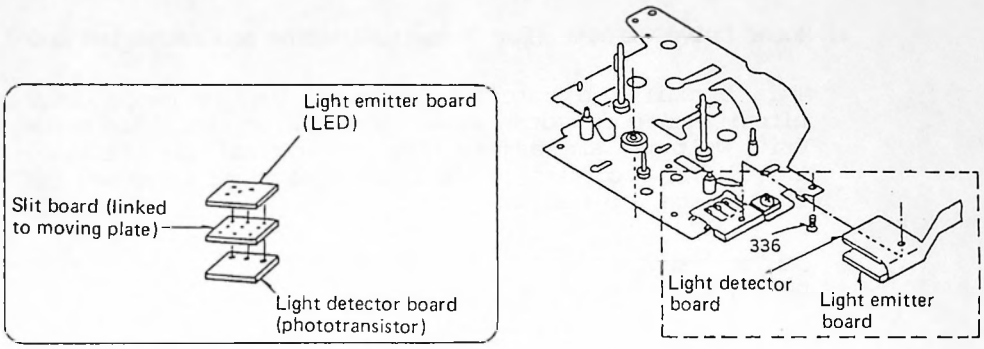


Figure 7-2-6 Arrangement of PC3 to PC5

Table 7-2-4 Mechanism Modes

IC117 Input			Mechanism Mode
(42) MOD0	(41) MOD1	(40) MOD2	
H	H	H	When the cassette is loaded in the mechanism (Stop 3)
H	L	H	Slack stop (Stop 2)
H	H	L	Unload stop (Stop 1)
L	L	H	FF.REW
L	H	L	Pause
L	H	H	PLAY
L	L	L	Intermediate

(1) For the mechanism to proceed to the next mode, the state of the current mode is sent to IC-117 in the from of a 3 bits data.

(2) The state of the mechanism mode is represented by a combination of photocoupers PC3 through PC5 at the detection circuit, the output of which are input by pins 42 (MMOD0), 41 (MMOD1) and 40 (MMOD2) of IC-117.

4) Motor Drive Circuit (for cassette loading and mechanism mode)

This circuit integrates a cassette loading motor drive circuit and mode motor drive circuit. However, the motor drive voltages are adjusted by an external circuit since they differ according to the cassette loading speed and the load on the drive mechanism.

During cassette loading= 6 volt
During mode motor operation= 4 volt

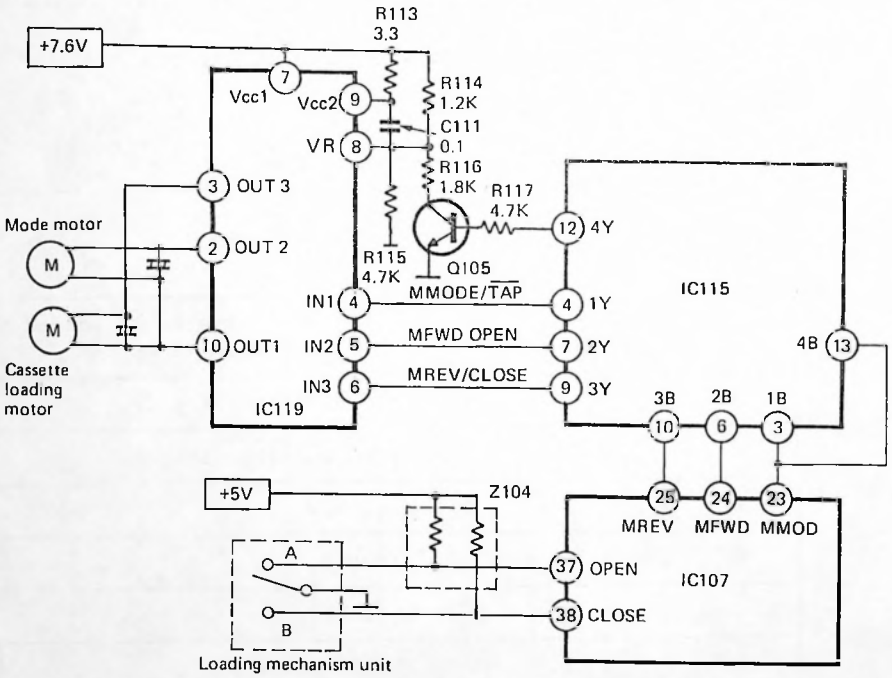


Figure 7-2-7 Motor Drive Circuit

Motor Drive Voltage Switching

(1) The command from pin 12 of IC-115 switches Q105 on and off.

(2) The on or off state of Q105 connects or disconnects voltage dividing R116 which is connected to R115. This is used to switch the voltage applied to pin 8 of IC-119.

(3) The supplies from pins 7, 8, and 9 of IC-119 comprise the motor power supply.

Table 7-2-5 Motor Drive Voltage Switching Mode

I/O \ Mode		During Cassette Loading Motor Drive	During Mode Motor Drive
IC115	(13)	L	H
	(12)	L	H
Q105		OFF	ON
IC119	(8)	H	L

Motor Drive Circuit (refer to figure 7-2-7)

Command signals issued as result of pressing a panel key are sent to IC-107 from the panel control microcomputer. Commands from pins 23, 24, and 25 of IC-107 are sent to IC-115 and then to IC-119 which drives the cassette loading motor and mode motor.

The motor drive modes are shows in table 7-2-6 below.

Table 7-2-6 Motor Drive Modes

Drive System	IC107 Output			IC115 Output			IC119 Output			Drive Mode	Operation
	(23) MMOD	(24) MFWD	(25) MREV	(4) 1Y	(7) 2Y	(9) 3Y	(10) OUT1	(2) OUT2	(3) OUT3		
Cassette Loading Motor Drive	L	H	L	L	H	L	H	OPEN	L	Pin 10 to 3, forward rotation	Tray open
	L	H	H	L	H	H	L	OPEN	H	Pin 3 to 10, reverse rotation	Tray close
	L	L	Unde-fined	L	L	Unde-fined	L	L	L	Motor stop	
Mode Motor Drive	H	L	L	H	L	L	H	L	OPEN	Pin 10 to 2, forward rotation	Tape load
	H	L	H	H	L	H	L	H	OPEN	Pin 2 to 10, reverse rotation	Tape load
	H	H	Unde-fined	H	H	Unde-fined	L	L	L	Motor stop	

After the cassette loading motor has been activated, the detection switches (leaf switches) linked to the top of the cam gear in the cassette loading mechanism detect the open or closed state of the tray and send the stop command for the cassette loading motor to pins 37 and 38 of IC-107. After this, the output signals from IC-107, IC-115, and IC-119 are as shows in table 7-2-6.

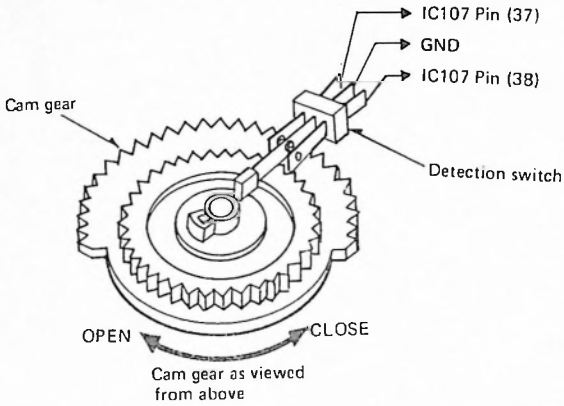


Figure 7-2-8 Tray Detection Switch Positions
(Shows at intermediate position)

Table 7-2-7 Tray States

Tray State	Detection Switch		IC107		Motor
	(A)	(B)	(37) OPEN	(38) CLOSE	State of Rotation
When open	OFF	ON	H	L	Stopped
During movement	OFF	OFF	H	H	Rotating
When closed	ON	OFF	L	H	Stopped

5) Power off Unload Circuit

This circuit unconditionally unloads the cassette to protect the tape and cylinder when the power is turned off with the cassette loaded.

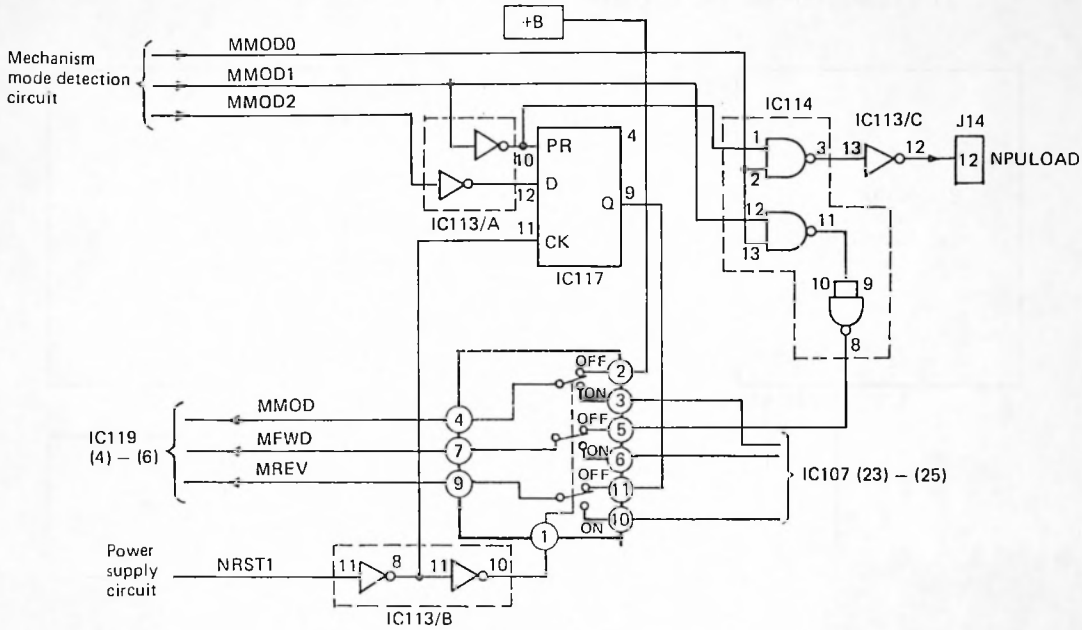


Figure 7-2-9 Power off Unload Circuit

(1) When the power is turned off, NRST1 and NPMUTE of the power supply section change from high to low.

(2) The switches within IC-115 switch from on to off. This switches the mode motor drive commands to those from the +B line, pin 9 of IC-117 and pin 8 of IC-114.

(3) The commands for the predetermined mode transition operation, from the current mode to the completion of the unloading operation, are sent from the mechanism mode detection circuit to mode motor drive IC-119 via IC-115. (refer to the mode drive modes in table 7-2-6).

(4) The signals from pin 12 of IC-113(C), which is sent to the capstan motor in the servo circuit, is the capstan motor rotation direction command used to take up the tape when the cassette is being unloaded.

7-3 Signal Flow in the System Control Circuit and Peripheral Circuits

This section describes the flow and processing of signal with the peripheral circuits shows in figure 7-1-1.

1) Signal Processing Circuit

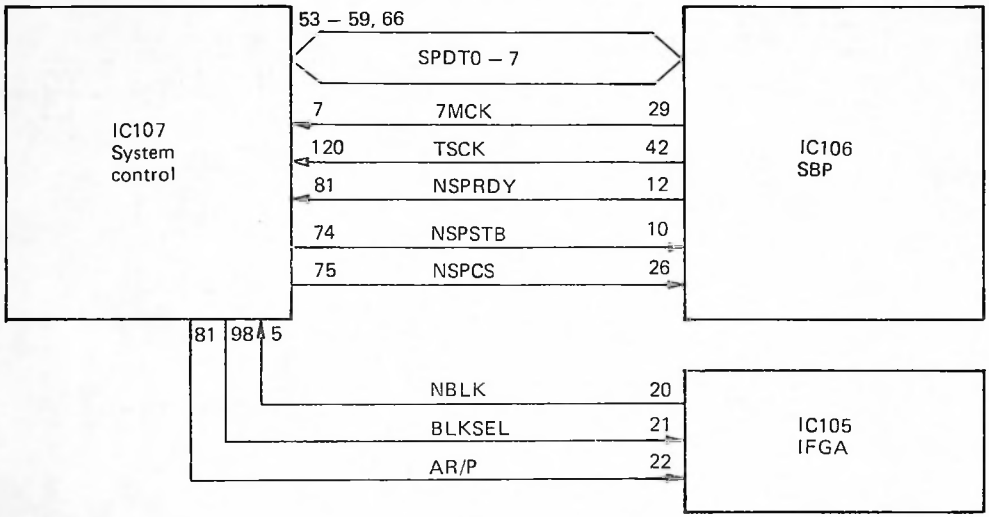


Figure 7-3-1 Connection with the Signal Processing Section

(1) The following types of data are transferred through the data bus (SPDT0 through SPDT7):

System Control to Signal Processing

(a) Subcode ID data (data which is to be written in the subcode area such as absolute time, program time, program number, etc).

(b) PCM ID data (ID data written in the PCM area such as preemphasis on/off, sampling frequency, number of channels, number of quantization bits, track pitch, copy inhibit code, etc.)

(c) Operating mode (PLAY,FF,etc)

(d) Muting command for digital signals

(e) Digital input and Analog input

Signal Processing to System Control

(a) Subcode ID data

(b) PCM ID data

(c) Copy inhibit information

(2) NSPRDY, NSPSTB and NSPCS for handshaking when transferring data using SPDT0 through STDT7, represent; ready (ready to receive), strobe (ready to transmit), and interrupt request, respectively.

(3) The SBP transfer uses parallel transfers with the sequence and timing shows in figure 7-3-3.

(a) Write (system control to SBP)
Two bytes representing the mode code are sent to inform the SBP of the system control's current mode (PLAY,FF,etc).

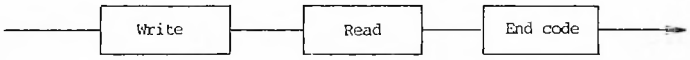


Figure 7-3-2 Basic SBP Transfer Sequence

(b) Read (SBP to system control)
The number of bytes that are sent is 3, 8, or 26 bytes, and this varies depending on the system control's operating mode.

(c) End code (system control to SBP)
One byte is sent as a code which informs the SBP that transfer has completed.

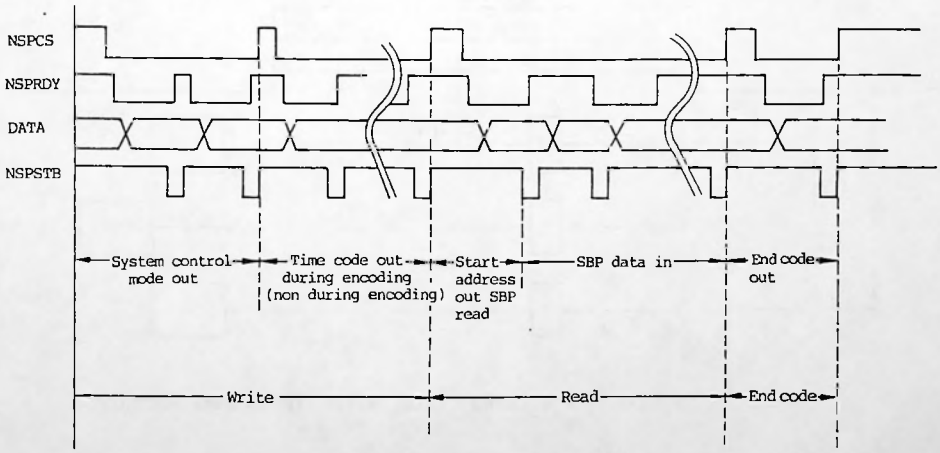


Figure 7-3-3 SBP Data Transfer Timing Chart

(4) Other signals are given below.

7MCK : Clock for IC-117 (7.056 MHz)

TSCK : 33.3 Hz used for timing control of signal transfers.

NBLK : This signal, used to detect program intervals of the record input signal, goes low when a signal which is lower than the prescribed level continues for longer than the prescribed duration.

BLKSEL : Command which determines the decision level for a location, whether it is in the middle of a program or between programs. High: -60 dB, Low: -50 dB.

AR/P : REC/PLAY mode switching signal for the analog circuit. High: PLAY, Low: REC.

2) Servo Circuit

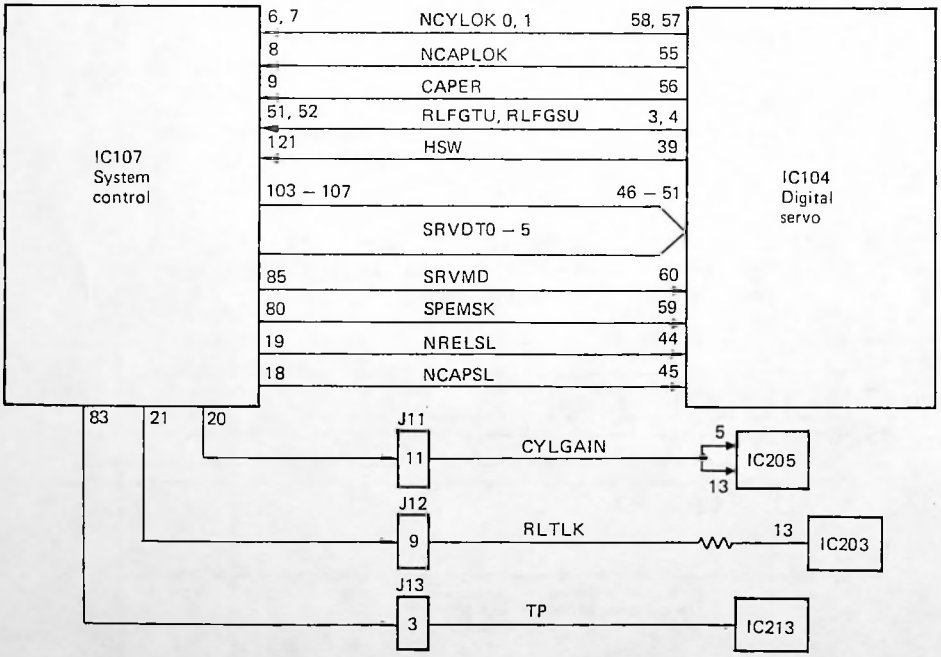


Figure 7-3-4 Connection with the Servo Section

(1) FG signals (from the MR devices attached to the reels) are sent from the reels (TU: takeup, SU: supply). For every rotation of reel, 40 FG pulses are output. These FG pulses are used for the following purposes:

(a) Tape counter signal input (counter counts 1 for every 8 pluses from the takeup reel).

(b) Tape protection during reel lock (mechanism operation cancel when the takeup reel stops)

(c) Tape control (decelerates at the end of take winding when accelerating or decelerating at 50 to 200 times standard speed).

(d) Tape length detection (60 minute tape, 90 minute tape etc) The diameter ratio of tape would on the reel is calculated during FF and REW. This is necessary to control the output timing for (c) above.

(e) Position detection during search operation.

(2) NCYLLOKO-1 are data which represent the cylinder lock atate. The system control circuit receives these signals and uses them to check that the cylinder motor is rotating at the specified speed. (Transfer timing switching porcessing of the speed command data).

(3) NCAPLOCK is a signal which represents the capstan lock state. The system control circuit receives this signal and uses it to check that the capstan motor is rotating at the specified speed. (Transfer timing switching processing of the speed command data).

(4) CAPER represents the actual rotation direction of the capstan motor. Actually, the rotation direction of the reel, which is belt driven by the capstan motor, is detected. CAPER is then used to determine whether the tape counter is to be incremented or decremented.

(5) HSW, and A/B head switching signal, is used in the system control circuit to control the timing during data transfers. (reference time for time counting of long periods such as still unload, auto rec mute, subcodes ID frame control, etc).

(6) SRVDT0 through SRVDT5 are data lines which determine the rotation speed of the capstan and cylinder. An example (for atandard speed) of their outputs is shows table 7-3-1.

Table 7-3-1 SRVDT Mode During Standard Speed

IC107 pin No.	Output	Remark
(108) SRVDT 0	(L)	Standard speed (1x)
(107) SRVDT 1	(L)	
(106) SRVDT 2	(H)	
(105) SRVDT 3	(H)	
(104) SRVDT 4	(L)	Cylinder rotation command Low: rotation High: stop
(103) SRVDT 5	(H)	Capstan rotation command High: forward Low: reverse

(7) SRVMD is a capstan servo mode switching command. It is low when synchronized with ATF (during PLAY) and high when not synchronized with ATF (REC, FF, etc).

(8) NCAPSL and NRELSL are latch command signals for SRVDT. The output states for SRVDT are as shows in table 7-3-1 when latched with NCAPSL. NRELSL latches SRVDT0 through SRVDT5 and consists of a 6 bits data which represents the rotation speed of the reel during FF and REW.

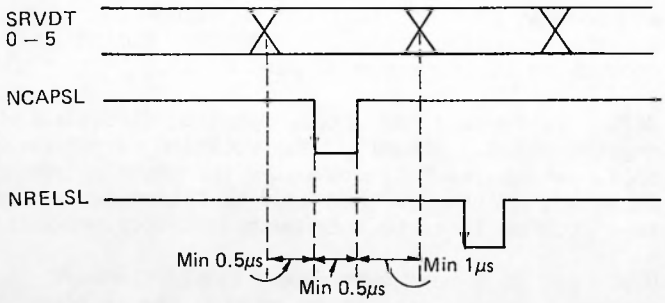


Figure 7-3-5 Timing Chart for NCAPSL and NRELSL

(9) SPEMSK is a signal which, makes SPE in order to quicken the drop of the ATF. The output conditions are:

(a) Activation of the PLAY mode.
(b) RFENV signal turns on during operation of the PLAY mode.
(c) Activation of the REC mode.

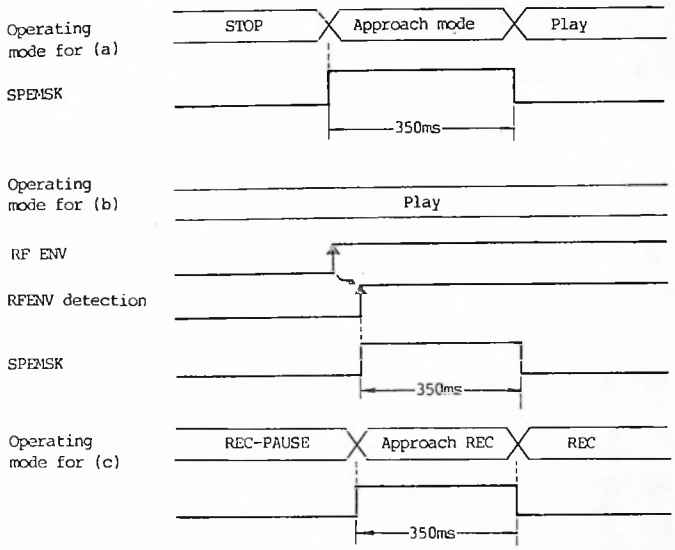


Figure 7-3-6 SPEMSK Output Timing

(10) CYLGAIN is a gain switching signal for the cylinder servo. When low, the gain is reduced.

(11) RLTLK is a torque switching signal for the reel servo. High ... Standard, Low ... down.

(12) TP is a switching signal for track pitch.
High ... normal (13.6 μm)
Low .... 1.5 TP (20.4 μm)

3) Panel Control Circuit

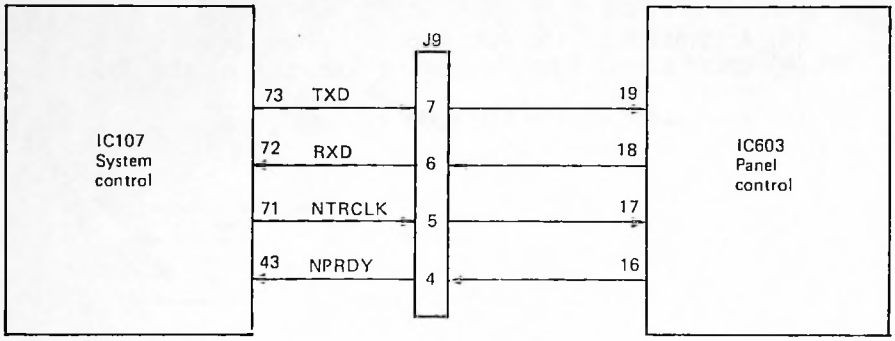


Figure 7-3-7 Connection with the Panel Control Section

(1) Data transfers with the panel control circuit are performed is serial using the TXD and RXD lines. The following types of data are transferred:

System Control to Panel Control

(a) Data which is to be displayed on the LEDs (PLAY, REC, PAUSE, etc).
(b) Data which is to be displayed on the FL display tubes.

Panel Control to System Control

(a) Operating key input signal
(b) Remote control information
NTRCLK is a serial transfer clock (110.25 KHz)

(2) NPRDY is a ready signal for data transfers from panel control to system control.

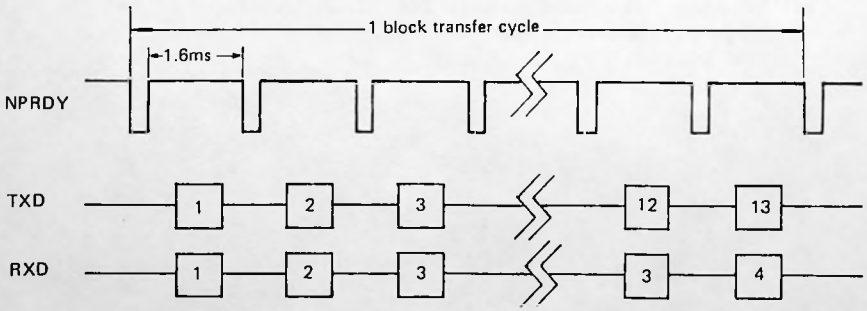


Figure 7-3-8 Timing Chart for NPRDY

4) Analog Circuit (RF section,audio section)

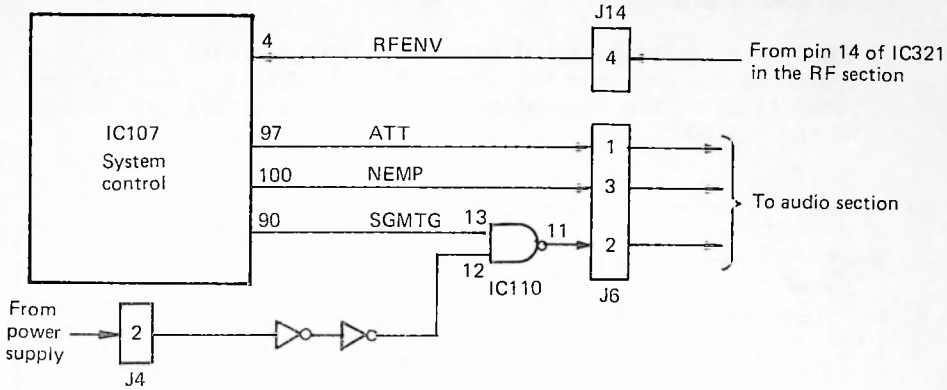


Figure 7-3-9 Connection with the Analog Section

(1) RFENV detects the envelope of the RF output signal.
High ..... Envelope present
Low ..... Envelope absent

(2) ATT is a signal used to lower the gain of the LINE output during CUE or REV.
High ..... Normal
Low ..... -10 dB attenuation

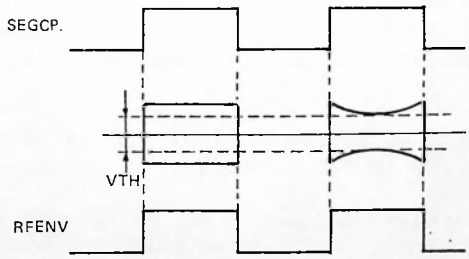


Figure 7-3-10 Timing Chart for RFENV

(3) NEMP is a signal used to apply deemphasis during PLAY depending on the presence or absence of preemphasis in the PCM ID area, which is recorded on the tape.
High ..... Deemphasis off
Low ..... Deemphasis on

(4) SGMTG, a signal muting command, is high in any mode other than PLAY, REC, PAUSE and STOP and mutes the LINE output.
High ..... Muting on
Low ..... Muting off

7-4 Other Circuits

1) Dew Sensor and Heater

This circuit is designed to supply current to the heater to evaporate any dew when it forms. This is done to prevent the possibility of the tape sticking to the head when there is dew on the cylinder.

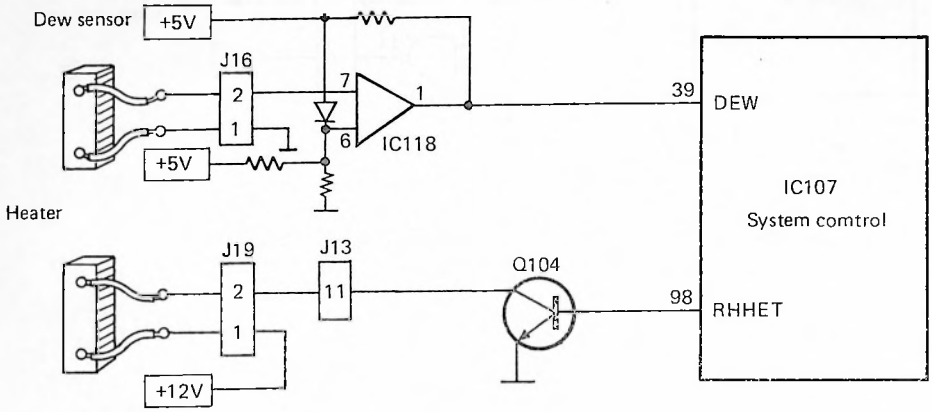


Figure 7-4-1 Connection of the Dew Sensor and Heater

(1) The dew sensor is located near the cylinder. When numidity rises, its resistance increases and the voltage at pin 7 of IC-118 increases so that pin 1 goes high.

When pin 39 of IC-107 is high, duw is detected. And when low, duw is not detected.

(2) This is received and pin 98 of IC-107 goes high. Q104 turns on and current is supplied to the heater to evaporate the dew.

When pin 98 of IC-107 is high, the heater is on. And when low, the heater is off.

(3) IC-107 issues a command to the mechanism control and servo sections to unconditionally set the stop mode (tape unload, cylinder rotation). At this time, the dew indicator flashed and all operations (except for open and close) are ignored.

2) Reset Signal Generation Circuit

This circuit generates a reset signal for the various circuits.

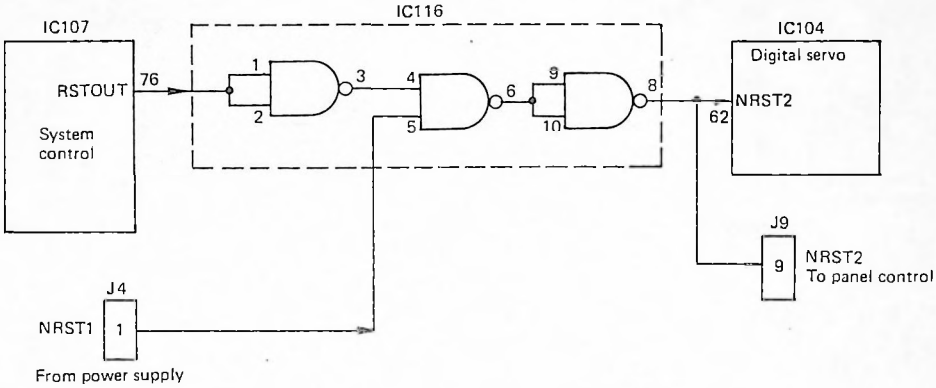


Figure 7-4-2 Reset Signal Generation Circuit

(1) The signals at various points are as shows in figure 7-4-3.

(2) NRST2 is a reset signal generated by IC-116 and supplied to the digital servo (IC-104 and panel control circuit to reset the respective CPUs.

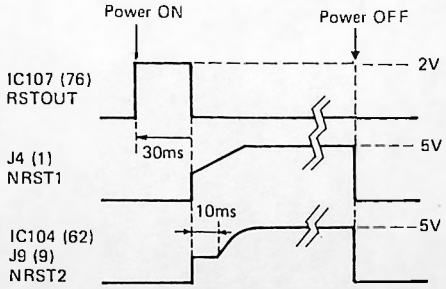


Figure 7-4-3 Timing Chart for Reset Signal

3) 130KMAD Control Circuit

This circuit outputs the 130KMAD signal only during normal recording since the subcode area may be affected when the 130KMAD signal goes high during post-recording.

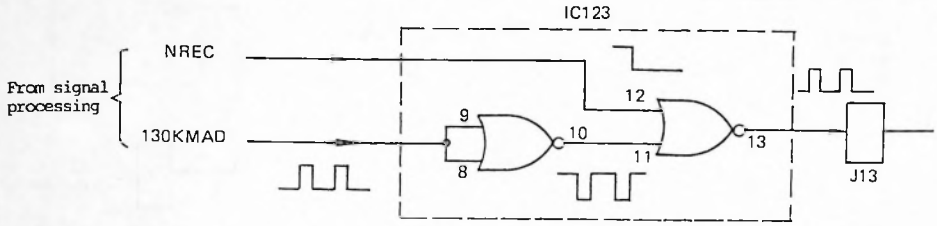


Figure 7-4-4 130KMAD Contorl Circuit

(1) 130KMAD, which is sent from the signal processing section, enters pins 8 and 9 of IC-123 and becomes an inverted signal when it is output from pin 10.

(2) NREC is a low output only during normal recording, otherwise it is high.

(3) The signal at pin 11 of IC-123 is inverted and output from pin 13 of IC-123 when pin 12 is low. Pin 13 goes low when pin 12 is high.

8. SERVO

8-1 General Description

1) Capstan Servo
2) Cylinder Servo
3) Reel Servo

8-2 Block Diagram

8-3 FG Signal Shaping Circuit

1) Capstan FG
2) Cylinder FG and PG
3) Reel FG

8-4 Capstan Servo

1) Capstan Servo in REC Mode
2) Capstan Servo in PLAY Mode

8-5 Integrating and Low-Frequency Compensation Circuits

1) Integrating Circuit
2) Low-Frequency Compensation Circuit

8-6 ATF Servo

1) Operation
2) Circuit Description (Based on Block Diagram)
3) Sampling Pulse Timing
4) Pilot Signal Peak and Differential Pilot Voltage Detectors
5) ATF Operation During Non-Recording Blank Playback

8-7 Cylinder Servo

1) Cylinder Servo in REC/PLAY Mode
2) Cylinder Servo in FF/REW Mode
3) Cylinder Servo Gain Switching Circuit

8-8 Reel Servo

8-9 Power-Off Unload Circuit and the Unload Circuit

1) Power-off Unload Circuit
2) Unload Circuit

8-10 Triangular Wave Generator

8-11 Servo Block Pin Names and Symbols

8-1 General Description

The servo system comprises the following three servo blocks:

1) Capstan servo

2) Cylinder servo

3) Reel servo

These servo blocks use different servo techniques to control their control objectives:

1) Capstan Servo

The capstan servo circuit uses different servo system for REC and PLAY modes:

(a) REC mode
In this mode the circuit provides system and phase servo control to requlate tape speed.

(b) PLAY mode
In this mode the circuit provides system and ATF servo control. The ATF servo controls tape speed (capstan motor speed) so that the play head always tracks the center of the main play track.

2) Cylinder Servo

The cylinder servo circuit provides system and phase servo control in both REC and PLAY modes to regulate the cylinder's rotation speed.

3) Reel Servo

To ensure the deck reads subcode information of the tape at high tape speeds, the reel servo circuit controls capstan motor rotation so that the relative speed of cylinder to the tape is requlated to a constant.

The reel servo yields a certain value (A) for a specified reel speed, computes the sum of reel rotation periods (e.g. "B" for takeup reel and "C" for supply reel), and controls the reel speeds so that A=B+C.

8-3 FG Signal Shaping Circuit

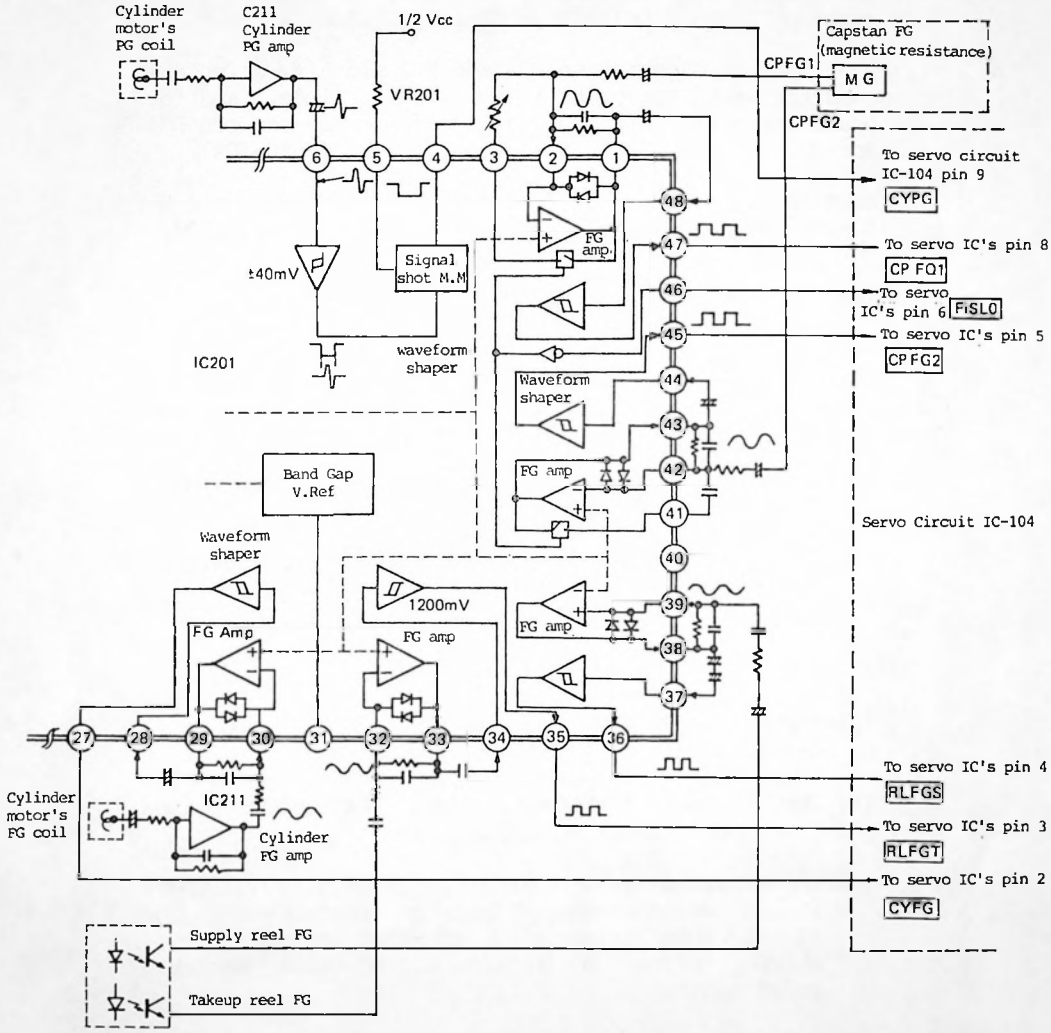


Figure 8-3-1

This circuit waveform-shapes the FG and PG (cylinder only) signals coming from the capstan motor, cylinder motor, and reel pases and transfers them to the servo controller, IC-104, that follows.

1) Capstan FG

(1) The magnetic resistance (MR) devices used in the capstan FG generate high-precision FG signal.

(2) The capstan FG generates FG1 and FG2 signals, which are used for speed servo utilizing signal periods, and for phase servo utilizing the phase difference between FG1 and FG2 (processed within the servo circuit IC-104).

(3) Each FG signal is waveform-shaped into a square wave by IC-201 and transferred to the servo controller IC-104.

2) Cylinder FG and PG

(1) FG

(a) The cylinder FG signal is generated by an FG coil provided on the cylinder motor.

(b) The FG amplifier IC-211 serves to eliminate noises from the cylinder FG signal.

(c) The signal is waveform-shaped into a square wave by IC-201 and transferred to the following servo controller IC-104.

(2) PG

(a) The cylinder PG signal is created by a PG coil provided on the cylinder motor.

(b) The PG amplifier IC-211 serves to eliminate noises from the cylinder PG signal.

(c) The PG signal is applied to pin 6 of IC-201, where it is waveform-shaped into a square wave. The signal then triggers a one-shot multivibrator, which produces a PG pulse signal with variable pulse width.

(d) VR201 at pin 5 of IC-201 is used to vary the pulse width of this PG pulse signal. It controls the relative head position to tape tracks by varying the PG pulse width.

3) Reel FG

(1) Reel FG signals are generated from photosensors (phototransistor/photodiode pairs) used for both the supply and takeup reels. A reflection plate is provided on the bottom side of each reel base.

8-4 Capstan Servo

The capstan servo circuit uses different servo system for REC and PLAY modes:
** REC mode .... Speed and phase servos
** PLAY mode ... Speed and ATF servo

1) Capstan Servo in REC Mode

In REC mode, the capstan servo circuit provides speed and phase control over the capstan to regulate tape speed to a constant (8.15 mm/sec).

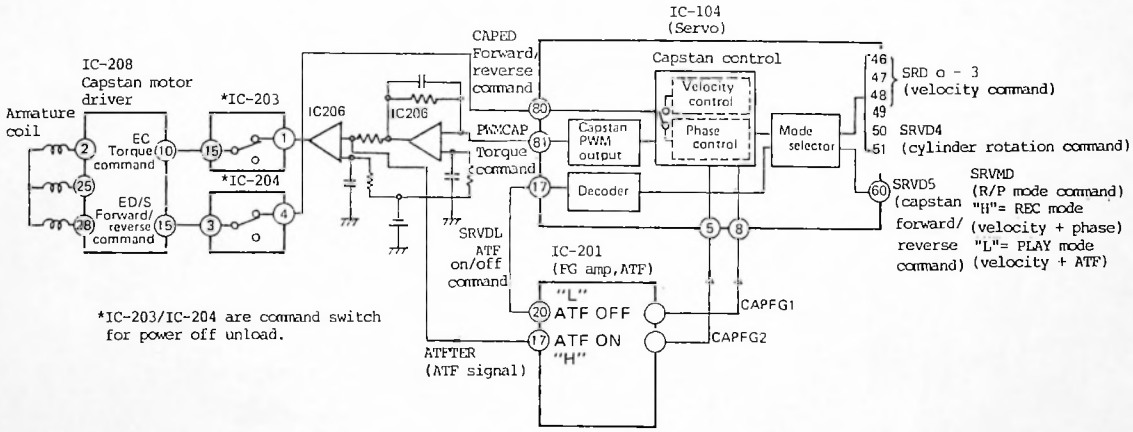


Figure 8-4-1

(1) Rotation Speed Command

(a) A rotation speed command is applied from the system controller IC-104. Table 8-4-1 shows an example of the command bit status (for x 1 speed):

Table 8-4-1

IC104's pin No.		Command bit status	Remarks
(46)	SRVDT 0	(L)	x 1 speed
(47)	SRVDT 1	(L)	
(48)	SRVDT 2	(H)	
(49)	SRVDT 3	(H)	
(50)	SRVDT 4	(L)	Cylinder rotation command: High=Stop; Low=Start
(51)	SRVDT 5	(H)	Capstan forward/reverse command: High=forward; Low=reverse

(b) The rotation speed command is then coupled to IC-104's internal speed control logic.

(c) At the same time, the Forward/Reverse command applied to IC-104's pin 51 appears at IC-104's pin 80, and couples to pin 11 of the capstan motor driver of IC-208 via IC-204.

(2) Speed/Phase control selection command

(a) In REC mode, pin 85 of the system controller IC-107 and pin 60 (SRVMD) of the servo controller IC-104 are both set to high, which places IC-104 in velocity/phase control mode.

(b) Pin 17 (SRVDL) of IC-104 is set to low and coupled to pin 20 of IC-201 to shut off the ATF output (Low = ATF output off, High = ATF output on).

(3) Torque command

A phase control signal subjected to speed PWM modulation appears at pin 81 of IC-104 and couples to IC-206 (integrating circuit), where it is converted into a DC level signal. This signal is then applied via IC-203 to pin 10 of the capstan motor drive IC-208, as a torque command. (The integrating circuit will be described in a later section).

2) Capstan Servo in PLAY Mode

In PLAY mode, the capstan servo controls capstan motor speed so that the play head always tracks the center of the current track on the tape being played.

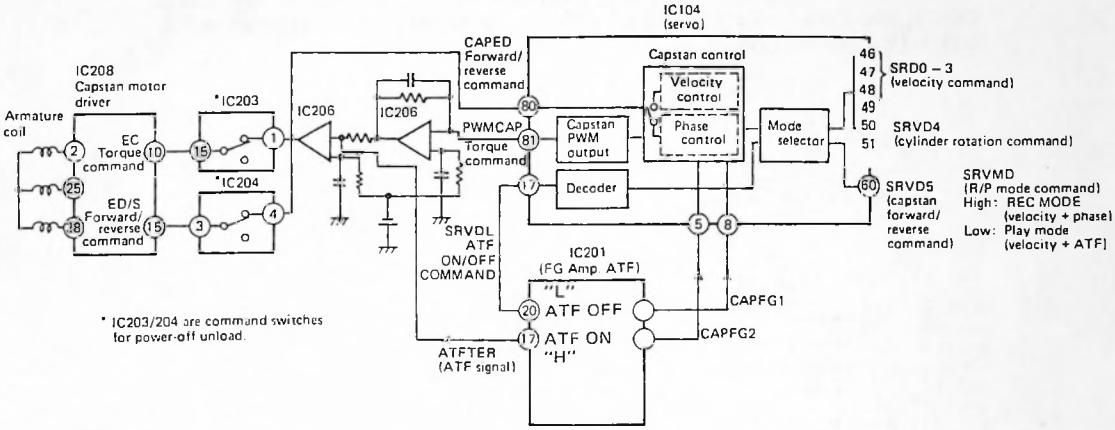


Figure 8-4-2

In PLAY mode, the capstan servo circuit provides velocity and ATF servo control. The velocity servo uses the capstan motor's FG signal for control, whereas the ATF servo uses the ATF signal for control. The capstan motor speed is controlled by centered on the current track. (ATF control will be described in a later section).

(1) Rotation speed command

The rotation speed command is applied from the system controller to pin 46 through 51 of the servo controller IC-104, as with the case of REC mode (see table 8-4-1).

(2) Torque command

(a) When pin 60 (servo mode command) of the servo controller IC-104 is set low, the controller is switched to the speed control mode, in which a torque command sppears at pin 81. The torque command is then applied to integrating circuit IC-206, where it is converted into a DC level signal.

(b) At the same time, pin 17 (ATF ON/OFF command) of IC-104 is set high, which sets pin 20 of the ATF drive IC-201 to high. As a result, an ATF control signal appears at pin 17 of IC-201.

(c) The torque and ATF control signals are then applied to a low-frequency compensation circuit, where they are added to each other. This summation signal is transferred, as a torque command, to pin 10 of the capstan motor driver IC-208 via IC-203.

8-5 Integrating and Low-Frequency Compensation Circuits

The integrating circuit integrates the three-level PWM torque signals (for capstan and cylinder motors) coming from the main servo controller IC-104 into DC level signals, which are then used for driving the respective motor drivers to control their motor torques. The following describes only the capstan motor circuit operations.

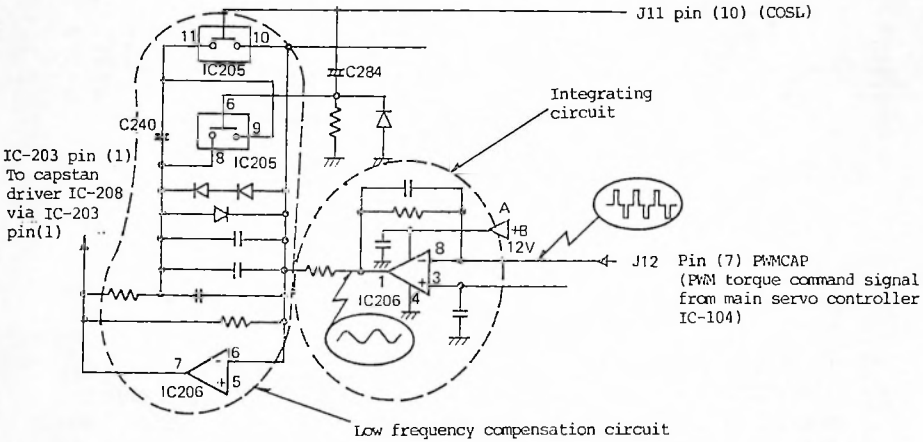


Figure 8-5-1

1) Integrating Circuit Operation

(1) The torque command signal (PWM signal) from the main servo controller IC-104 is applied to IC-206's internal integrating circuit, where it is converted into a DC level signal.

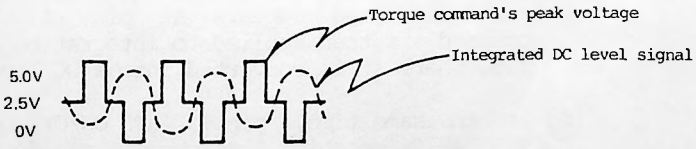
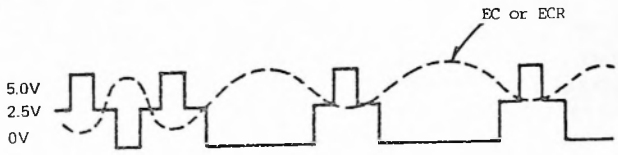


Figure 8-5-2

(2) When the motor speed is normal, the PWM torque command signal has a relatively short period. If motor speed varies, the signal period is extended as shows in figure 8-5-3. As a result, the integrated DC level deviates to the positive or negative side to a level of 2.5 volts, serving as an acceleration or deceleration command to the motor driver.



(capstan motor)
2.5V > EC: deceleration command
2.5V < EC: acceleration command

(cylinder motor)
2.5V > ECR: acceleration command
2.5V < ECR: deceleration command

Figure 8-5-3

2) Low-Frequency Compensation Circuit

(1) The remaining portion of IC-206 is a low-frequency compensation circuit. It serves to supply a high precision torque command signal to the motor driver by increasing the voltage gain for the acceleration or deceleration torque command.

(2) As mentioned earlier, the capstan servo accomplishes motor speed control by using the capstan FG signal in PLAY mode and reel FG signals in FF/REW mode. This means that the FG signal period in PLAY mode differs from that in FF/REW mode. This leads to the necessary for low-frequency compensation with different cutoff frequencies in these two modes. The switching device IC-205, switches this cutoff frequency for more precise servo control.

(a) In FF/REW mode, pin 10 of IC-206 is shorted to pin 11, which connects the capacitors to the low-frequency compensation circuit within the same IC to select the other cutoff frequency.

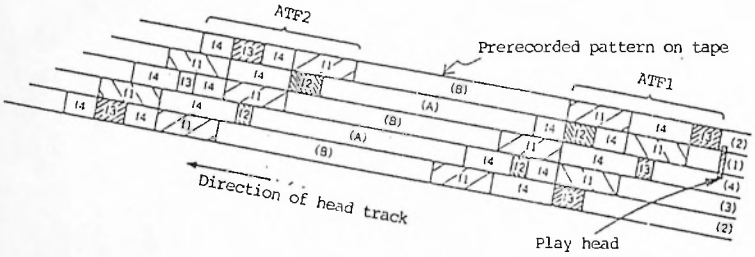
(b) C284 is differentiating capacitor. When IC-205's pin 10 is high, it yields a high pulse, which shorts pin 8 of IC-205 to pin 9. This discharges C240 and prevents adverse affects from torque command switching.

8-6 ATF Servo

The ATF servo controls (in PLAY mode) tape speed (capstan motor speed) so that the play head always tracks the center of the current track.

1) Operation

The play head picks the prerecorded ATF signal pilot (f1= 130 KHz) off the two tracks adjacent to the track being played. The ATF servo detects the level difference between these two pilots and controls capstan motor speed (tape speed) according to the level difference, so that the play head always tracks the center of the current track.



f1 = fch/72 (PILOT): 130.67 kHa
f2 = fch/18 (SYNC1): 522.67 kHz for A
f3 = fch/12 (TSYNC2): 784.00 kHz for B
f4 = fch/6 (ERASE): 1.568 MHz

** When track (1) is being played, the head picks up the pilots f1 in this sequence: i.e. ATF(1), ATF(2), ATF1(4), ATF2(2), ATF2(4), and ATF2(1).

** If the level of f1 on track (4) is indentical to that on track (2), the play head is tracking the center of the main track.

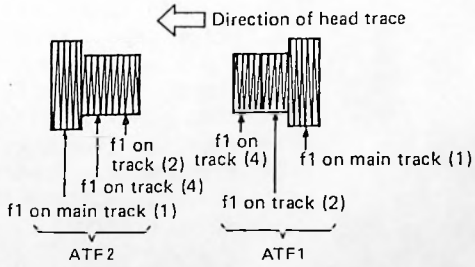


Figure 8-6-1

2) Circuit Description (Based on Block Diagram)

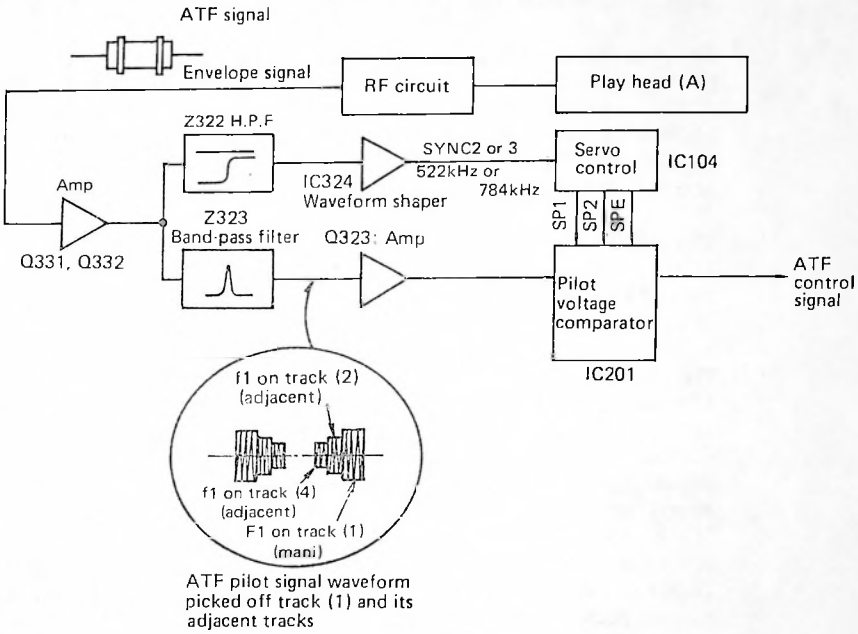


Figure 8-6-2

(1) The signal recording on tape is picked up by the rotary heads and applied to high-pass filter (HPF: Z322) via an RF circuit.

(2) The HPF filters out the 130 KHz pilot component from the playback signal so as to stabilize the operation of the following circuit, IC-324.

(3) The signal, after being waveform-shaped by a comparator IC-324, is applied to the servo controller IC-104, which detects the SYNC signal components (522 KHz for head A: 784 KHz for head B) from playback signal and creates sampling clocks.

(4) The sampling clocks appearing at pins SP1, SP2, and SPE of IC-104 are applied to IC-201, where they are used to sample-and-hold the pilot signal.

(5) In the mean time, the playback signal takes another part to band-pass filter (BPF; Z323), where the 130 KHz pilot signal is extracted from it. The pilot signal picked up by head A has a different envelope from that picked up by head B, as different ATF signal patterns are recorded for these heads.

(6) The pilot signal is then applied to a detector circuit IC-201 where it is subject to envelope detection. The resulting envelope is sampled by the sampling clocks, SP1, SP2, supplied from IC-104.

(7) The pilot signal's peak levels obtained off the adacent tracks are sampled-and -hold within IC-201 and are used for controlling capstan motor speed so that the difference in the peak levels is nullified. The velocity and ATF control signals for this purpose are supplied from IC-201 to capstan motor driver IC-208.

When a non-recorded blank on tape is encountered, capstan motor speed is slightly increased within the servo lock range so that the ATF servo is pulled in as soon as the heads subsequently enter a recorded portion.

3) Sampling Pulse Timing

The SYNC signal, f2 (522.67 KHz) or f3 (784 KHz), is extracted from the ATF signal contained in the playback envelope signal (coming from the RF circuit). It is then applied to the ATF block within the servo controller IC-104, where sampling clocks, SP1, SP2, and SPE, are created and transferred to the ATF block within IC-201.

(1) SP1

(a) Timing
The servo controller IC-104 yields SP1 immediately after it has detected the ATF SYNC signal (f2 or f3).

(b) Purpose

SP1 is used sampling the peak levels of the pilot signal pickud off either of the adacent tracks.

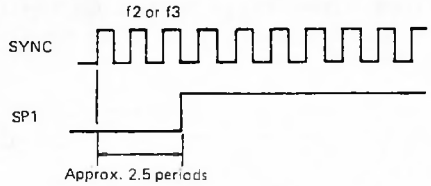


Figure 8-6-3

(2) SP2

(a) Timing
The servo controller yields SP2 at the timing shows at left, after it has detected the ATF SYNC signal and yielded SP1.

(b) Purpose
SP2 is used for sampling the peak levels of the pilot signal picked off either of the adacent tracks. (SP1 samples the pilot read off the untraced track from the two adjacent tracks, while SP2 samples that read off the already traced track).

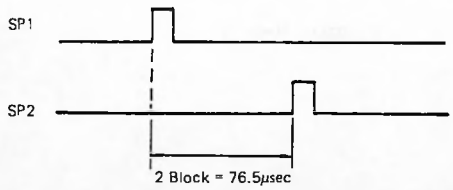


Figure 8-6-4

(3) SPE (Sample Pulse Error)

(a) Timing
The servo controller yields the SPE signal at the trailing edge of the HSW signal (see figure 8-6-5).

(b) Purpose

** SPE is used for controlling capstan motor speed so that the play head always tracks the center of the track even if the recorded tracks on tape have poor linearity, by making the ATF control time on the track entrance side equal to that on the track exit side.

** SPE is also used to ensure stable ATF control by canceling offset caused by mechanical loads to the ATF system, etc.

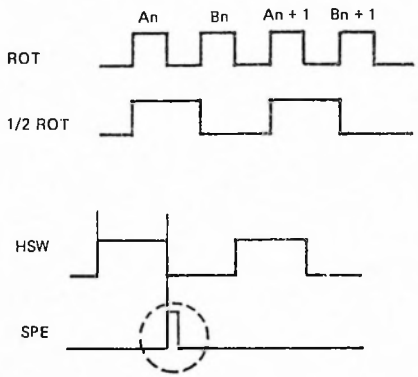


Figure 8-6-5

4) Pilot Signal Peak and Differential Pilot Voltage Detectors

(1) Pilot peak detector

The pilot peak detector, internal to IC-201, detects the peak levels of the 130 KHz ATF pilot signal.

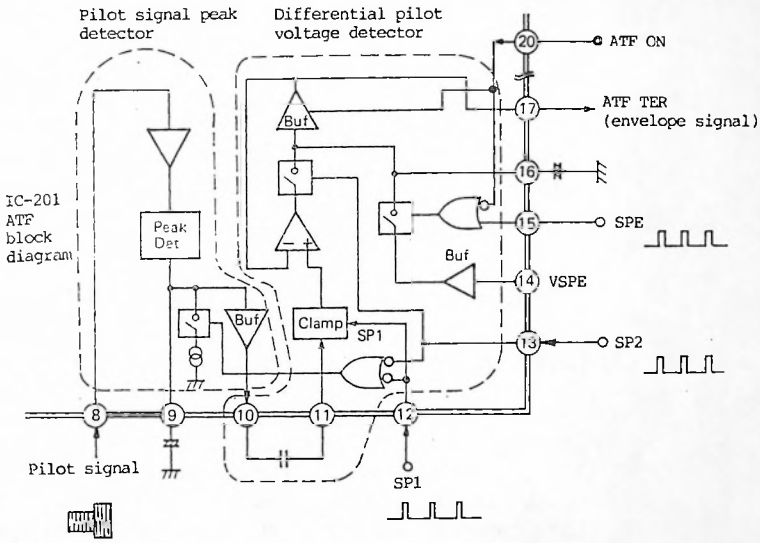


Figure 8-6-6

(a) The pilot signal is extracted by BPF (Z323) and is applied to pin 8 of IC-201.

(b) The pilot signal is then detected by the pilot peak detector.

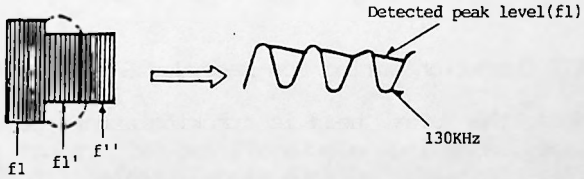


Figure 8-6-7

(c) The detected peak level is sampled-and-hold by sampling clock SP1 applied to IC-201's pin 12 or SP2 applied to IC-201's pin 13, and appears at pin 10 of IC-201.

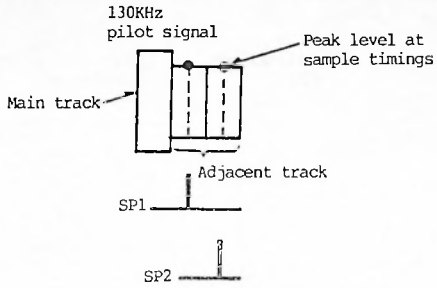


Figure 8-6-8

(2) Differential pilot voltage detector

The differential pilot voltage detector compares the levels of the 130 KHz pilot signals contained in the ATF signals read off the tracks adjacent to the main track (being played) and yields a control signal, to the capstan motor driver IC-208 which will nullify the level difference between the two pilots.

(a) The sampled-and-hold peak pilot levels (for adjacent tracks) are applied to a clamp circuit within IC-201.

(b) The clamp circuit, along with an external capacitor, extracts a differential voltage of the two peak pilot levels.

(c) The differential voltage is sampled-and-hold at the SP2 sampling clock timing (at IC-201's pin 13), and appears at pin 17 of IC-201 as an ATF control signal.

5) ATF Operation During Non-Recorded Blank Playback

When the play head is tracking a non-recorded blank on tape, sampling clocks SP1 and SP2 are not applied to IC-201. Instead, a Vspe signal created from the SPE clock appears at pin 17. It is used to slightly increase tape speed in such non-recorded blanks (so that ATF servo is pulled in as soon as the head subsequently enters a recorded portion).

8-7 Cylinder Servo

The cylinder servo circuit uses different servo techniques for REC/PLAY and FF/REW modes.

**REC/PLAY mode ..... speed + phase servos
**FF/REW mode ..... system servo

1) Cylinder Servo in REC/PLAY Mode

In REC/PLAY mode the servo circuit detects the FG and PG signals from the cylinder motor provides speed and phase control to maintain the constant motor speed of 2000 rpm.

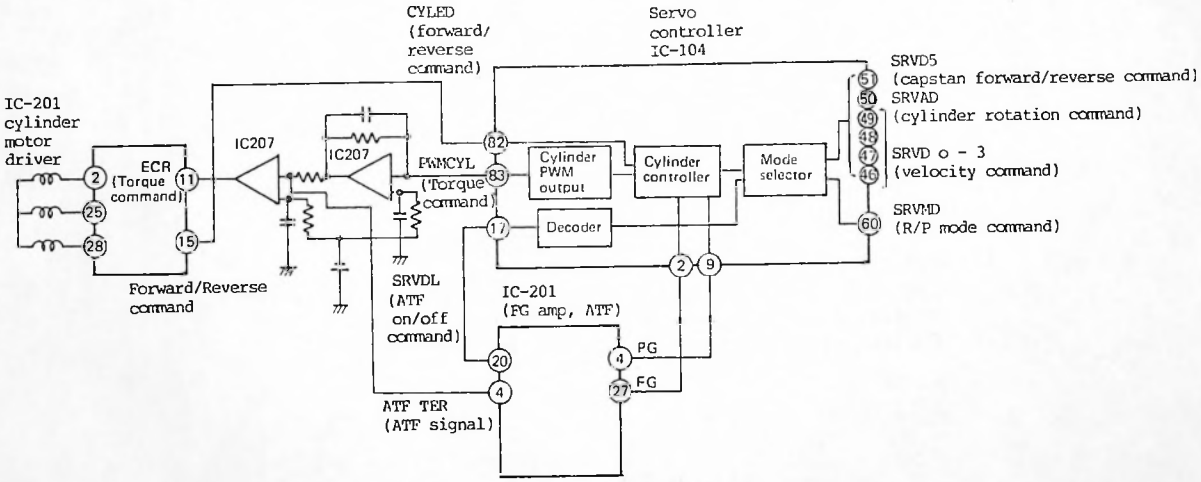


Figure 8-7-1

(1) Cylinder rotation speed command

The cylinder rotation speed command is applied to pins 46 through 51 of the servo controller IC-104 as with the case of the capstan rotation speed command.

** The servo controller IC-104 contains both cylinder and capstan motor control circuits, which yield different velocity commands for the same speed command applied to pins 46 through 51.

(2) Torque command

The cylinder FG and PG signals are applied to pins 2 and 9 of IC-104 where they are subject to speed and phase control. The resulting signal appears at pin 83 as a cylinder motor troque command.

(3) Integrating circuit

The integration circuit IC-207 integrates the torque command (phlse array) supplied from IC-104's pin 83 into a DC level and couples it to pin 11 of cylinder motor driver IC-210 as a torque signal via low-frequency compensation circuit IC-207.

2) Cylinder Servo in FF/REW Mode

(1) In FF/REW mode, tape speed varies to 25, 50, 75, 100, 150, and 200 times in the REC/PLAY mode.

(2) As the tape speed varies, cylinder motor's rotation speed must vary step-by-step from 2000 to 3000 rpm in FF mode or 2000 to 1000 rmp in REW mode.

(3) This cylinder motor speed variation is controlled only by speed servo control using the FG signal.

(a) Cylinder rotation speed command
Cylinder rotation speed command is applied to pin 46 through 49 of the servo controller IC-104. The following shows the command bit status:

Table 8-7-1

IC104's pin 46	H	L	H	L	H	L
47	H	L	L	H	H	L
48	H	L	L	L	L	H
48	L	H	H	H	H	H
Tape speed in FF/REW mode	x 25	x 50	x 75	x 100	x 150	x 200

IC-104's pin 50 is low when the cylinder is rotating, and is high when it is stationary. IC-104's pin 51 is high in FF mode, and is low in REW mode.

(b) Torque command and integrating circuit

See paragraphs (2) and (3) under "Cylinder Servo in REC/PLAY mode."

3) Cylinder Servo Gain Switching Circuit

At a tape speed transition (e.g.from x50 to x75) during high-speed search, a relative speed difference occurs between the tape and the head, which may lead to subcode overlook error. In order to prevent this, cylinder servo gain is reduced for a certain time period (100 ms in FF, 50 ms in REW) at the beginning of tape speed changes to suppress the relative speed difference.

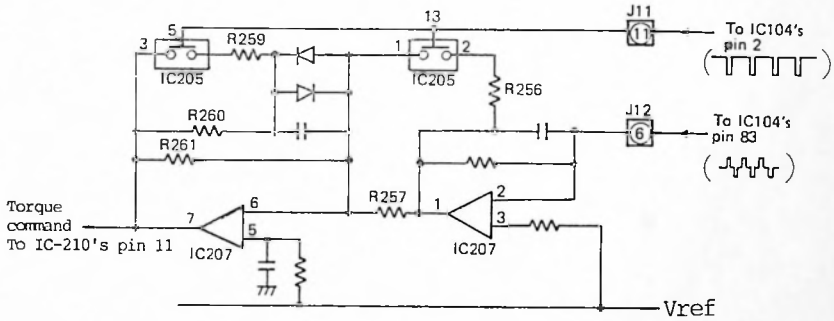


Figure 8-7-2

(1) IC-205 is turned on or off depending on the cylinder gain (CYL GAIN) signal status (OFF if low. ON if high).

(2) When IC-205 is off, R256 and R259 are not included in the feedback loop, letting the amplifiers provide the normal servo gain. When IC-205 is on, R256 and R259 are inserted into the feedback loop to reduce the servo gain.

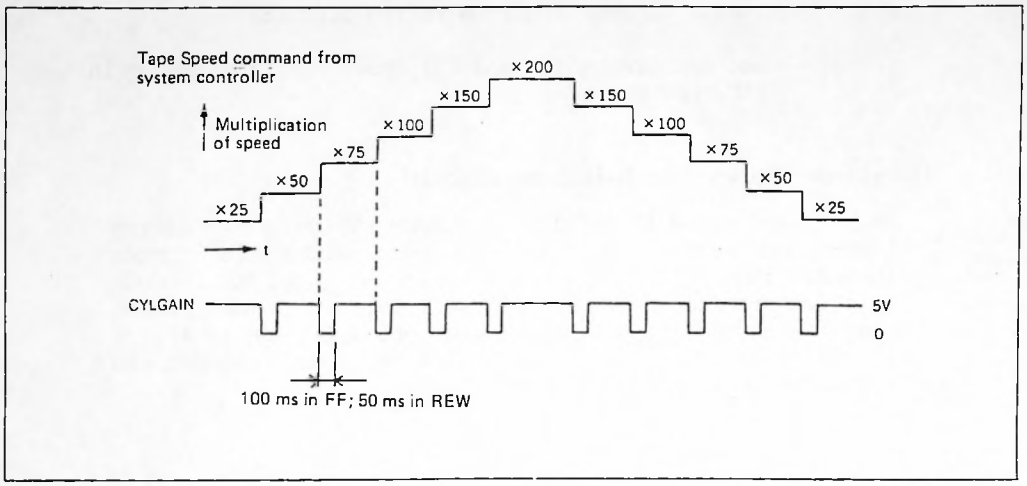

Tape Speed command from system controller
Multiplication of speed
×25
×50
×75
×100
×150
×200
×150
×100
×75
×50
×25
t
CYLGAIN
5V
0
100 ms in FF; 50 ms in REW

Figure 8-7-3

8-8 Reel Servo

The reel servo regulates the relative speed of the cylinder and tape during high-speed serach to make sure that the deck can read subcode information prerecorded on tapes without any omission.

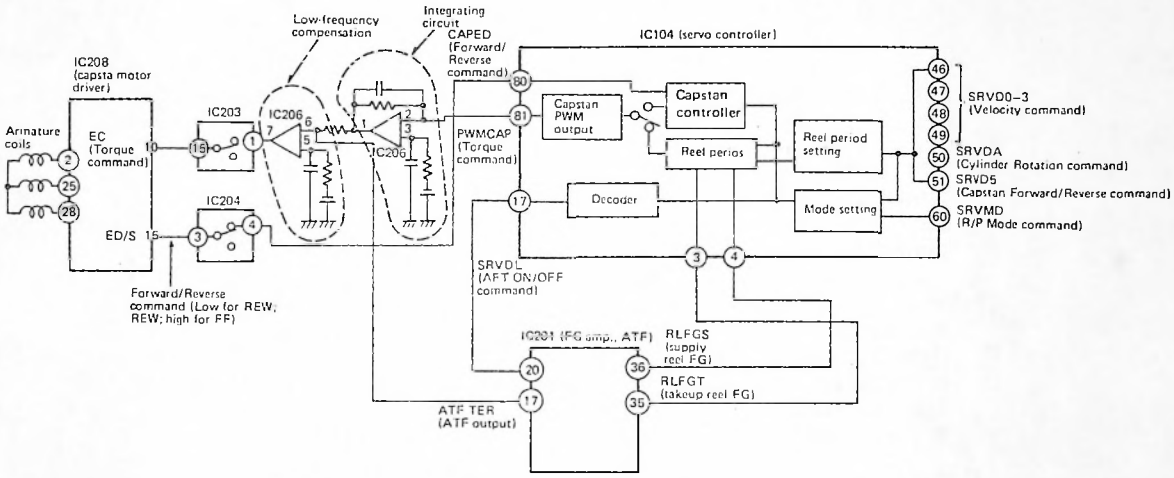


Figure 8-8-1

(1) The takeup and supply-reel FG signals from pins 35 and 36 of IC-201 are applied to pins 3 and 4 of IC-104 respectively.

(2) The FG signal pulses are counted within IC-104 and the sum of the supply and takeup FG pulse counts is computed.

** The sum of the supply and takeup FG counts is specified for each search speed (x25 through x200).

(3) The servo controller IC-104 then provides servo control so that the sum of the measured FG pulse counts equals the pulse count specified for a specific search speed.

** Pins 46 through 49 of IC-104 accept a tape speed command (x25 through x200) in FF/REW or search mode.

(4) The servo controller checks if the PLL signal which was read off the tape during search is locked with the internal reference PLL signal. If the PLL lock is off, the controller adjusts the reel period setting until they are locked.

**Example of circuit operation at the beginning of FF mode.

(1) The mechanism controller IC-107 issues a x25 speed command to the servo controller IC-104.

IC-104's pin 46 : High
47 : High } Condition for x25 speed
48 : High
49 : Low
50 : Low - Cylinder start command
51 : High - Capstan FWD/REV command (now FF)

(2) The above command information is applied to the servo controller, which then yields a velocity command for x25 speed at its pin 81. This command is used for controlling capstan motor torque.

(3) When the system controller detects that the servo system is set up for x25 speed and the signal processor detects a PLL lock state at the x25 speed, the speed controller issues the next velocity command for x50 to the mechanism controller, which then transfers the corresponding velocity command to the servo controller.

(4) These steps (1) through (3) are repeated until the tape speed reaches x200.

8-9 Power-Off Unload Circuit and the Unload Circuit

1) Power-off Unload Circuit

This circuit forcibly unloads the tape if the deck is Turned off in any mode (FF, REW, PLAY, REC, PAUSE) other than the STOP mode.

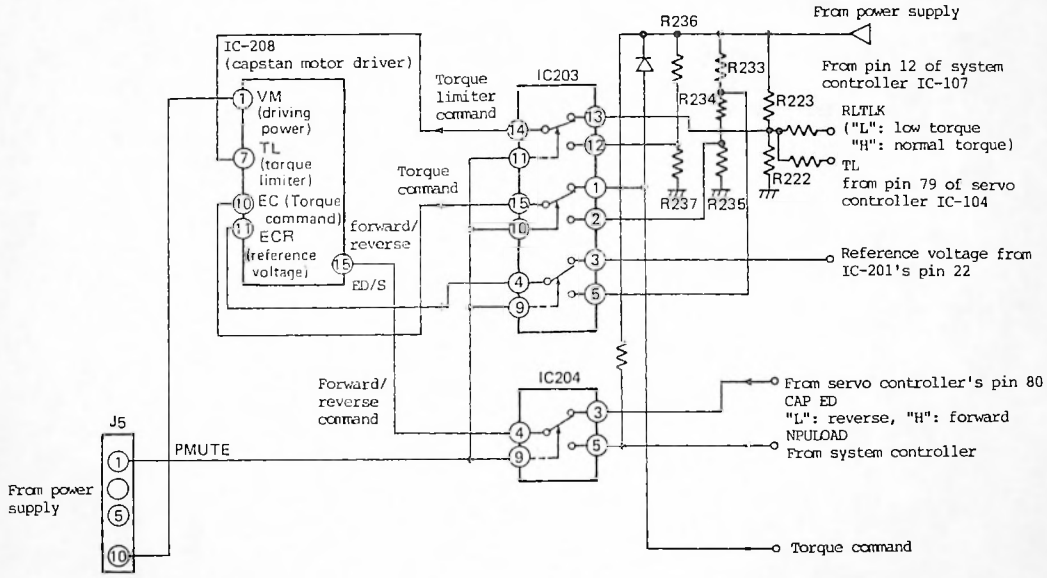


Figure 8-9-1

(1) At power off, the P MUTE signal from pin 1 of J5 switches IC-203/204's switch contacts to issue the following commands to the capstan motor driver:

** Torque command:
IC-203's pin 2 to 15 (voltage divided by R233/234/235).

** Torque limiter command:
IC-203's pin 12 to 14 (voltage divided by R236/237).

** Reference voltage:
IC-203's pin 5 to 4 (voltage divided by R233/234/235).

** Forward/Reverse command:
IC-204's pin 5 to 4 (command from system controller's NPU LOAD circuit).

2) Unload Circuit

Upon tape unload, the unload circuit limits tape reel torque so as to prevent tape slack on the unloaded cassette.

(1) The torque limiter (TL) command (servo controller's pin 79) is normally high. It is set to low only for tape unload.

(2) The RL TLK (reel torque) command (system controller's pin 21) is normally high. It is set to low when supply reel rotation is detected during tape unload.

RL TLK : High ..... Normal torque
Low ..... Low torque

(3) A torque limit command is issued to pin 7 (TL) of the capstan motor driver IC-208 only during tape unload.

8-10 Triangular Wave Generator

This circuit supplies the switching regulator (see the description of the power supply) with a triangular wave so that the regulator can supply the necessary minimum power to the motor drivers (IC-208 for capstan; IC-210 for cylinder) so as to prevent head dissipation caused by excess power.

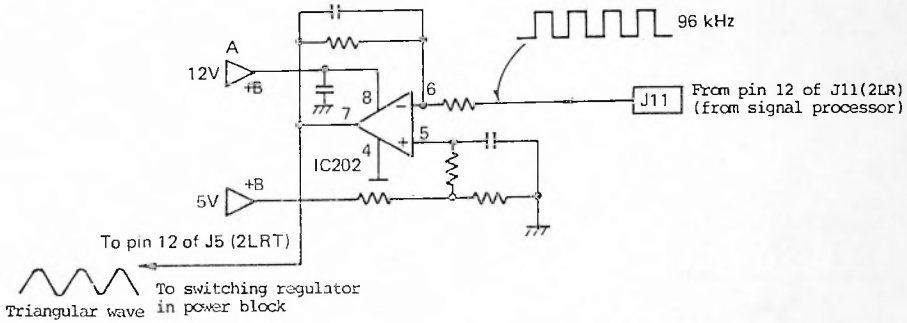


Figure 8-10-1

(1) The 2LR signal (96 KHz, twice the L/R switching signal frequency) is applied from the signal processor to IC-202.

(2) The integrating circuit IC-202 creats a triangular wave and supplies it to the switching regulator in the power block.

8-11 Servo Block Pin Names and Symbols

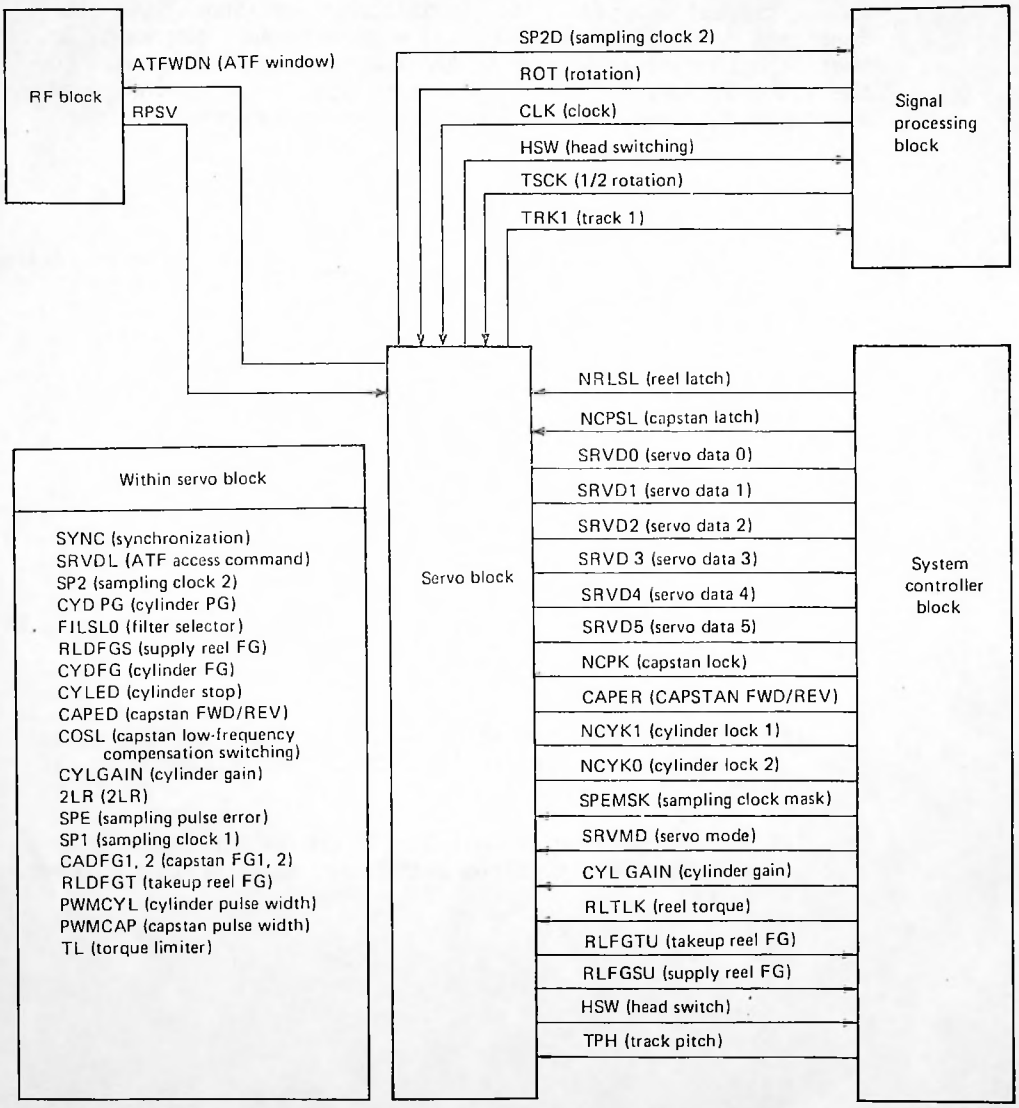


Figure 8-11-1

9. Tape Loading

9-1 Loading Mechanism Layout and Functions

1) Top View of Loading Mechanism

2) Bottom View of Loading Mechanism

9-2 Loading Operations and Functions

1) Tray Close Sequence

2) Tray Open Sequence

9-1 Loading Mechanism Layout and Functions

1) Top View of Loading Mechanism

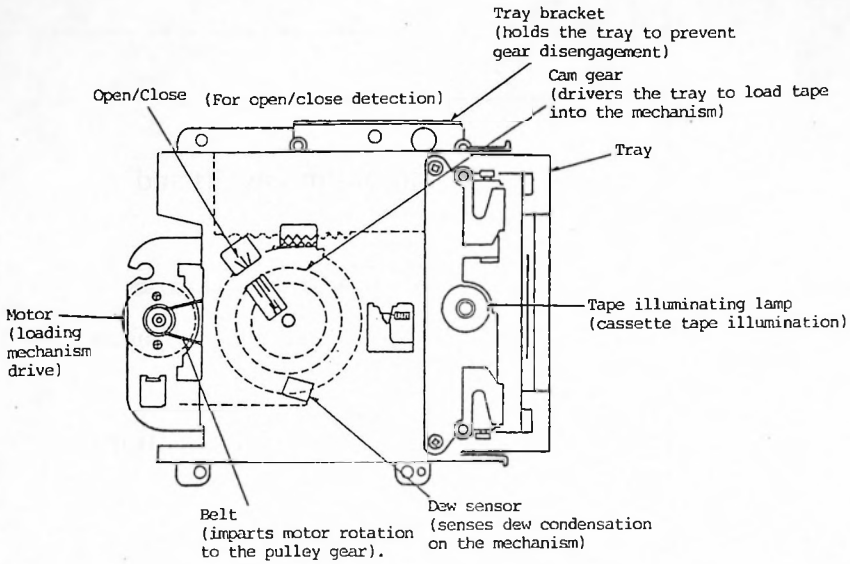


Figure 9-1-1 Top View of Loading Mechanism

2) Bottom View of Loading Mechanism

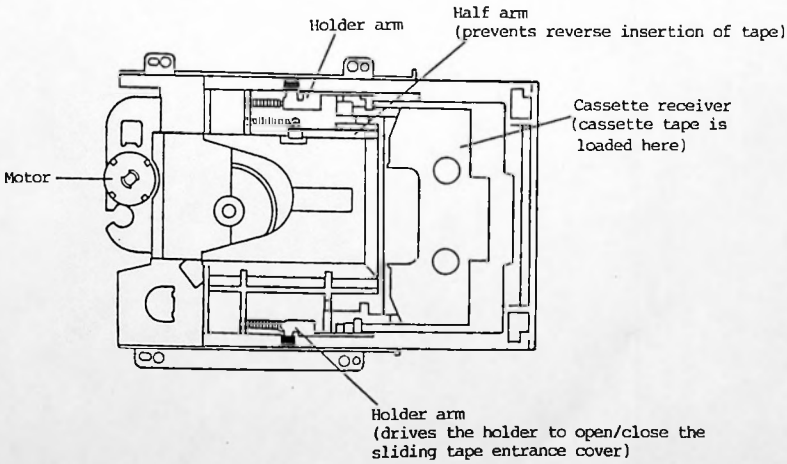


Figure 9-1-2 Bottom View of Loading Mechanism

9-2 Loading Operations and Functions

1) Tray Close Sequence

(1) If the OPEN/CLOSE switch is pressed when the tray is in the open position, the system processor IC-107 is informed. The processor then applies command voltages to pin 3 and 10 of the tray motor drivers, IC-115/ IC-119, which then drive the pulley gear via the belt.

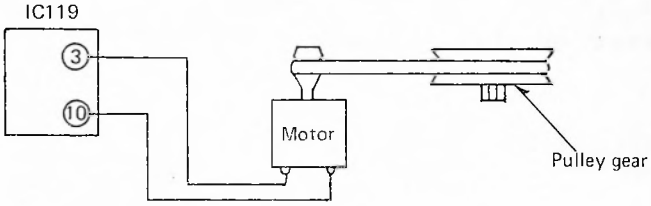


Figure 9-2-1

(2) The pulley gear is engaged with cam gear A.

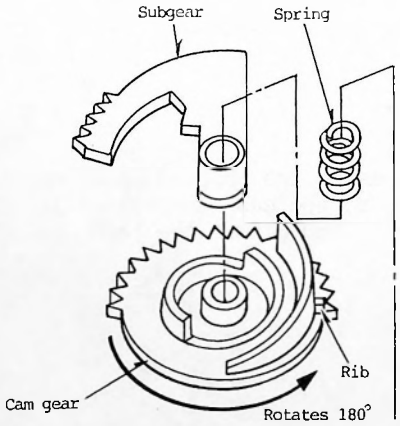


Figure 9-2-2 Cam Gear Backface

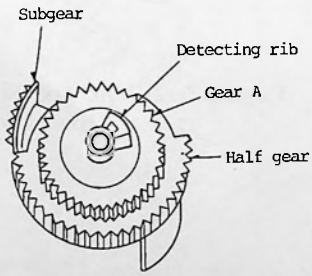


Figure 9-2-3 Cam Gear Surface

(a) Cam gear

The upper cam gear assembly has a detecting rib, gear A, and a half gear. It has the same diameter as the subgear.

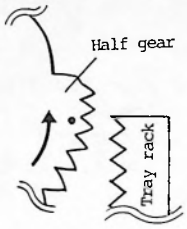
The lower cam gear assembly has a tapered cam, which receives a control plate pin along its slope.

(b) Subgear

The subgear has the same diameter as the half gear. It rotates over an angle of 180 degree.

(c) The cam gear and subgear are retained with a shaft spring.

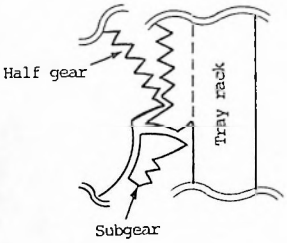
(d) The half gear is engaged with the tray rack.



Note: The last tooth of the tray rack engages with the second slot of the half gear.

Figure 9-2-4 Gear Engagement

(3) As the pulley gear rotates, the half gear rotates counterclockwise. This pulls the tray rack into the deck.



The tray rack has a larger tooth at its leading end. When the tray rack is fully retracted, the larger tooth is caught between the half gear and the subgear and this latches the tray rack. The half gear continues rotation after it is disengaged from the tray rack.

Figure 9-2-5 Gear Engagement in the Retracted Position

(4) As the control plate pin ribes on the tapered cam on the bottom side of the cam gear, the cassette holder is lowered onto loading mechanism and places the tape on it.

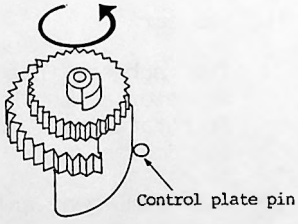


Figure 9-2-6 Control Plate Pin Riding on Tapered Cam

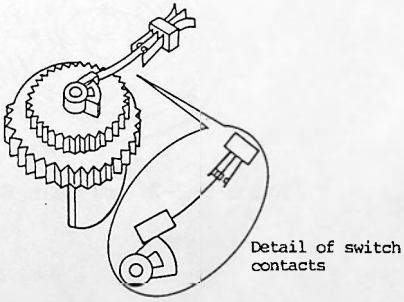


Figure 9-2-7 At the End of Tray Close Operation

As shows in figure 9-2-7, the detecting rib pushes the leaf switch ON, which issues a tray close end command, to the system processor IC-107 to complete the tray close sequence.

2) Tray Open Sequence

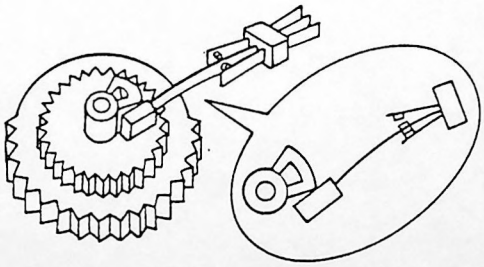
(1) If the OPEN/CLOSE switch is pressed when the tray is in the closed position, the system processor IC-107 is informed

The processor then applies command voltages (which are the reverse to those provided for the tray close sequence) to pin 3 and 10 of the tray motor drivers, IC-115 and IC-119, which then drive the tray motor. The tray motor drives the pulley gear via a belt.

(2) As the cam gear rotates counterclockwise, its tapered cam drives the control plate pin, which is normally lifted from the frame by spring force. As the control plate pin ribes on the tapered cam, it is lifted upward to raise the cassette tape from the loading mechanism.

(3) The tray rack, which is engaged with the half gear, is driven forward to drive the tray to the open position.

(4) The detecting rib on the cam gear pushes the leaf switch ON, which provided a tray open end command to the system processor IC-107 to complete the tray open sequence.



Detail of switch contacts

Figure 9-2-8

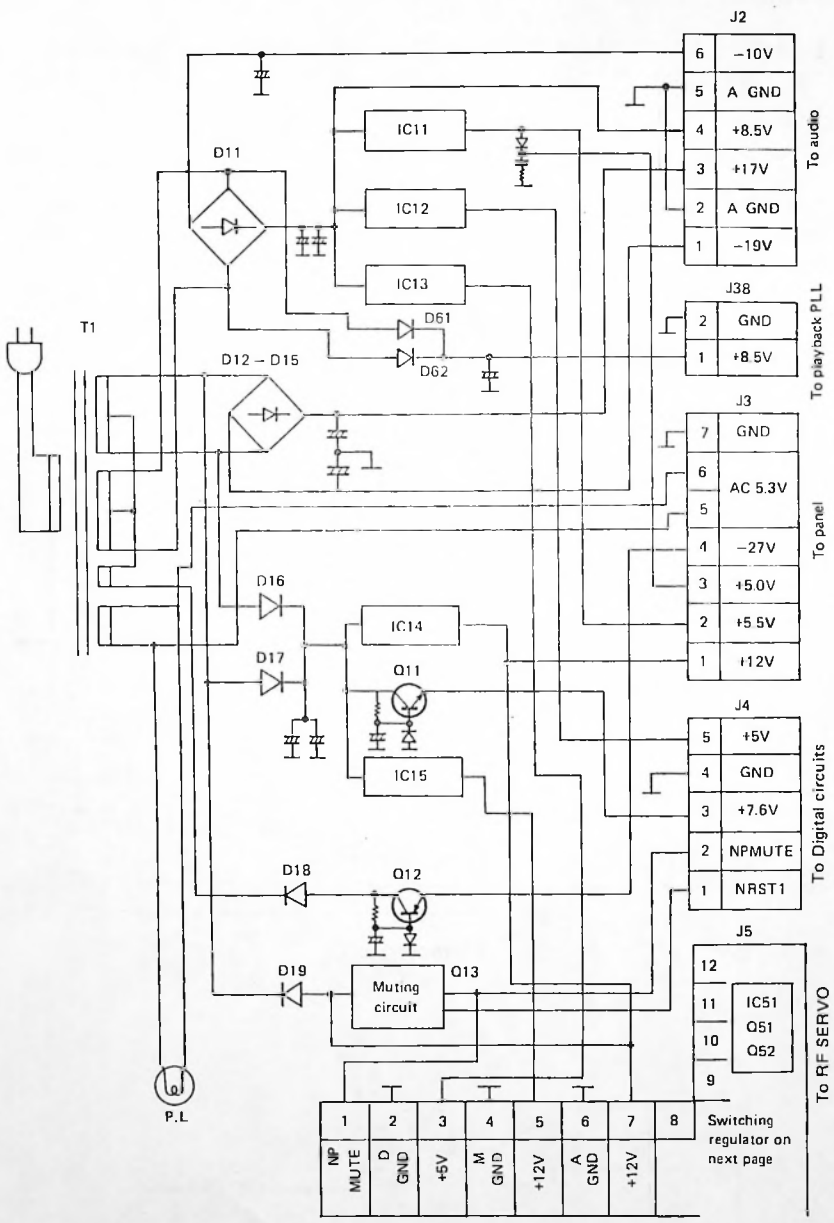
10. Power Supply

10-1 Block Diagram

10-2 Motor Drive Power Supply

10-3 Muting Circuit

10-1 Block Diagram



10-2 Motor Drive Power Supply

1) General

The SV-3500 employs the following power-saving circuit configuration to cylinder and capstan motors.

2) Circuit Description

The cylinder and capstan motor driving circuits have the same configuration. The following describes only the capstan motor driving circuit.

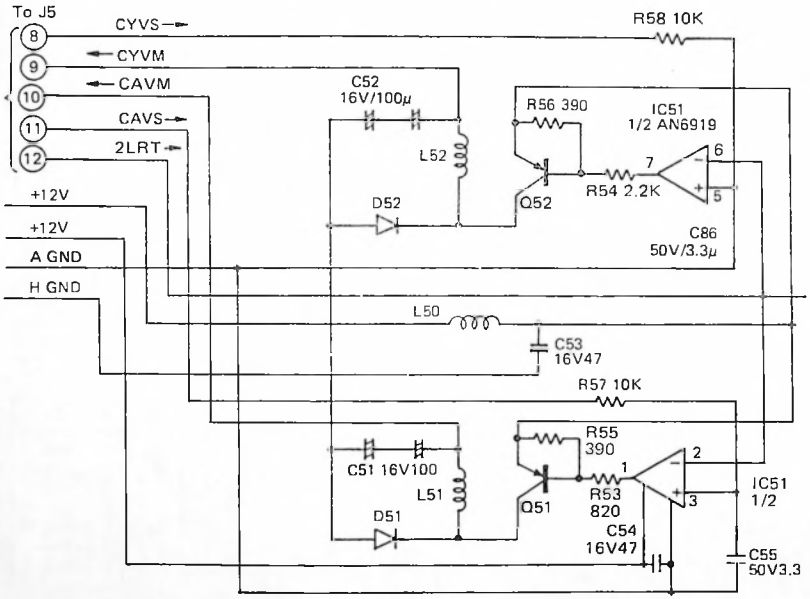


Figure 10-1

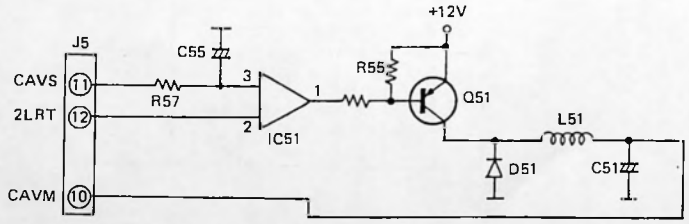


Figure 10-2 Schematic of Switching Regulator

(1) The CAVS signal (motor's FG signal) from the servo circuit is applied to pin 11 of connector J5 (see figure 10-3(A)).

(2) The 2LRT signal from the servo circuit is applied to pin 12 of J5 (2LRT is a 96 KHz triangular wave signal which is created by the signal processing circuit and used as a reference voltage signal). (see figure 10-3(B)).

(3) CAVS and 2LRT are then coupled to pin 3 and 2 of IC-51, respectively, where they are compared with each other. The resulting square-wave signal, appearing at IC-51's pin 1, varies its pulse width depending on tape speed (see figure 10-3(C)).

(4) Q51 a switching transistor, yeilds at its collector a square-wave signal which is a inversion of the output of IC-51 (see figure 10-3(D)).

(5) The square wave signal appearing at Q51's collector is then smoothed by L51 and C51 into a DC control voltage and coupled to pin 10 of connector J5 as a CAVS signal.

The signal is transferred to the VM input of the servo circuit's capstan motor driver IC-208 (see figure 10-3(E)).

The switching regulator thus creates motor driving voltages which entirely depend on the level of the CAVS signal (which represents motor rotation speed) and serves to save power.

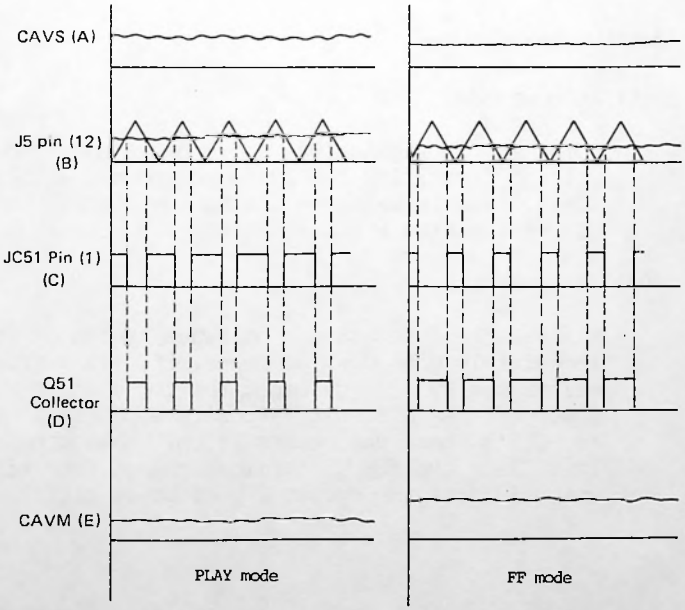


Figure 10-3 Switching Regulator's Signal Waveforms

10-3 Muting Circuit

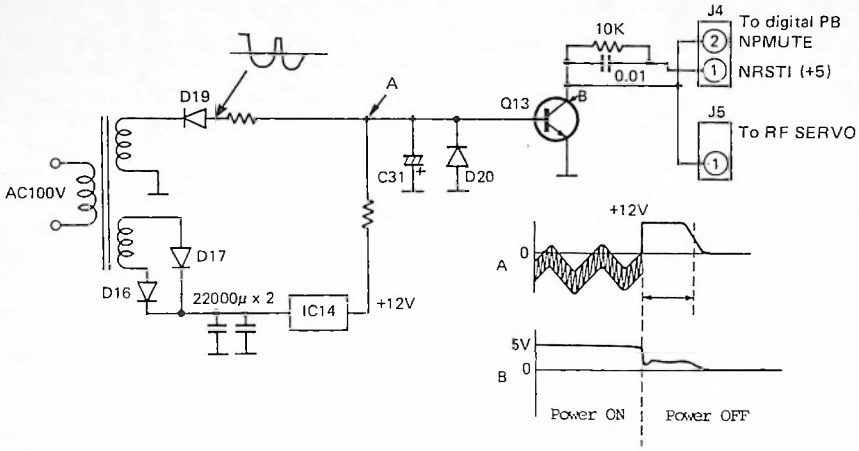


Figure 10-4

1) Purpose

At power on/off, the muting circuit puts the system CPU into a "muting" state to suppress pop noise output to the LINE OUT jacks, LEVEL METERS, or PHONES jack. Also at power off, it issues a tape unload command to the tape loading mechanism.

2) Circuit Description

(1) At power on

Point A in figure 10-4 above has a negative halfwave voltage (rectified by D19) superimposed with +12 V from IC-14, and is balances in the low state, which turns Q13 off, making a potential of +5 V appear at point B.

(2) At power off

While the negative halfwave voltage from D19 immediately goes down at power off, +12 V from IC-14 is maintained by a large capacitor for a short time after power off. As a result, a positive potential is applied to Q13's base and turns it on, making point B low. This lets the NPMUTE terminal change from high to low which informs the system CPU of power off.

11. Mechanism

11–1. Mechanism Compact Layout

11–2. Mechanism Operation

1) Mechanism Mode

2) Mechanism Compact Operation

11–3. Mechanism Mode Transition Timing

11–4. Mechanism Operation and States in Different Modes

11–5. Upper Cylinder Head and Cyliner Block Replacement

11—1. Mechanism Compact Layout

1) Top Side of View

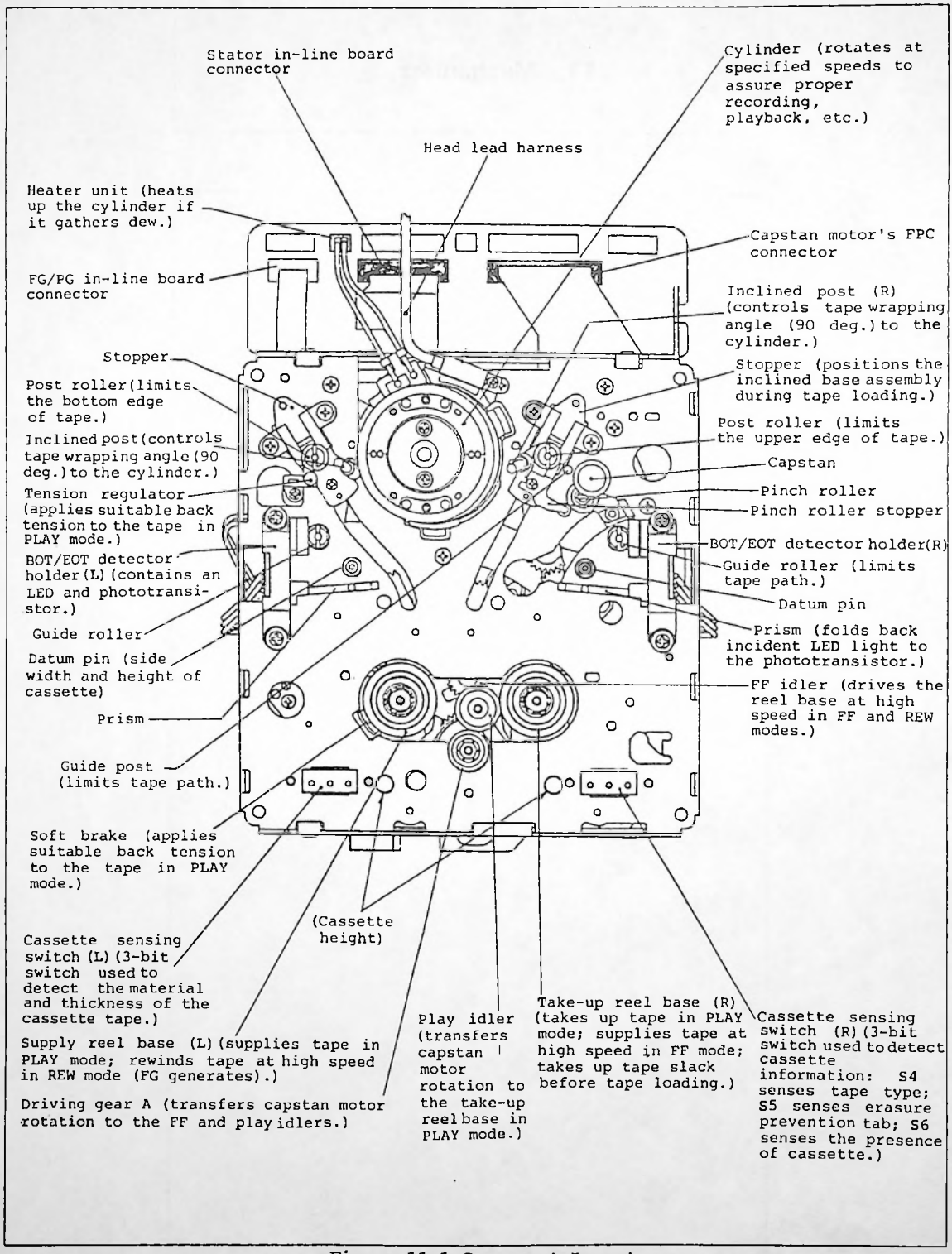


Figure 11-1 Component Layout

2) Bottom Side of View(1)

The following figure shows a bottom-side view of the mechanism after the FG board has been removed:

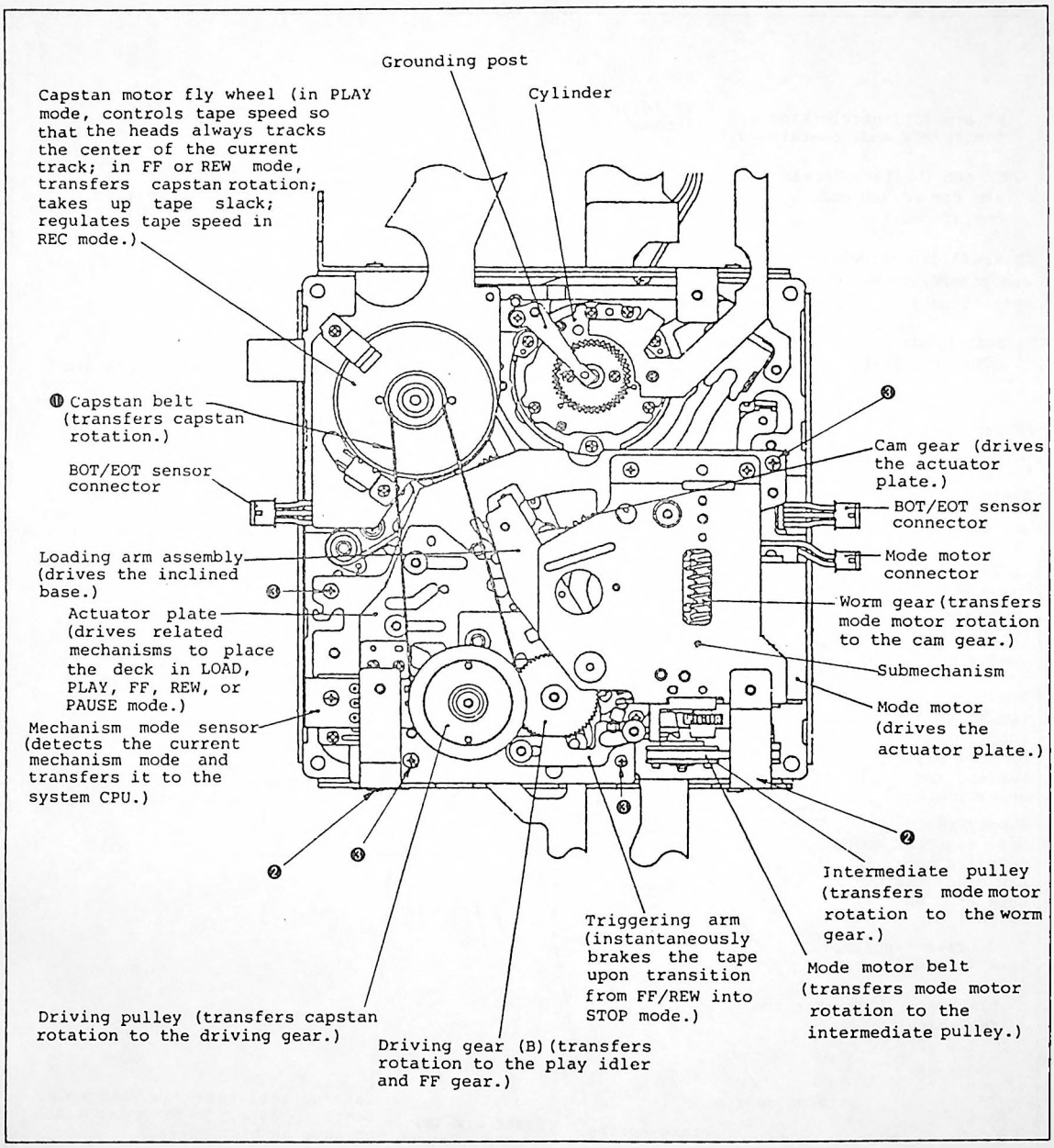


Figure 11-3 Bottom Side (1)

Removing the submechanism assembly.

(1) Remove the capstan belt (1).
(2) Take off the two PB angle screws (2).
(3) Remove the four screws retaining the submechanism assembly.

3) Submechanism Assembly (reel base side)

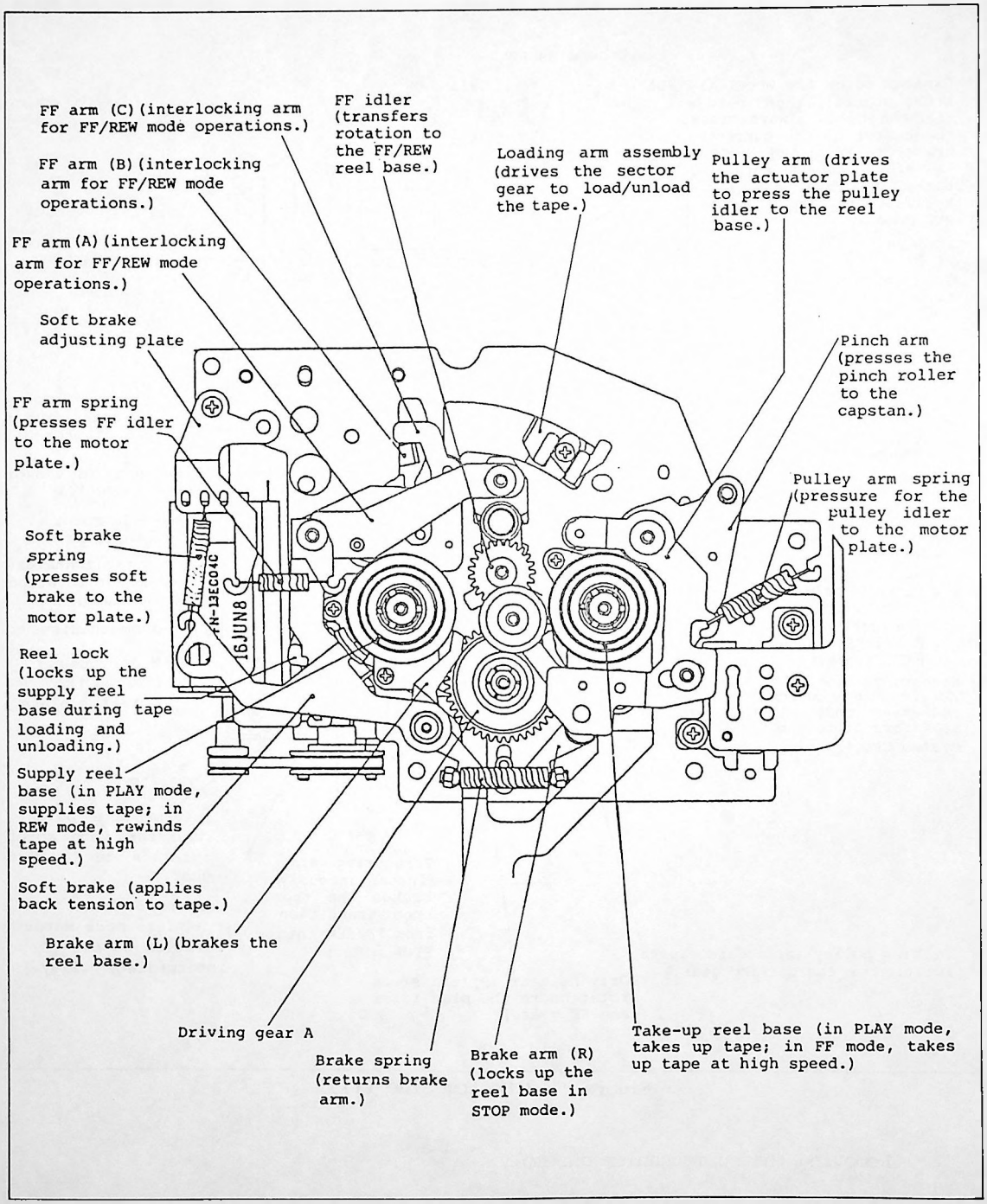


Figure 11-4 Submechanism Assembly (reel base side)

4) Bottom Side of Main Chassis(2)

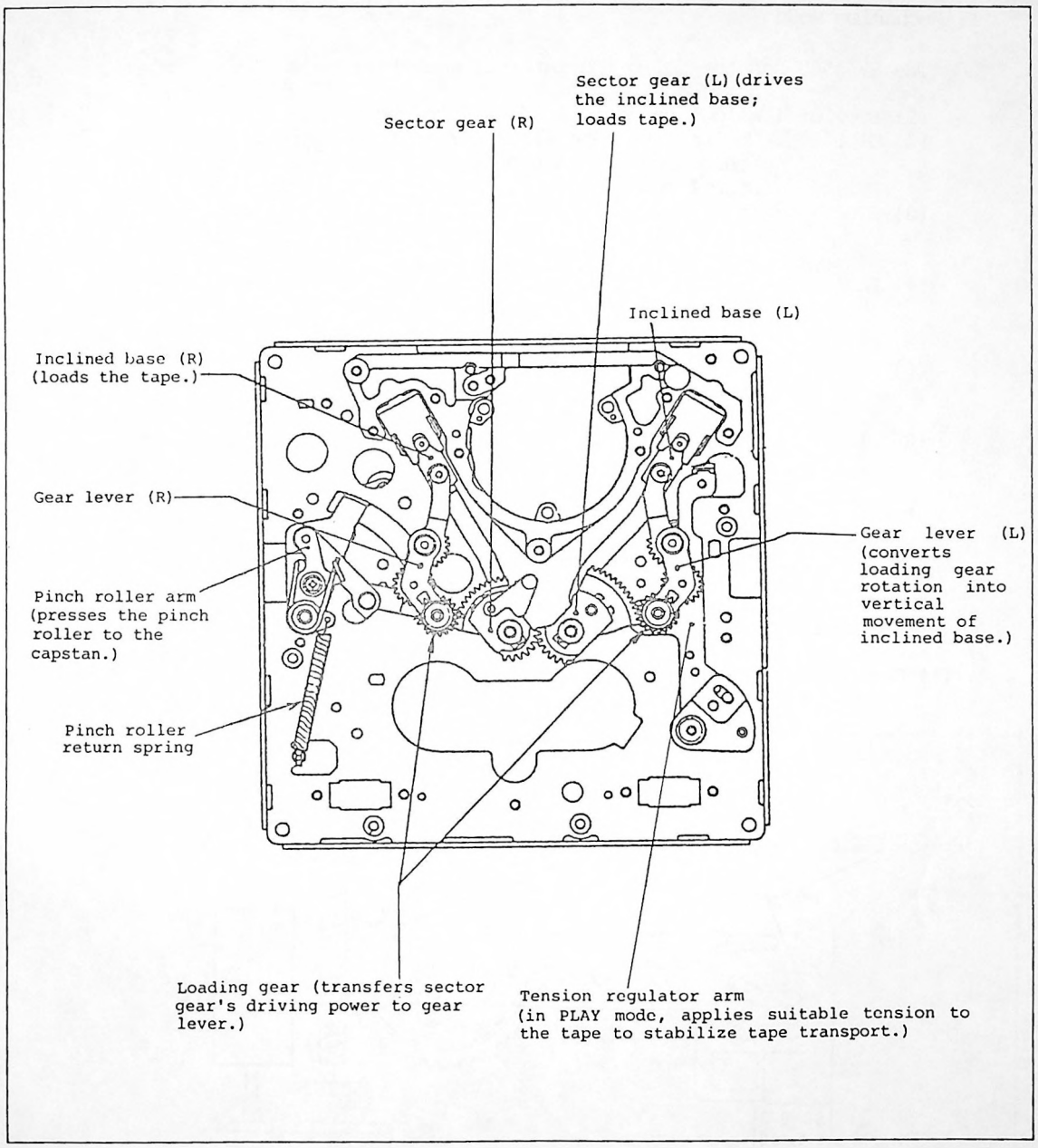


Figure 11-5 Bottom Side of Main Chassis (2)

11–2. Mechanism Operation

1) Mechanism Mode

The SV-3500 has the following internal mechanism modes:

(1) STOP 3 : Allows cassette loading into the deck.
(2) STOP 2 : To take up tape slack during tape unloading (this mode is used only in transitions from STOP 1 mode).
(3) STOP 1 : In this mode the deck is ready tepe loading, or is in STOP mode after tape unloading (ready for cassette eject).
(4) LOAD : In this mode the deck is busy tape loading or unloading.
(5) FF/REW : In FF/REW operation.
(6) PAUSE : The deck pauses in this mode after tape loading is completed or from ther FF/REW/PLAY mode.
(7) PLAY : In this mode the deck transports the tape at a constant speed.

The following outlines the operations of major mechanism components:

2) Mechanism Compact Operation

(1) Cam Gear and Actuator Plate Operation

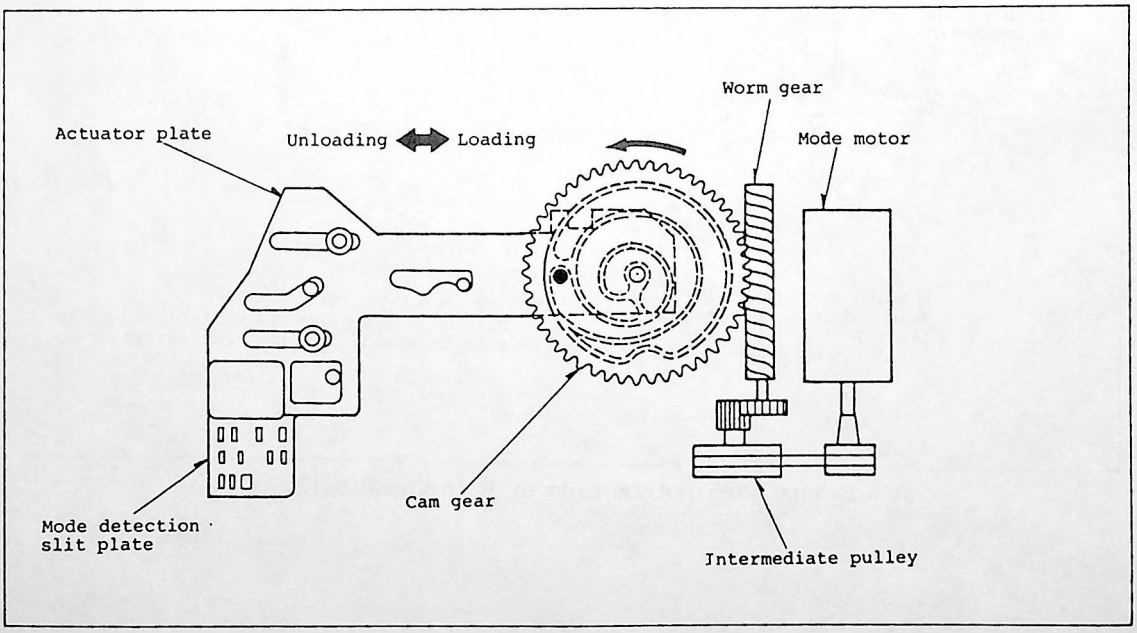


Figure 11-6 Bottom View

(a) The mechanism components are driven by the cam slot provided in the cam gear as the cam gear rotates (see figure 11-6).

(b) The cam gear is driven by the mode motor. It has a rotation span of 440 deg.

(c) The actuator plate slides sidewise as the cam gear rotates. The components linked to the actuator plate are driven by the sliding actuator movement.

Load is excluded from the six mechanism modes

Mode / bit	(1) STOP3	(2) STOP2	(3) STOP1	* LOAD	(4) FF/REW	(5) PAUSE	(6) PLAY
2	o	o	-	-	o	-	o
1	o	-	o	-	-	o	o
0	o	o	o	o	-	-	-

Table 11-1 Mode Sensor's Bit Status for the six modes

(2) Mode Detection Slit Plate Operations

The mode detection slit plate interlocked with the actuator plate, and the photoransistors and LEDs provided above and beneath the slit plate, detect the six mechanism modes which depend on the actuator positions. The detection signal is transferred to the mechanism control logic.

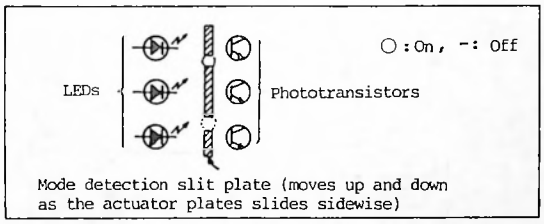


Figure 11-6-1 Mode detection slit plate Sensor operation

(3) Loading Arm and Post Roller Operation

The figure below shows a step in the loading sequence.

(a) The cam gear drives the loading are, which then drives the post roller in the vertical directions to load or unload the tape.

(b) The loading arm is linked with the sector gear (R). As the arm swings in the direction of the arrow (↗), its rotation is transferred to the post roller (R) via the three gears on the gear lever (R) and pushes up the post roller in the direction of the arrow (↖).

(c) The sector gear (R) is engaged with the sector gear (L) via other gears. As sector gear (R) rotates, sector gear (L) also rotates and pushes up the post roller (L), via gear lever (R), in the direction of the arrow (↗).

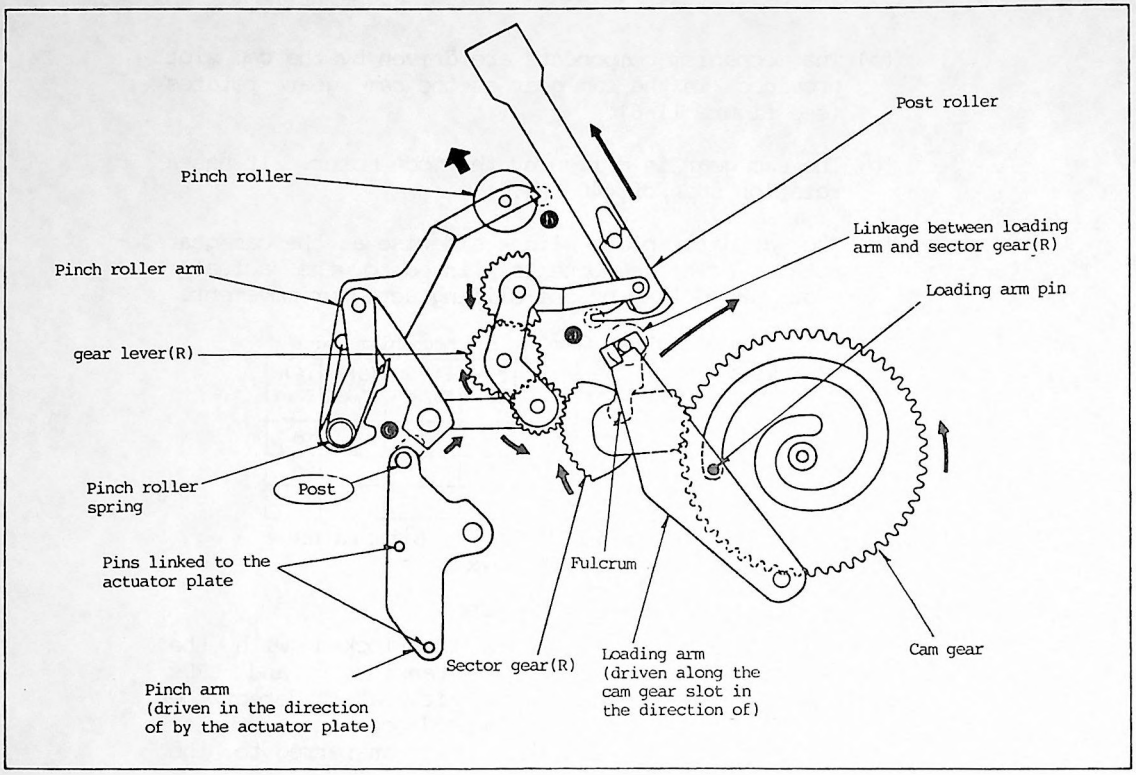


Figure 11-7 Bottom View

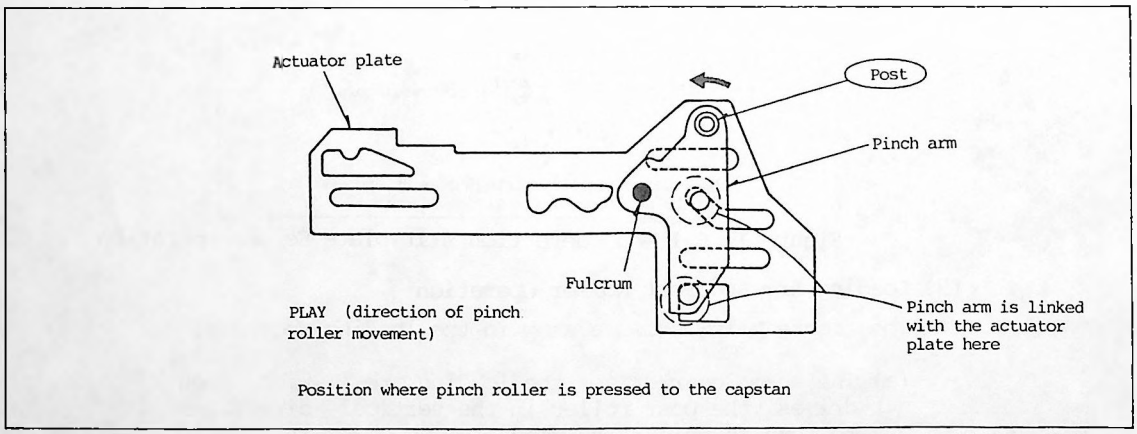


Figure 11-8 Linkage between Actuator Plate and Pinch Arm (viewed from the reel bse)

(4) Pinch Roller Operations

(a) Point (a) of the post roller is brought into contact with point (b) of the pinch roller arm and pushes up the pinch roller in the direction of the arrow (↖).

(b) After this, the pinch arm is swing by the actuator plate in the direction of the arrow (⇦) and pushes up the pinch roller arm in the direction of the arrow (↗) to press the pinch roller to the capstan (point (C) in figure 11-7).

(5) FF Idler Operations

The figure below shows a step in the idler engagement sequnce.

(a) As the cam gear rotates, the FF arm (B) is driven sidewise along the cam gear slot. This causes the component movements indicated by arrow (1) through (4) and engages the FF gear with the driving gear and reel base.

(b) Switching between the FF and REW modes is accomplished when the FF gear swings sidewise as the driving gear rotates in the CW (clockwise) and CCW (counterclockwise) directions.

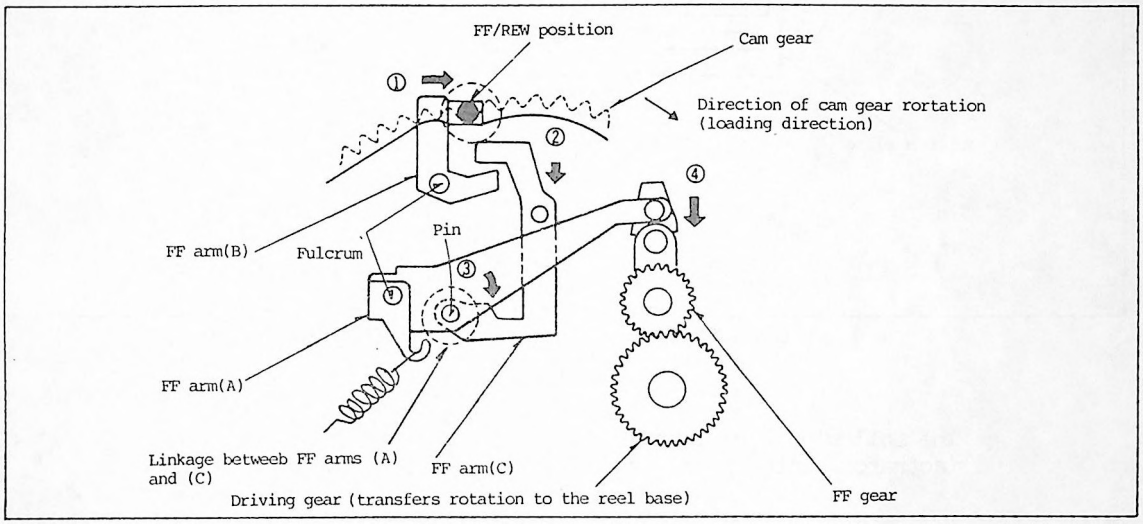


Figure 11-9 View from the Reel Base Side

(6) Reel Lock Operations

The purpose of reel locking is to allow tape loading from the take-up reel by locking the supply reel during tape loading.

(a) The soft kick is driven by the actuator plate in the directions of the arrows (1), (2), and (3), which then drives the reel lock in the direction of arrow (4) to lock up the supply reel.

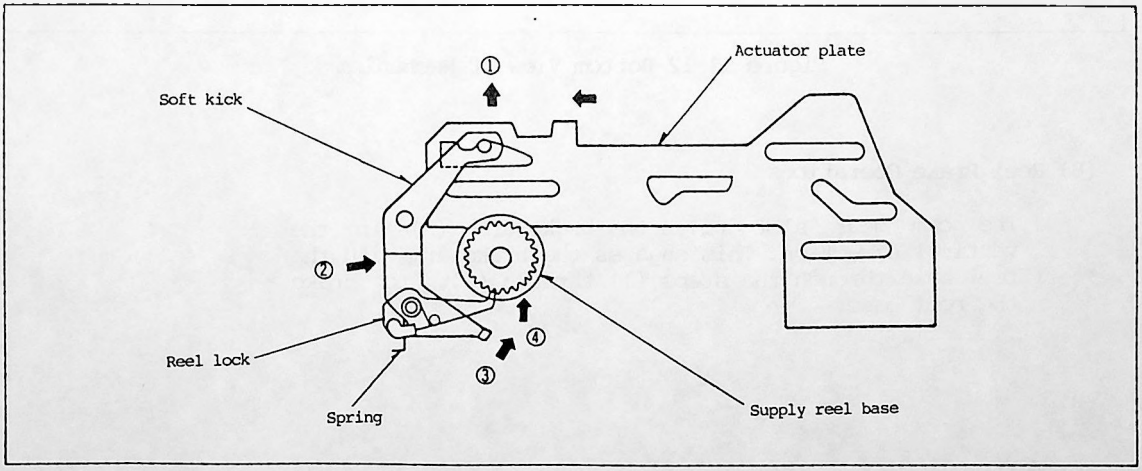


Figure 11-10 View from the Reel Base Side

(7) Play Idler Operation

The figure below shows a step in the braking sequence.

(a) The actuator plate drives the pulley arm, which then presses the play idler to the take-up reel base and driving gear.

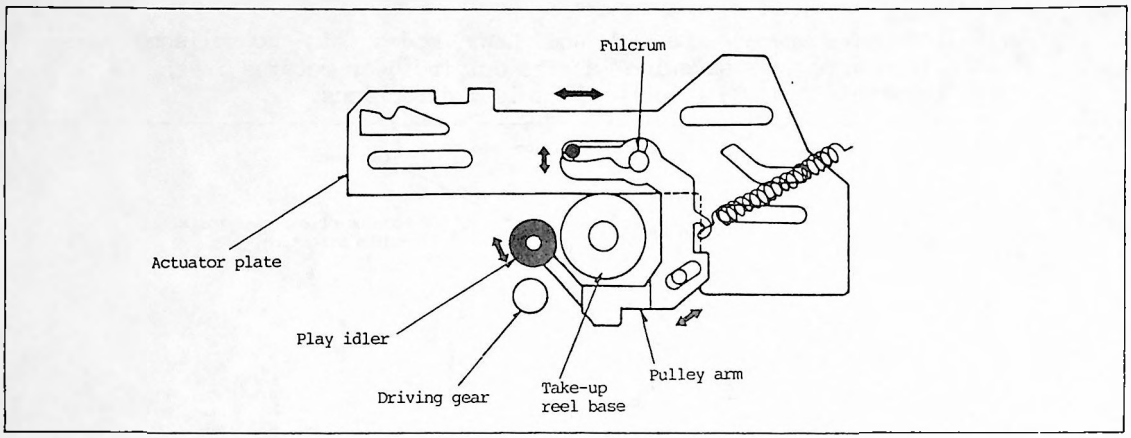


Figure 11-11 View from the Reel Base Side

The following figure shows the play arm actuator shaft (actuator plate) positions for the mechanism modes:

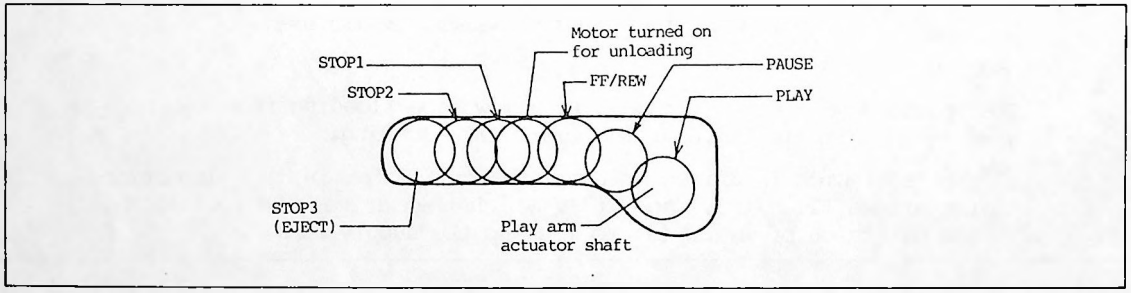


Figure 11-12 Bottom View of Mechanism

(8) Reel Brake Operations

The cam gear slot drives the brake arm (A) in the vertical direction. This engages the brake arm with the reel base through the steps (1) through (5), to brake the reel base.

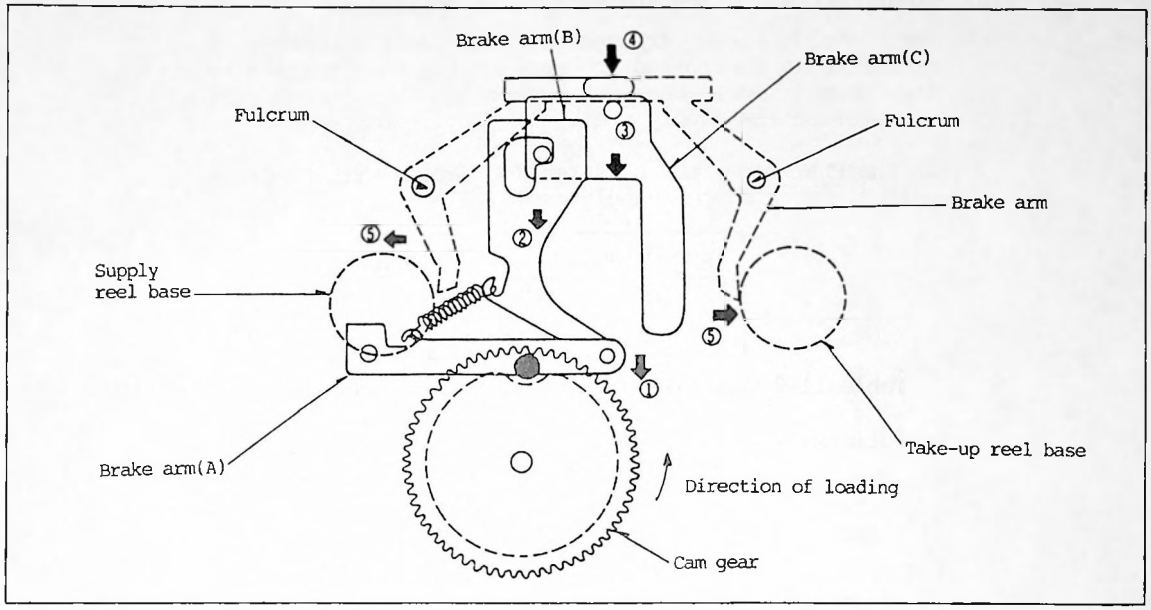


Figure 11-13 Bottom View of Mechanism

(9) Trigger Brake Operations

The trigger brake mechanism applies quick brake to the reel base to prevent tape slack during transition from the FF/REW into STOP mode.

(a) At the top of cam gear's cam, the pin on the brake arm (C) pushes up the trigger arm. As a result, the trigger arm claw is engaged with the intermediate pulley rack, causing only the brake arm (C) to trip in the direction of arrow (6) to apply quick brake to the reel base.

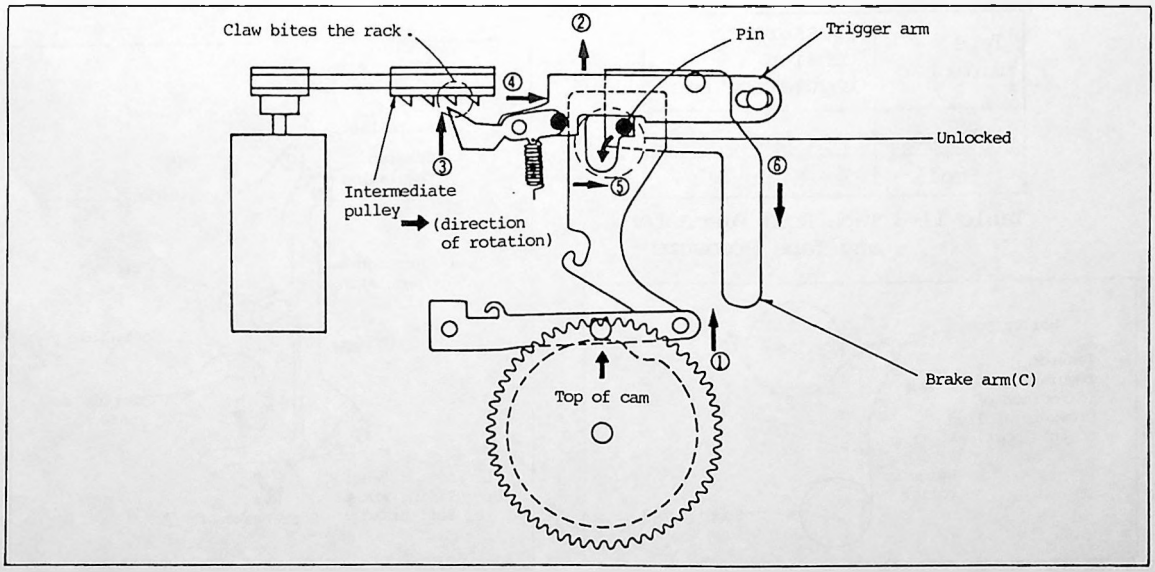


Figure 11-14 Bottom View of Mechanism

(10) Tension Regulator Arm and Soft Brake Operations

For stable tape transport, the soft brake is mechanically controlled to regulate the back tension to the supply reel base by detecting the tape roll diameter on the supply reel.

In the PLAY mode, the back tension varies with the tape roll diameter on the supply reel.

Tape diameter	B.T
Large	Small
Small	Large

Table 11-2 Tape Roll Diameter and Back Tension

Operations

(a) The tape roll diamenter on the supply reel is detected from the tape pressure applied to the tension regulating post shows in figure 11-15.

(b) As the tape roll diameter on the supply reel increases, the pressure on the tension regulating post increases, pushing the post to the left.

(c) The tension regulating arm, linked with the tension regulating post, also moves in the direction of arrow (1) in figure 11-16.

(d) The soft brake, linked with the tension regulating arm at the point enclosed with a dotted circle, swings in the direction of arrow (2).

(e) The soft brake, which is in contact with the supply reel base, is pushed in the direction of arrow (3) to weaken back tension on the tape.

Tape diameter	Pressure to tension regulating post
Large	Low
Small	High

Table 11-3 Tape Roll Diamenter and Tape Pressure

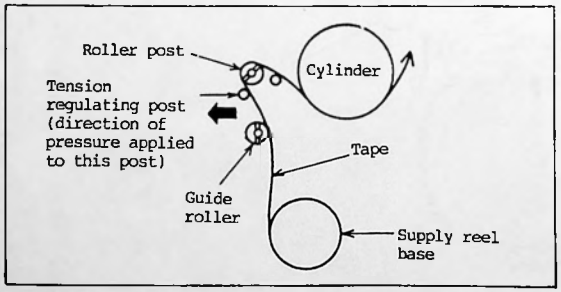


Figure 11-15 Tape Roll Diamenter Detection

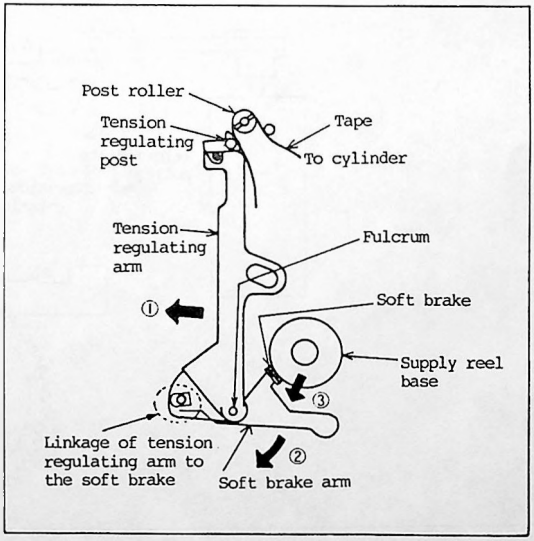


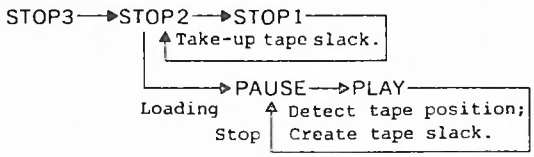
Figure 11-16 Tape Roll Tension Regulation

11–3. Mechanism Mode Transition Timing

The mechanism operation timing is created in the system controlling block. The outputs at pins 28 and 29 of the mechanism CPU (IC-501) control the direction of mode motor rotation.

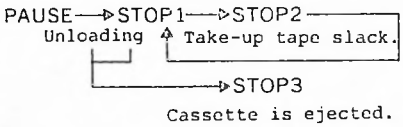
1) **Mode Transition for Cassette Load**

When OPEN/CLOSE button is pressed.



2) **Mode Transition for Cassette Eject**

When OPEN/CLOSE button is pressed in PAUSE mode.



3) **Mode Transition to FF**

PAUSE → FF

4) **Mode Transition to REW**

PAUSE → REW

5) **Mode Transition to PLAY**

PAUSE → PLAY

11–4. Mechanism Operation and States in Different Modes

1) **STOP 3 Mode**

Cassette loading mode:

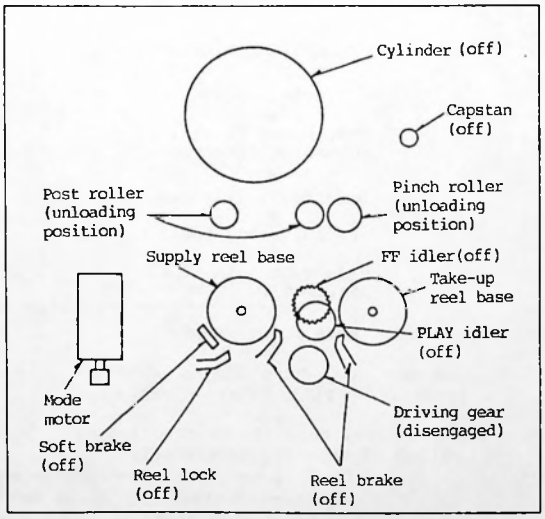


Figure 11-17 STOP 3 Mode

** In the STOP 3 mode, the reel brake, soft brake, and reel lock are all released from the reel bases.

** The FF and PLAY idlers are also released from the reel bases.

** The post roller and pinch roller are in the unloading position.

2) STOP 2 Mode

At a transition from STOP 1 into STOP 2 mode, the mechanism takes up tape slack and winds up the leading section of tape.

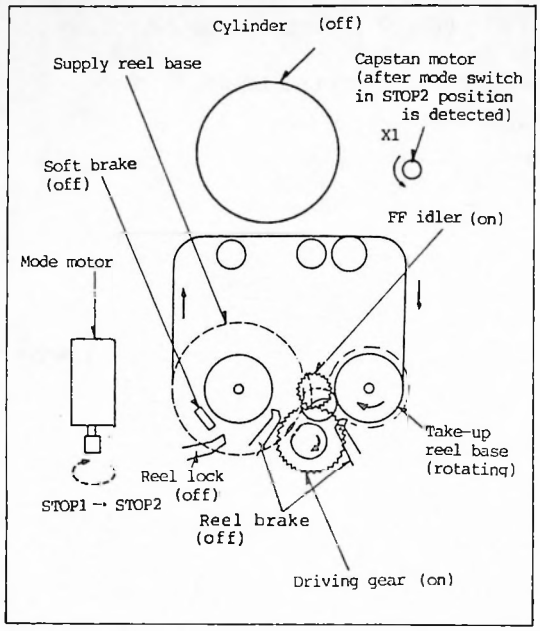


Figure 11-18 STOP 2 Mode

** In the STOP 2 mode, the soft brake and reel lock are released from the reel bases.

** The cylinder remains stationary.

STOP1 mode
↓
Mode motor rotates in unloading direction.
↓
Reel brake released.
↓
FF idler engaged.
↓
Mode switch in STOP2 position is detected.
↓ → Capstan motor starts.
Mode motor stops.
↓
Take-up reel base starts rotation (capstan → PLAY idler → reel base).
↓
* Supply reel base starts rotation pulled by tape (FG generates).
↓ → Capstan motor stops after FG is detected.
Mode motor rotates (in loading direction).
↓
Trigger brake applied.
↓
FF idler released.
↓
Mode switch in STOP1 position is detected.
↓
Mode motor stops.
↓
STOP1 mode

3) STOP 1 Mode

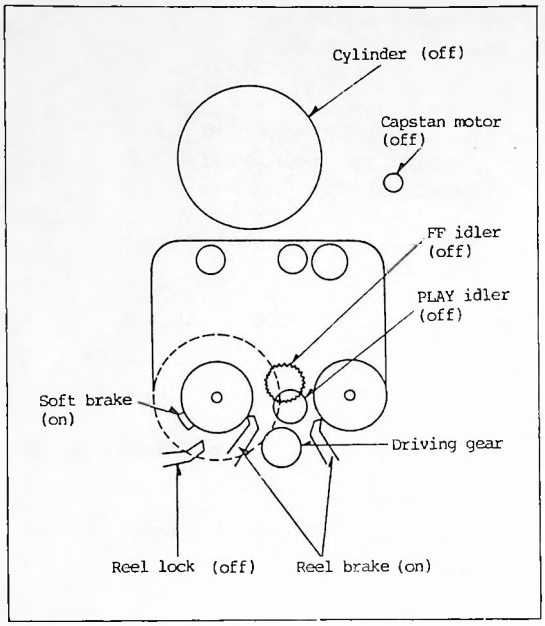


Figure 11-19 STOP 1 Mode

** In the STOP 1 mode, the reel and soft brakes are applied to the reel bases.

** The FF and PLAY idlers are released from the reel bases.

4) Loading Operation

Tape loading pick up the tape out of the cassette and wrap it around the cylinder by means of post rollers.

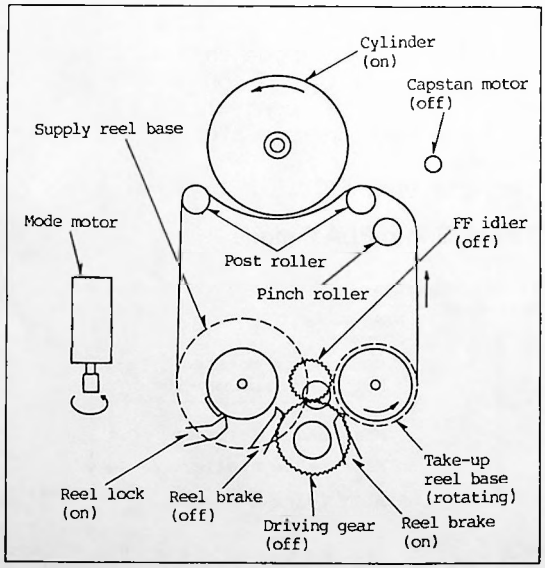


Figure 11-20 Tape LOading

STOP1 mode

Cylinder starts rotation (0 to 2000 rpm).

Mode motor starts (in loading direction).

Reel lock turned on; FF idler engaged; Reel brake off.

Post and pinch rollers are elevated (to pick up tape from the take-up reel).

Mode switch in PAUSE position is detected.

Mode motor stops.

Note: After tape loading is completed, the deck is momentarily placed in the PLAY mode, wherein the tape position is sensed and tape slack is created, then is set back to the PAUSE mode.

** During tape loading, the supply reel is locked up by the reel lock.

** The FF odler is engaged with the during gear (but remains stationary)

** The soft brake is applied to the reel base, and the PLAY idler is released.

5) PAUSE Mode

The tape stops in the PAUSE mode just after tape loading is completed or the deck has exited the FF, REW, or PLAY mode.

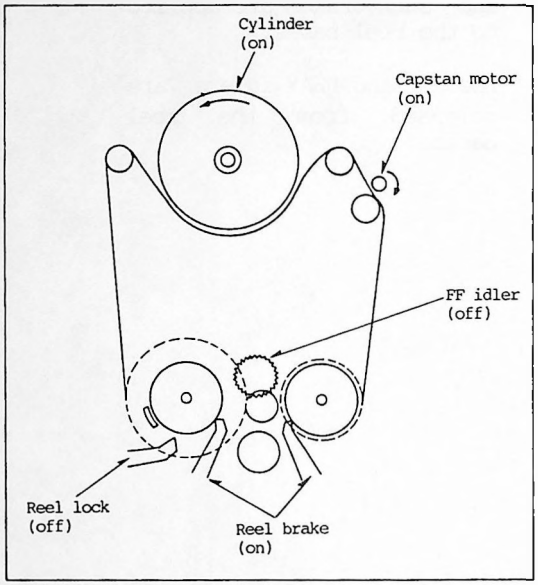


Figure 11-21 PAUSE Mode

** In the PAUSE mode the pinch roller is disengaged from the capstan.

** The cylinder rotates at 2000 rpm.

** The capstan rotates at the normal (x1) speed.

** The soft brake, reel lock, PLAY idler, and FF idler are all in released position.

** The reel brake is applied.

6) PLAY Mode

In the PLAY mode the tape is driven at a constant speed by the pinch roller and capstan.

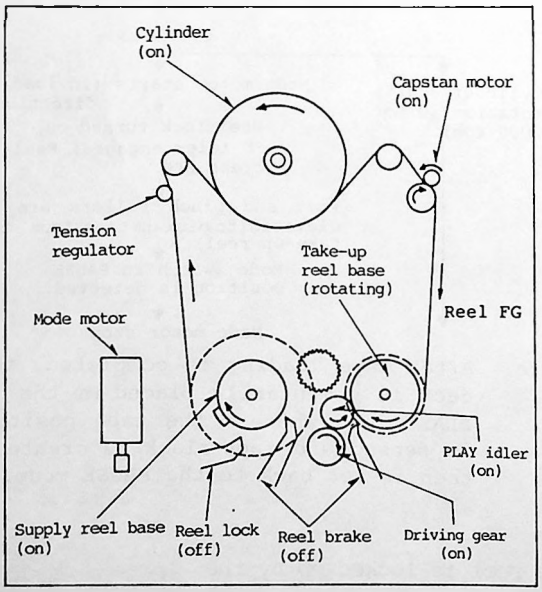
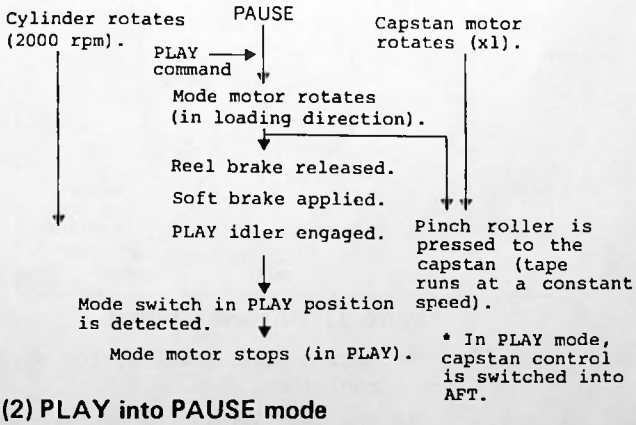


Figure 11-22 PLAY Mode

** In the PLAY mode the soft brake is turned on (back tension is controlled by the tension regulator).

** The PLAY idler is engaged.

(1) PAUSE into PLAY mode



(2) PLAY into PAUSE mode

The mode motor rotates in the unloading direction to the PAUSE mode position.

7) FF Mode

In the FF mode, the FF idler directly drives the reel base. Other mechanism remain in the PAUSE mode.

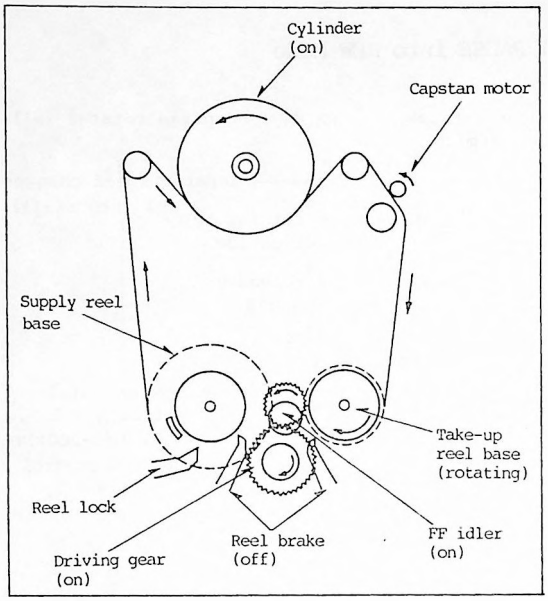
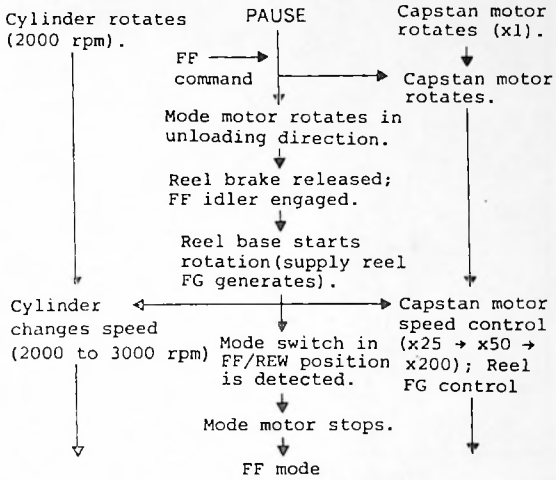


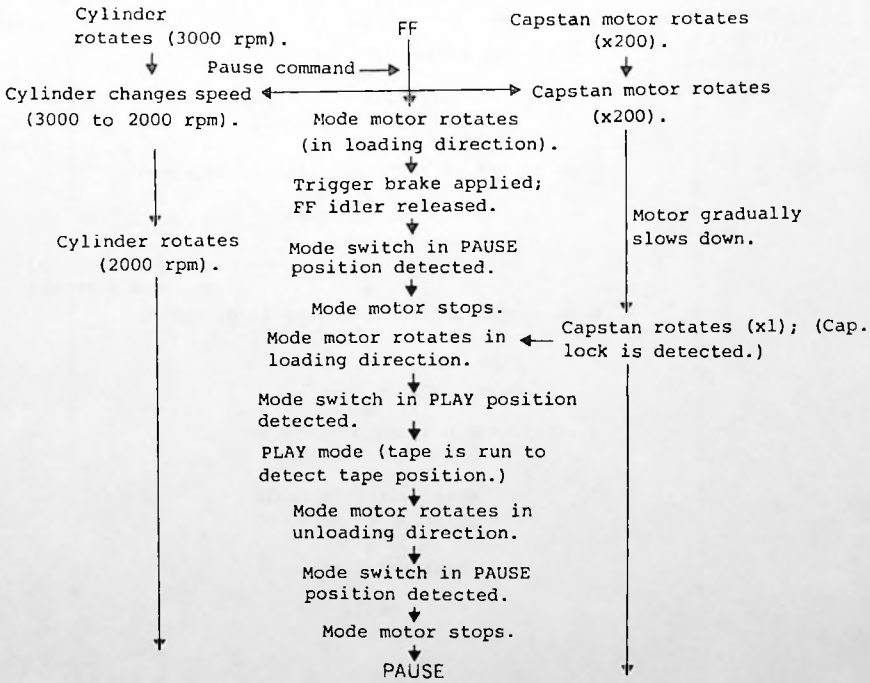
Figure 11-23 FF Mode

(1) PAUSE into FF Mode



(2) FF into PAUSE Mode

For transition from FF into the PAUSE mode, the mechanism first goes into the PAUSE mode, then temporarily into PLAY mode (where the tape position is detected), and finally into the PAUSE mode.



8) **REW Mode**

In the REW mode, the FF idler directly drives the reel base. Other mechanism including the pinch roller are in the PAUSE mode.

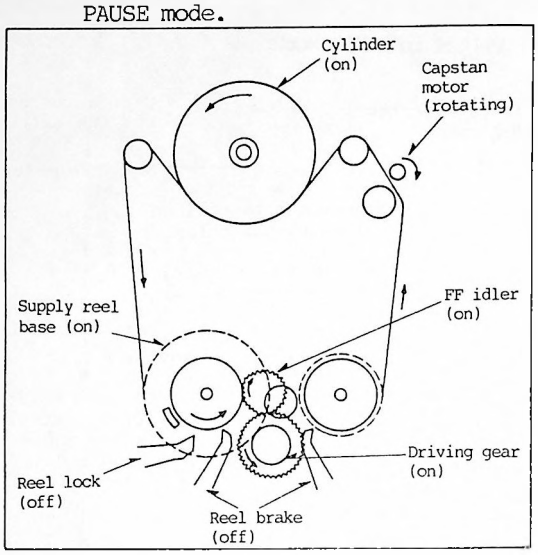
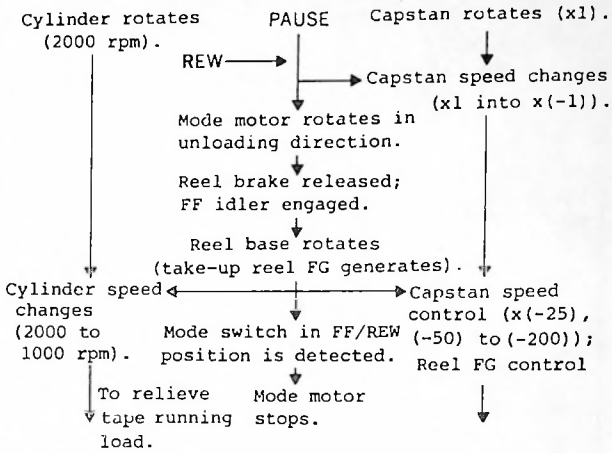


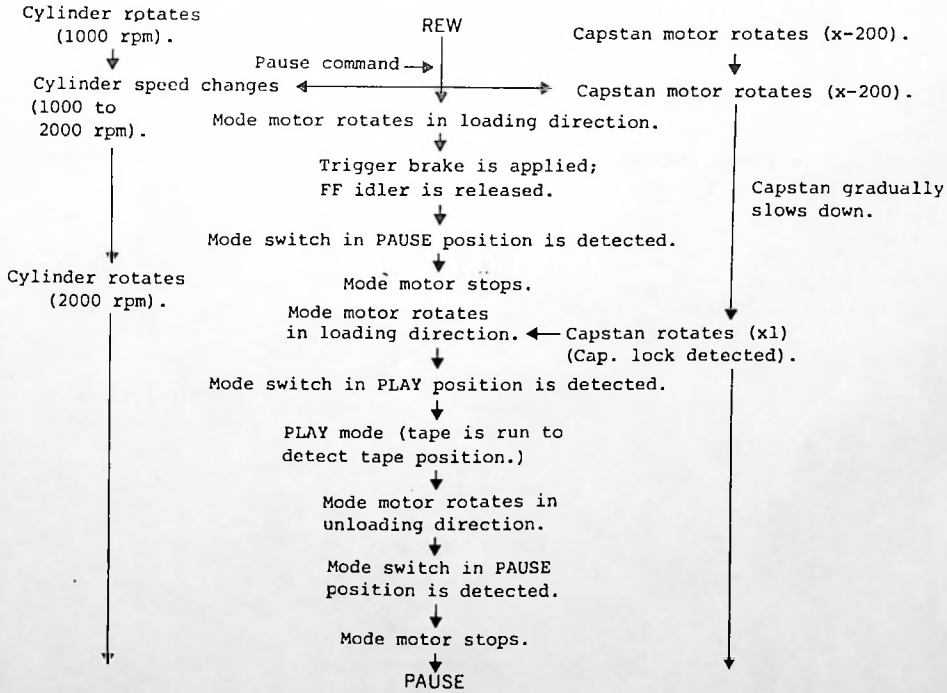
Figure 11-24 REW Mode

(1) PAUSE into REW Mode



(2) REW into PAUSE Mode

For transition from the REW into PAUSE mode, the mechanism first goes into the PAUSE mode, then temporarily into the PLAY mode (where the tape position is detected), and finally into the PAUSE mode.



9) Unloading Operation

For tape unloading, the post and pinch rollers are repositioned to the unloading position and the tape is taken up into the cassette.

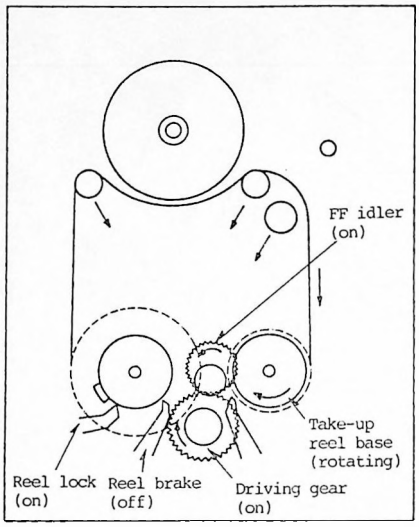
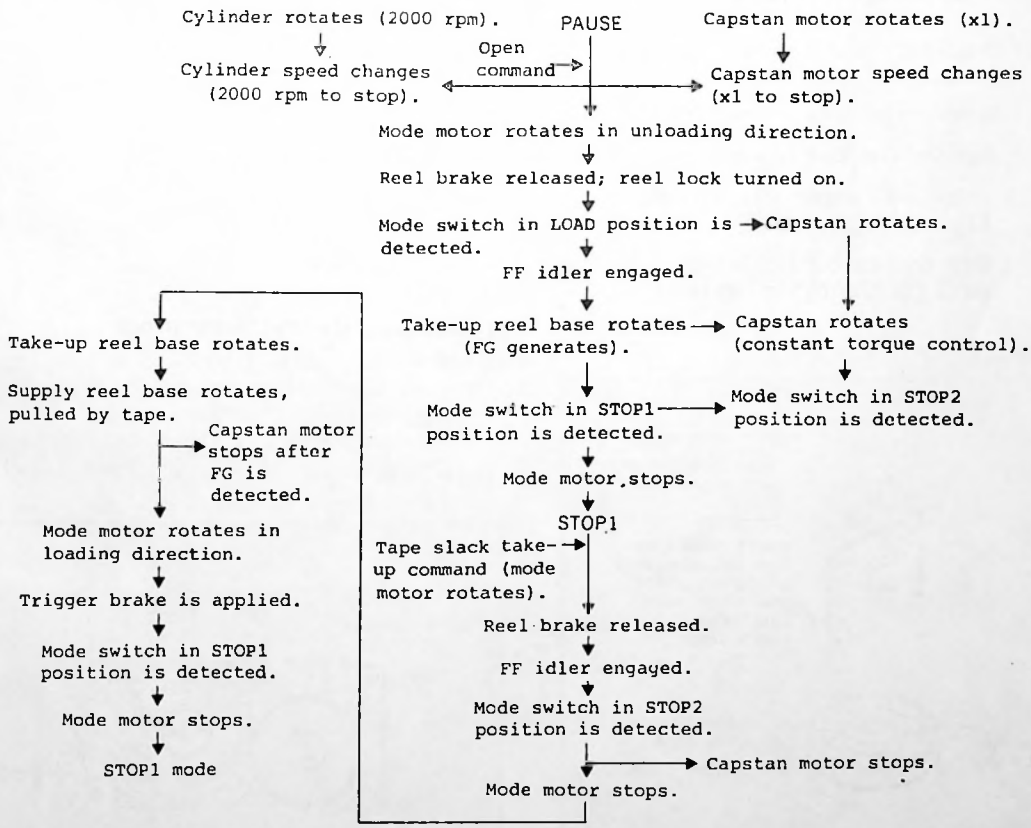


Figure 11-25 Unloading Mode

** During unloading the supply reel is locked up by the reel lock.

** The FF idler is engaged.

** The play idler and reel brakes are released.



11–5. Upper Cylinder Head and Cyliner Block Replacement and Alignment Procedure

1) Replacement

(1) Removing the Upper Cylinder

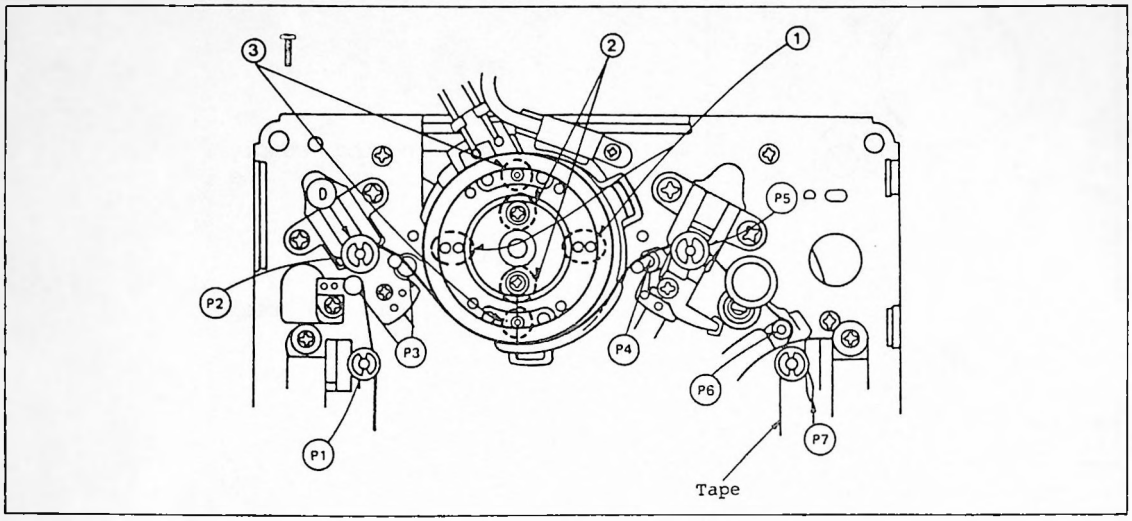


Figure 11-26 Upper Cylinder Head and Cylinder Block Replacement and Alignment

(a) Desolder the head terminals and disconnect the leads.

(b) Remove the two screws retaining the upper cylinder.

(c) Remove the two hexagon socket head screws.

(d) Using a paper clip, make a fixture as shows in figure 11-27.

(e) Put the fixture's hooks into the cylinder holes and pull up the cylinder head.

(2) Removing the Cylinder Block

(a) Remove the grounding lead screw (1).

(b) Remove the three screws (2), (3), and (4) retaining the cylinder.
(These screws should be retightened in the order of (2), (3), and (4).)

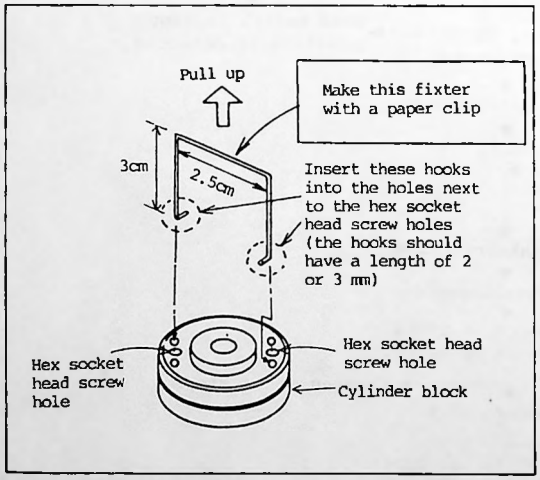


Figure 11-27 Cylinder Block Removal Fixture

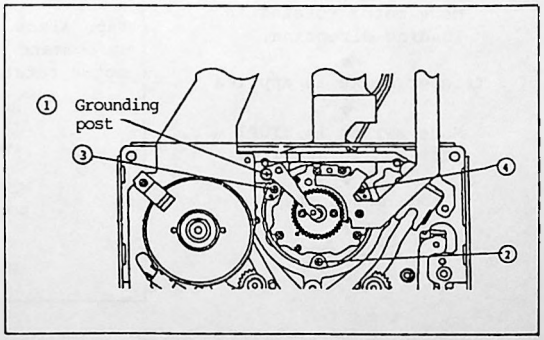


Figure 11-28 Cylinder Block Removal

2) Check and Alignment after Replacement

(1) Checking Tape Transport

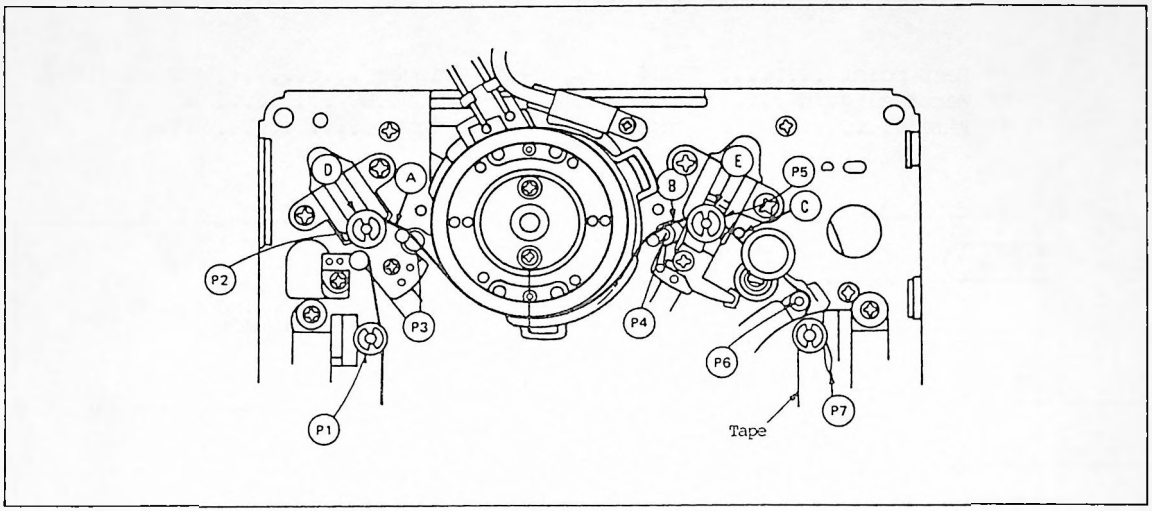


Figure 11-29 Checking Tape Transport

Check the tape at points (A), (B), and (C) in the figure above by alternately putting the deck in the PLAY and STOP modes, and verify that the top and bottom edges of the tape are free from creases.

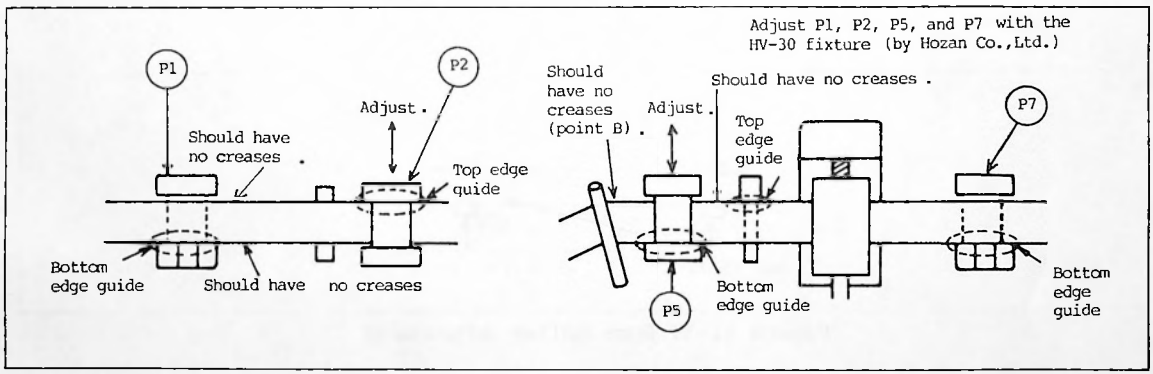


Figure 11-30 Top and Bottom Checks

(2) Checking Envelope Waveform

The head picks up data of the tape while the cylinder rotates 90 deg. If the tape wrapping angle to the cylinder is less than 90 deg., the leading or trailing shoulders of the read signal envelope will round. A similar symptom may also occur if the tape is lifted off the head surface due to poor tape transport.

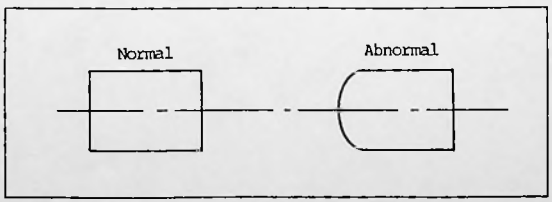


Figure 11-31

Set up the oscilloscope with the following settings and observe the read signal envelope:

** Test point TP804
** Vertical gain ..... 20 mV/Div.
** Time ..... 5 ms/Div.
** Trigger ..... Normal (CH-2)
** AC.GND.DC ..... AC
** Delay ..... None

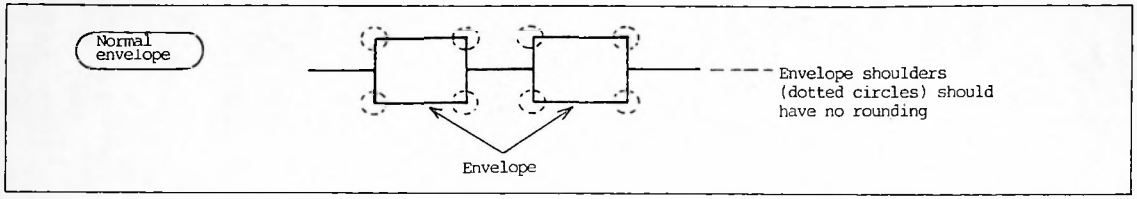


Figure 11-32 Normal Envelope

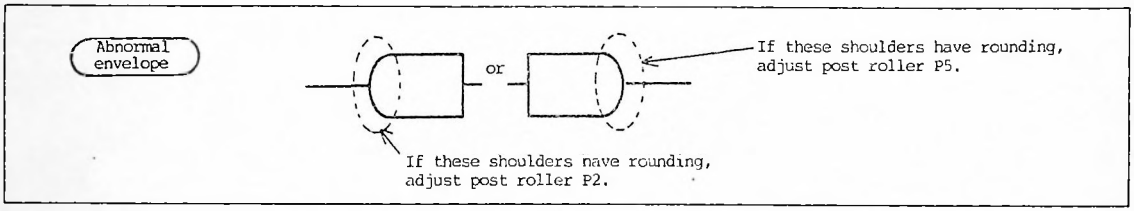


Figure 11-33 Abnormal Envelope

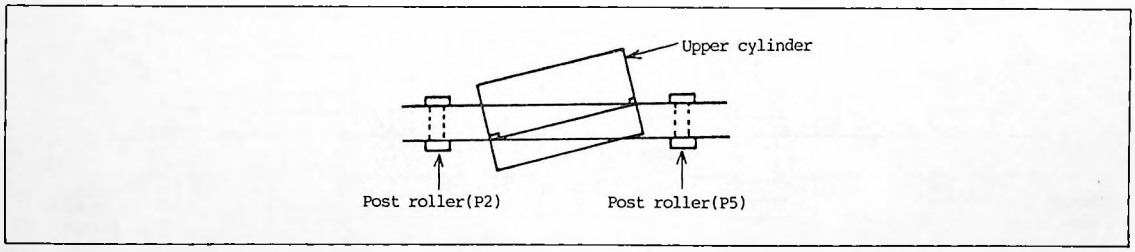


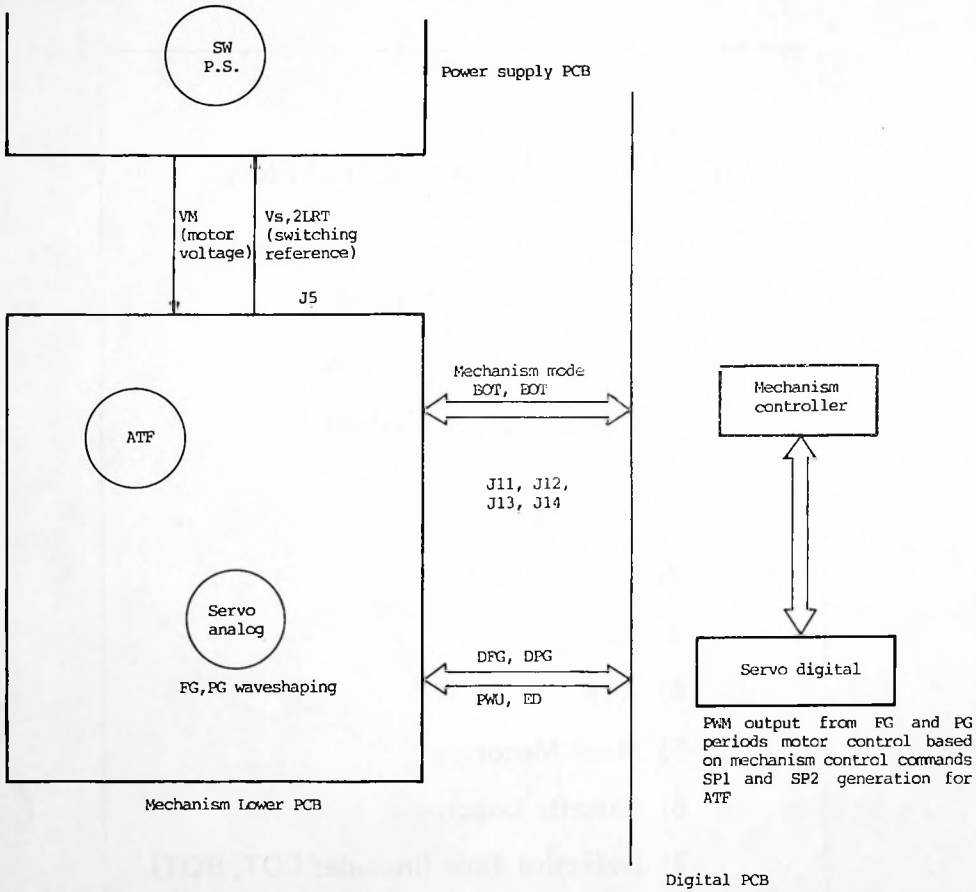
Figure 11-34 Post Roller Adjustment

12. Troubleshooting Manual

1. PC Board Layout: Signal Flow
2. Block Diagram
3. General Power-On Flow
4. Detailed Power-On Flow
5. Troubleshooting Manual

    1) Capstan
    2) Cylinder
    3) Reel
    4) ATF
    5) Mode Motor
    6) Cassette Loading
    7) Defective Tape (includes EOT, BOT)

1. PC Board Layout: Signal Flow



2. Block Diagram

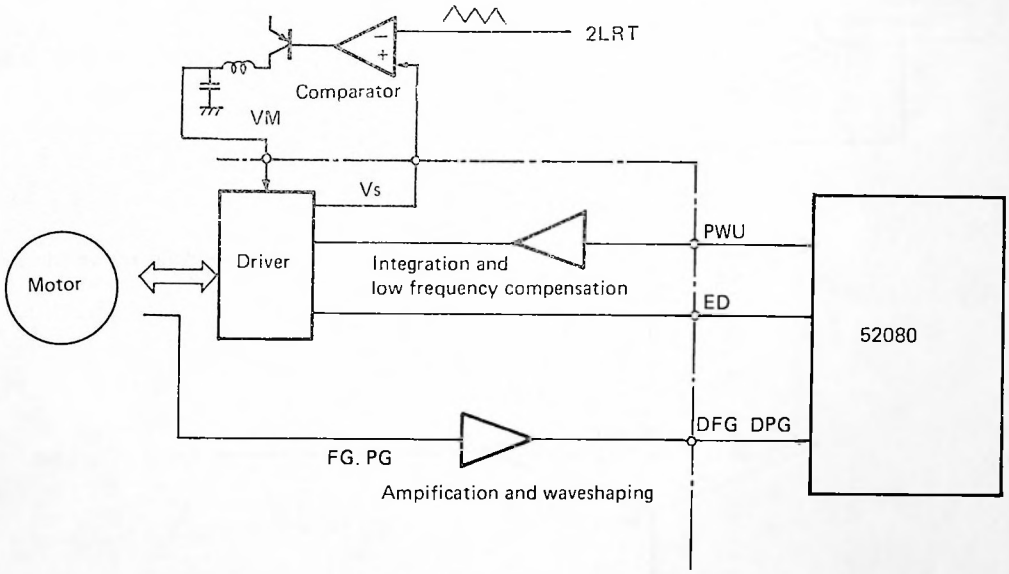
Mechanism control is roughly divided into two types:

1) Mode motor control which controls the mechanism mode.

2) Capstan and cylinder motor control which controls tape transport.

The control in 1) simply rotates the mode motor until the desired mode is obtained. It is not a complicated process.

The control in 2) is represented as a block diagram below.



Motor Control Loop

** FG and PG which are output from the motor are amplified, waveshaped and sent to the digital section.

** The PWM and ED (forward/reverse/stop) signals are generated digitally from DFG and DPG, based on commands from the mechanism control circuit, and output to the analog section.

** The PWM and ED signals are interfaced and sent to the motor driver.

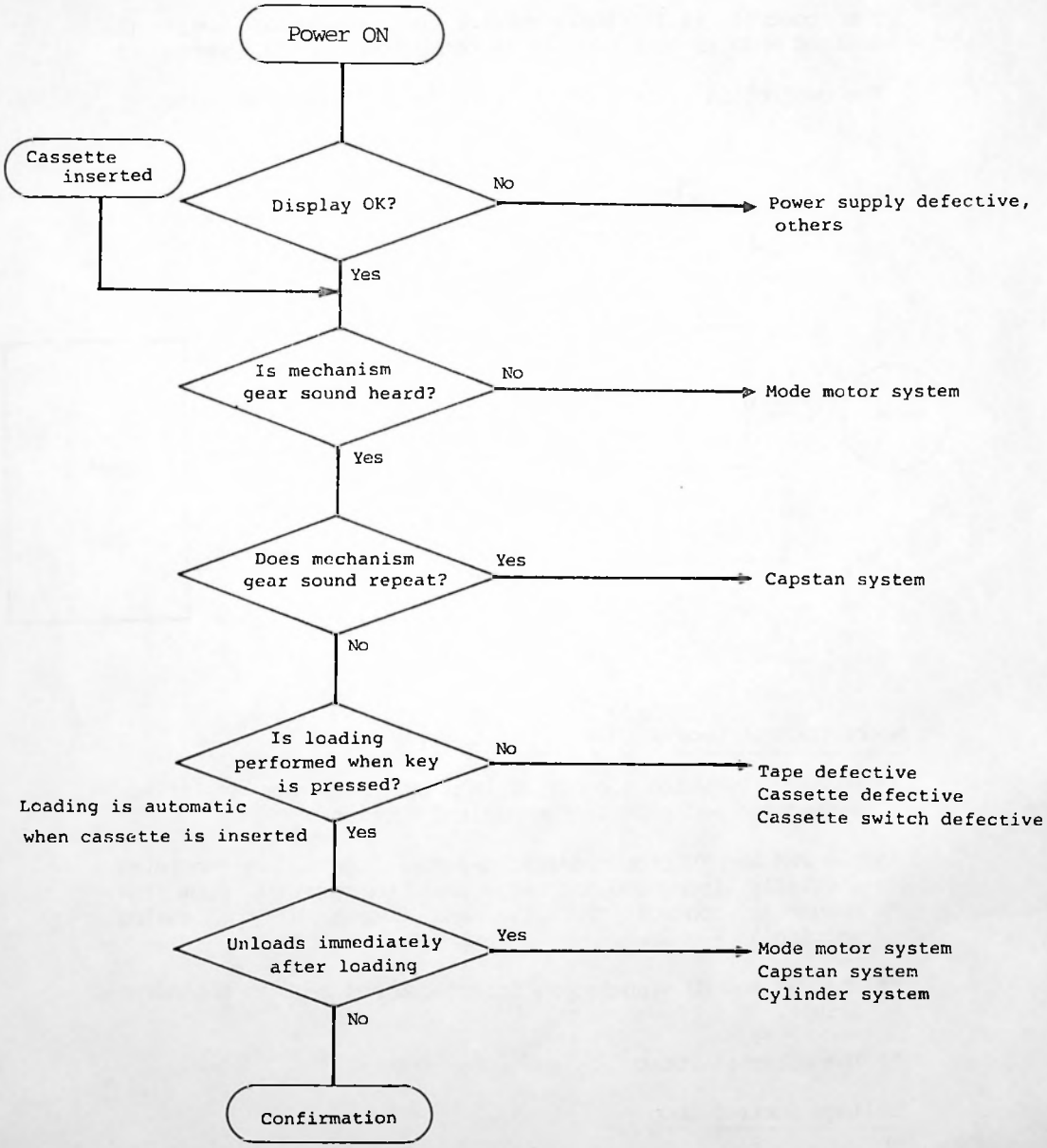
** The motor is rotated by the motor driver.

Voltage Control Loop

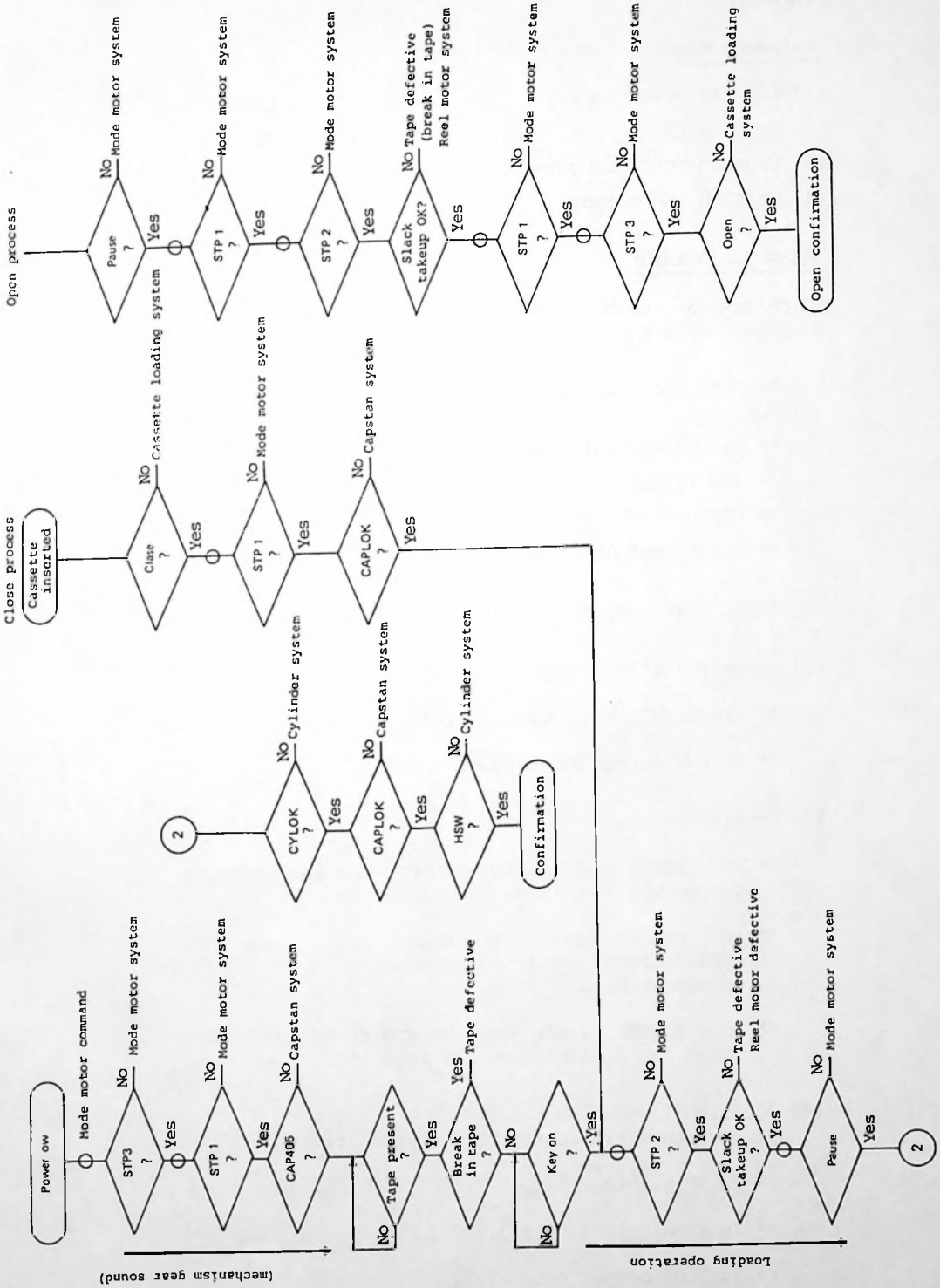
** With respect to V, the counter emf which is generated in proportion to the speed of the motor, Vs varies so that VM = Va + Vce (sat) if satisfied.

3. General Power-On Flow

The mechanism and servo system can be considered 90% operational if 50% of loading is completed at power-on initialization (a sound is heard when the mechanism gear operates).
The general flow is shows below.



4. Detailed Power-On Flow



5. Troubleshooting Manual

1) Capstan

Relevant Signals

(1) Capstan power supply	CAVM, CAVS, 2LRT
(2) Capstan FG	CADFG1, CADFG2
(3) Capstan rotation command	CAPED
(4) Capstan PWM output	PWMCAP

Types of Trouble

There are 3 types of motor trouble: no rotation, uncontrollable rotation and erratic rotation.

(1) No Rotation (if all items OK, check mechanism lower PCB)

** Is the mechanism locked?

** VM= 12 V?

** CAPED= 5 V?

** Is PWM output at acceleration? 2.5V

** Is 2LRT output? 3.5V 1.5V

(2) Uncontrollable Rotation

** Are CADFG1 and CADFG2 output? 324Hz 2.5V

** Is PWM output at deceleration?

(3) Erratic Rotation

** Are CADFG1 and CADFG2 output when the cassette is removed and rotated by hand?

** Is PWM output abnormal? (e.g. repeated deceleration and acceleration or full deceleration).

** Does CAPED match the direction of rotation? (high for forward, low for reverse).

(4) Occasional Stopping
(temperature rise portection of the driver)

** Is VM within 2.5 to 5 V?.

** Is VS within 1.5 to 3.5 V?.

** Is 2LRT output properly?.

2) Cylinder

Relevant Signals

(1) Cylinder power supply	CYVM, CYVS
(2) Cylinder FG, PG	CYDFG, CYDPG
(3) Cylinder rotation command	CYLED
(4) Cylinder PWM output	PWMCYL
(5) HSW, OROT2	

Types of Trouble

(1) No Rotation

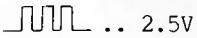
** Is the mechanism locked?

** VM= 12 V?

** VS= 2.5 V +- 1 V?

** CYLED= 5 V?

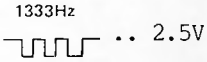
** Is PWM output at acceleration?



(2) Uncontrollable

** Is CYDFG output?

** Is PWM output at deceleration?



(3) Erratic Rotation

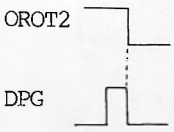
** When rotated by hand, is CYDFG output properly in proportion to the rotation (duty 50:50)

** Is PWM output abnormal?
(e.g. repeated deceleration and acceleration)

** CYLED= 5 V?

(4) No Phase Lock (CYLOKo is sometimes high)

** Is CYDPG output properly?
30Hz



(5) No HSW Output

** Are CYDFG and CYDPG output?

(6) Occasional Stopping
(temperature rise portection of the driver)

** Is VM within 3 to 6 V?

** Is VS within 1.5 to 3.5 V?

** Is 2LRT output properly?

3) Reel

Except for supplying the FG signal from both reels, the analog section for the reel is the same as that for the capstan (including the drive system).
Thus, only the items below need be checked.

Relevant Signals

(1) Reel FG ..... RLDFGT. RLDFGS
(2) Unloading torque command ... RLTLK, TL

Types of Trouble

(1) Trouble during loading (e.g. continuous slack takeup, etc).
** Is the reel FG output?

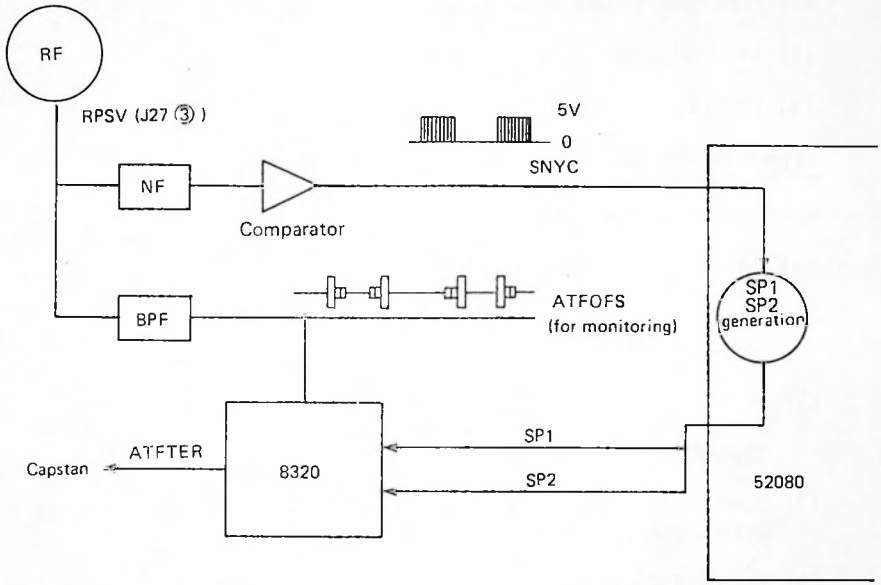
(2) During unloading, the tape suddenly returns back into the cassette.

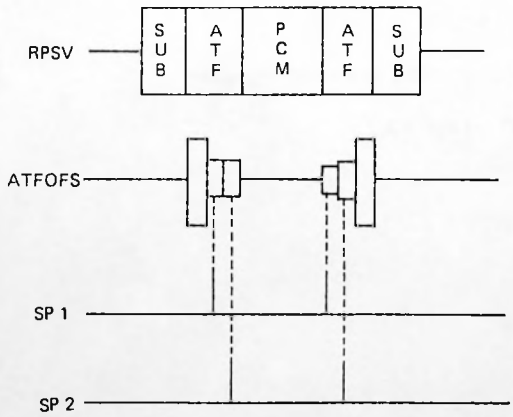
** Is TL low?
** Does RCTLK change?

(3) Uncontrollable during FF/REW (time code can't be read)
** Is the reel FG output?

4) ATF

The ATF is the control signal used to keep the head on-track during playback. The pilot signal from the RF circuit is sliced with the SYNC signal and then controlled by the servo.





The difference of the ATFOFS sampled by SP1 and SP2 is output to the capstan as ATFTER.

Relevant Signals

(1) REC/PLAY switching signal ..... SRVDL

(2) Sampling pulse SP1, SP2

(3) SYNC signal ..... SYNC

(4) ATE offset signal ..... ATFOFS

Types of Trouble

Griding sound is emitted during playback.

(1) Is the tape OK? (is the same sound heard at the same location on the tape?)

Check for scratches.

(2) Is the cassette inserted properly?
Is there any foreign matter or paper stuck to the cassette?

(3) Does the envelope flow? The p-p value changes erratically.

(4) Is ATFOFS output?

(5) Is the SYNC signal output?

(6) Are SP1 and SP2 output with correct timing?

(7) Is SRVDL low during playback?

5) Mode Motor

Trouble relating to mode transition of the mechanism is discribed.

Relevant Signals

(1) Mode motor power supply ..+7.6V & BA6238A (digital PCB)

(2) Mode motor command .....MDMR (+) (-)

(3) Mode motor output .....MMOD ϕ - 2

Types of Trouble

(1) No mode transition

** Is the mode motor power supply 7.6 V?
** Is the BA6238A output voltage OK?
** Are MDMTR+ and MDMTR- OK? (includes direction of rotation)
** Is the mechanism locked?

(2) Mode motor does not stop due to overrun.

** Direction of rotation for MDMTR+ and MDMTR- OK?
** Does the mode motor output change properly?

6) Cassette Loading

Relevant Signals

(1) Cassette loading motor power supply ...+7.6V & BA6238A (digital PCB)

(2) Cassette loading motor command .....CLDMTR -, +.

(3) Open signal

(4) Close signal

(5) Cassette Hall signal ..... TH1 - 6

Types of Trouble

(1) Open/Close key inoperable

** Is the power supply 7.6 V?
** Command CLDNTR-, CLDN4MTR+ OK?

** Are command output from the mechanism control circuit to BA6238A and HC157?

(2) Mechanism does not operate even if close, open immediately.

** Is the close switch on?
If OK, check the mode motor?

(3) Closes immediately even if opened.

** Is the open switch on?

(4) After the cassette is inserted, operation of the mechanism gear is heard but the cassette is not loaded.

** Are the states (ON/OFF) of TH1 - 6 correct?

7) Defective Tape

The following items are possible causes of a defective tape

(1) Brake in the tape.

(2) No operation, or excessive load, due to tangled tape.

(3) Reel lock due to defective cassette tape transparency.

(4) Faulty transport due to damaged tape.

(5) Abnormal operation due to improper tape transparency.

** Leader tape transparency is low so that EOT and BOT can't be detected.

** Magnetic tape transparency is high so that EOT and BOT continues to be defected.

The mechanism may also be at fault for (5). Check the following points.

** Are the LEDs for EOT and BOT on?

** Turns on/off when the light path is blocked?

** Out of adjustment? (VR202,VR203).

13. Adjustment Manual

1. PG Phase Adjustment
2. Equivalent Circuit Adjustment
3. ATF Gain Adjusment
4. RF Recording Level Adjustment
5. Playback PLL Adjustment
6. Playback Adjustment
   1) DAC Output Balance
   2) DAC Offset Adjustment
7. Recording Adjustment
   1) ADC Offset Adjustment
   2) ADC MSB Adjustment
8. Tape Begin/End Detection Sensitivity Adjustemnt

Electrical Adjustment

Equipment and Tools

** 2-channel 30 MHz oscilloscope (with external trigger and delay sweep and with a 10 : 1 probe).

** Standard electrical tools and equipment.

** Electrical adjustment screw driver ...SZZP1043C

** Standard test tapes.....RD-PG01 (PG reference)
.....RD-ER01 (error rate)

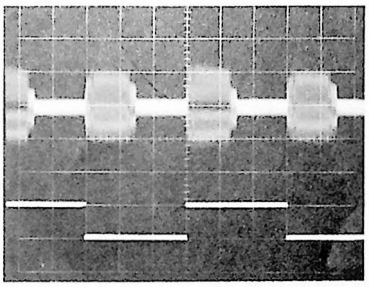
** Blank tape for recording and playback.
(commercially available blank tape)

1. PG Phase Adjustment

1. Play the PG reference standard test tape (RD-PG01).

2. Set up the oscilloscope and connect as shows below.

	CH-1	CH-2
Test Point	J27(3) (RPSV)	J102(14) (OROT2)
Volts/Div.	20 mV	0.5 V
Time/Div.	5 msec	
Delay	50 usec	
Trigger	CH-2	
AC.GND.DC	AC	DC
Adjustment Point	VR201	



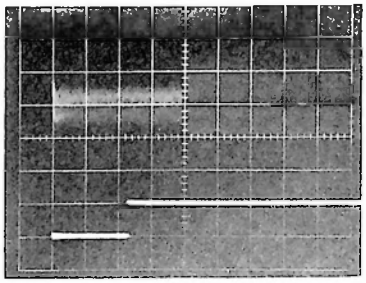
Note: TP624 is ground.

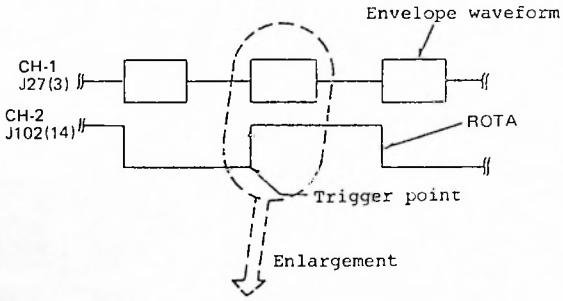
3. After set up, the waveform shows on the right appears.

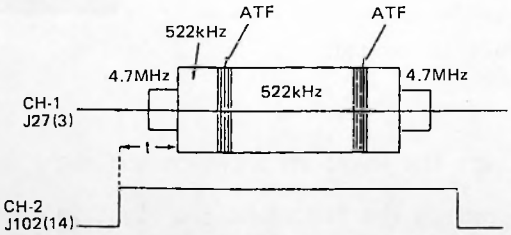
4. The waveform in the figure on the right is enlarged using the delayed sweep. The point where the delayed sweep is used to enlarge the waveform is the leading edge of the CH-2 (OROT2) waveform.

   The delayed sweep is 50 μsec.

5. Rotate VR201 (located on the mechanism board) and adjust the time ("t" in the figure below) from the leading edge of the waveform of CH-2 to the leading edge of the 522 KHz waveform of CH-1 so that it is within ± 0.04 msec of the time indicated on the label on the standard tape (e.g. 0.183 msec).







t: Value (msec) indicated on the standard tape ±0.04 msec.

2. Equivalent Circuit Adjustment

1. Play the error rate measurment standard test tape (RD-ER01)

2. Set the timer switch on the play position. Then, while holding down the "recall" button, turn on the power switch. (Plays the error measurement tape using timer playback) In this mode, the error rate is displayed on the tape counter whenever the "recall" button is pressed.

   The adjustment is correct if the error rate value is 100 or lower. If this value continues to be above 100, proceed to step 3. (Display range is from 0000 to 9999).

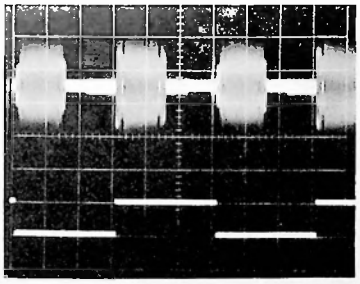
3. While viewing the error rate, adjust VR356, VR355 and VR354 a little at a time to reduce the error rate. (Target value : 50 or lower)

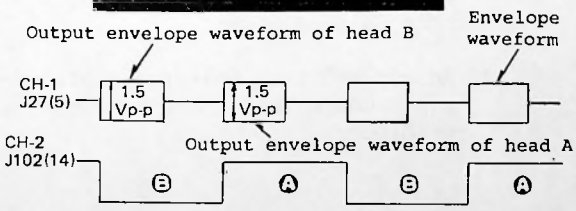
   Note:
   (1) It takes about 2 seconds for the result of the adjustment of VR354 - VR356 to be displayed.
   (2) If the error rate con't be lowered below 100, check the points below.
      a) Dirty head, clogged head, disconnected head, etc.
      b) Defective tape transport (dirty tape, uneven winding, etc).
      c) Other electrical adjustment defects (PG adjustment)
      d) Routing of the head leads (check if they are picking up induced noise).

If the error rate can't be reduced to the target value after the adjustments above have been performed, perform the adjustments of step 4. After completing this, repeat step 1 - 3.

4. Set up the oscilloscope and connect as shows below.

	CH-1	CH-2
Test Point	J27(5) (RPRF)	J102(14) (OROT2)
Volts/Div.	50 mV	0.5 V
Time/Div.	5 msec	
Delay	-	
Trigger	CH-2	
AC.GND.DC	AC	DC
Adjustment Point	VR356	VR355





As shows above, when the waveform of CH-2 (OROT2) is low, an envelope waveform is output from head B. On the other hand, the envelope waveform from head A is output when CH-2 is high.

5. After set up, the waveform shows on the right appears.

6. Adjust VR356 so that the amplitued of the output envelope waveform of head A is 1.5 V p-p.

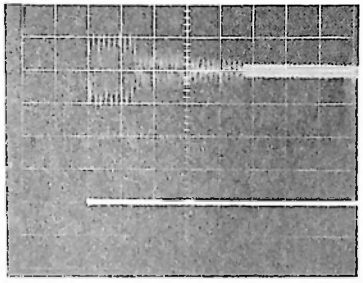
7. Adjust VR355 so that the amplitude of the output envelope waveform of head B is 1.5 V p-p.

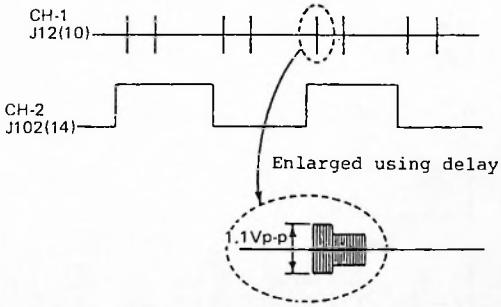
3. ATF Gain Adjusment

1. Play the error rate measurement standard test tape (RD-ER01)

2. Set up the oscilloscope and connect as shows below.

	CH-1	CH-2
Test Point	J102(9) (ATFOFS)	J102(14)
Volts/Div.	50 mV	0.5 V
Time/Div.	5 msec	
Delay	50 µsec	
Trigger	CH-1	
AC.GND.DC	AC	DC
Ajustment Point	VR321	





3. Monitor about 8 lines of the ATF waveform. Select the line with the largest amplitued and enlarge it using the 50 µsec delayed sweep.

4. Adjust VR321 so that the amplitude of the waveform is 1.0 V p-p. Check that the other smaller amplitudes are 0.8 V p-p or higher.

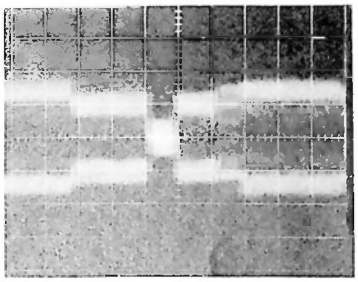
4. RF Recording Level Adjustment

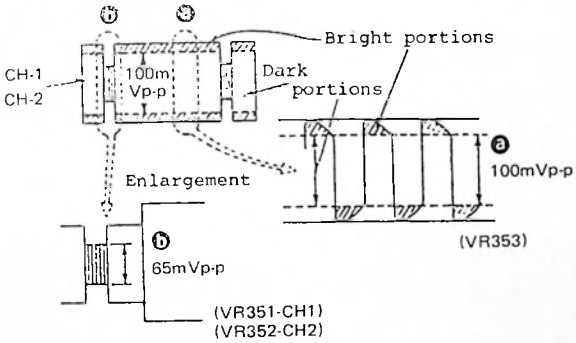
Note: Steps 1-4 are temporary adjustments. If the adjustments are off after performing 5-7 repeat steps 1-7.

1. Load blank tape for recording and set the recorder for "REC-PLAY".

2. Set up the oscilloscope and connect as shows below.

	CH-1	CH-2
Test Point	TP351 J28(2)	TP352 J28(4)
Volts/Div.	5 mV	5 mV
Time/Div.	2 msec	
Delay	0.1 msec	
Trigger	-	
AC.GND.DC	AC	AC
Adjustment Point	VR351	VR352





3. Set the delay time of the oscilloscope to 0.1 msec to enlarge the waveform. Adjust VR351 (CH-1) and VR352 (CH-2) so that "b" in the figure is 65 mVp-p.

4. Next, adjust VR353 so that "a" in the figure is 100 mVp-p.

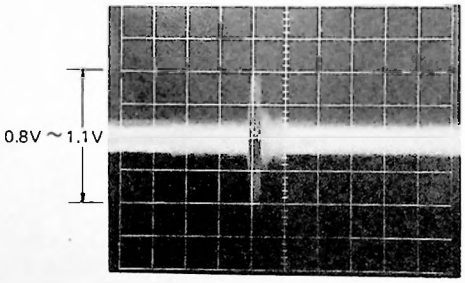
5. Set the oscilloscope and connect as shows below.

	CH-1	CH-2
Test Point	J102(9)	J102(14)
Volts/Div.	20 mV	0.5 V
Time/Div.	2 msec	
Delay	0.2 msec	
Trigger	CH-2	
AC.GND.DC	AC	DC
Adjustment	VR351	VR352
Point	Head A	Head B

6. Record a zero signal (erase) on the blank tape and play back the same portion.

7. The adjustment is correct if the amplitude of the waveform at J12(10) is within 0.8 to 1.1 V.

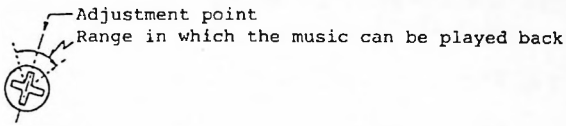
   If not, adjust VR351 for head A (or VR352 for head B). VR351 and VR352 adjust the recording current. After adjustment, record and check by playing back the same portion.



5. Playback PLL Adjustment

1. Load a music tape and set the recorder for "play"

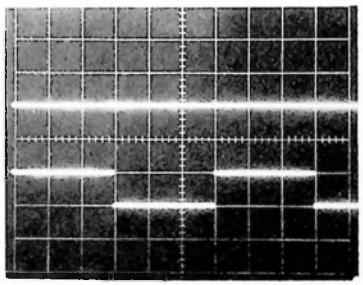
2. Adjust CT170 on the signal processing board to the point where the music can be played back.

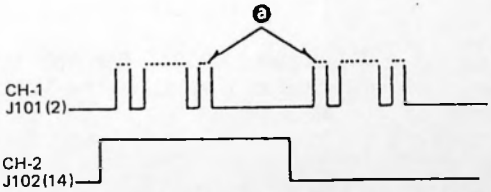


3. After determining the range in which the music can be played back by turning CT170 in the clockwise and counterclockwise directions, set CT170 to the center of the range.

4. Play the error rate measurement standard test tape (RD-ER01). (or , stop a tape already recorded with music and check the waveform at J101(2) (TIDP) in the FF or REW mode)

	CH-1	CH-2
Test Point	J101(2) (TIDP)	J102(14)
Volts/DIV.	0.5 V	0.5 V
Time/Div.	5 msec	
Delay	-	
Trigger	CH-2	
AC.GND.DC	DC	DC
Adjustment Point	CT170	





Note: Fine adjust CT170 for the maximum, number of pulses (appear as dots in "a" in the figure above) during FF or REW at 200 times normal speed (with the speed is the fastest)

6. Playback Adjustment

1) DAC Output Balance

1. Load a blank tape for recording.

2. Use a signal generator to feed a 1 KHz signal to ANALOG IN.

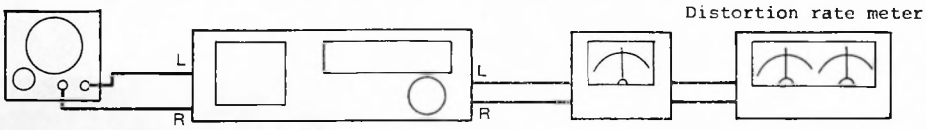
3. Set the recorder to the record mode and adjust INPUT VR so that the level meter moves to -20 dB.

4. Record the -20 dB signal.

5. Rewind the recorded portion and play it back.

6. Adjust VR501 (left chennel) and VR502 (right channel) to minimize the distortion rate. (reference distortion rate of about 0.05%).

7. After adjustment, check that the playback output is -20 dB ± 0.2 dB with respect to 0 dB at 1 KHz.

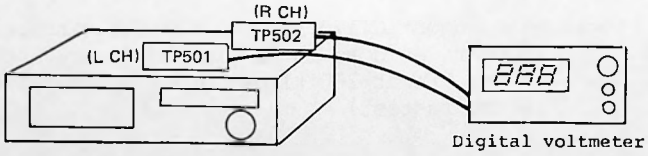


2) DAC Offset Adjustment

1. Set the recorder to DIGITAL IN in the stop mode. (no digital signal input).

2. Connect a digital voltmeter to TP501 for the left channel (TP502 for the right channel).

3. Adjust VR503 for the left channel (VR504 for the right channel) so that the voltage at the point above is 0 ± 0.1 mV.



7. Recording Adjustment

1) ADC Offset Adjustment

1. Set the recorder to ANALOG IN in the stop mode. (no analog signal input).

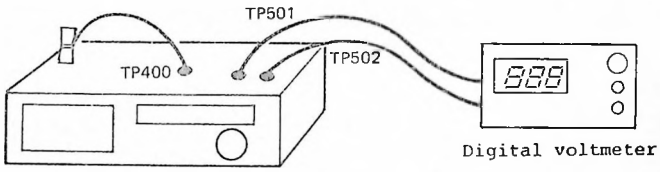
2. Connect TP400 to ground.

3. Connect the digital voltmeter to TP501 for the left channel (TP502 for the right channel).

4. Adjust VR401 for the left channel (VR402 for the right channel) so that the voltage at the point about is 0 ± 0.5 mV.

5. Disconnect TP400 from the ground, leave it floating.

6. Check that the voltage at TP501 and TP502 is 0 ±4 mV.

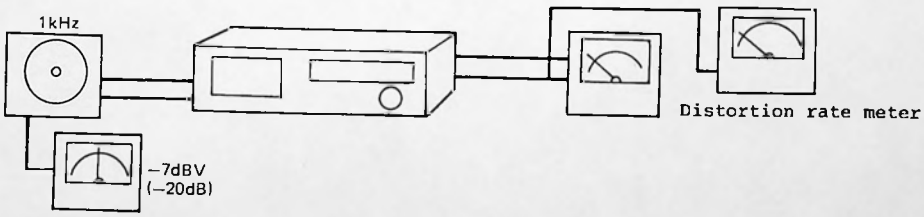


2) ADC MSB Adjustment

1. Use a signal generator to feed a 1 KHz, -7 dBV (0.45 V) signal to ANALOG IN.

2. Adjust VR403 (left channel) and VR404 (right channel) for a minimum distortion rate at the monitor outputs of ANALOG OUT. (reference distortion rate of about 0.01% or lower).

3. Lower the input level by 20 dB and check that the output level drops to -20 dB ±0.3 dB from 17 dBV (0.45 V).



8. Tape Begin/End Detection Sensitivity Adjustemnt

1. Load a 5% transparency tape (RD-SE01) into the mechanism.

2. Connect BOT (pin 6 of J13) to the oscilloscope and adjust VR203 so that the output is 3.5 V.

3. Connect EOT (pin 6 of J14) to the oscilloscope and adjust VR202 so that the output is 3.5 V.

14. Pin Description

14-1 IC-101 "SAQ0001-2"(DSP=Digital System Control)

Pin No.	Mark	I/O	Function
1 ∫ 8	SD0 ∫ SD7	I	Inputs the data of the sub-code (LSB~MSB).
9	SUBOE	O	Outputs the latch clock signal of the sub-code data.
10	SUBMAD	O	Outputs the window signal to calculate C1 of the sub-code.
11	FCH	O	Output a signal of 9.408MHz.
12	GND	I	For ground connection.
13	CDCP	I	Inputs the digital data during recording. Inputs the shift clock signal of the ID code during playback.
14	DCP	I	Inputs the shift clock signal of the main ID during recording. Inputs the shift clock signal of the playing data during playback.
15	ADRLOA	I	This is a block address and inputs the load signal of the ID code.
16	DEMDAT	I	Outputs the serial data of 8 bits of playing data.
17	DIRQT	I	Inputs the serial data of the main ID during recording. Inputs the write request signal of the playing data.
18 ∫ 25	IDB7 ∫ IDB0	I	These are internal buses of ECC (LSB~MSB).
26 ∫ 33	DB7 ∫ DB0	I/O	Data buses (LSB~MSB).
34	ORBCP	I	Inputs the latch clock signal of ECC output port B.
35	ORACP	I	Inputs the latch clock signal of ECC output port A.
36	WRQT	I	Inputs the write request signal from the GLU.
37	RRQT	I	Inputs the read request signal from the GLU.
38	GND	I	For ground connection.
39	TEST	I	This is the terminal for IC test. Normally this is for ground connection.
40	NEXT	I	For syndrome calculation. Inputs the page increment signal.
41	SNDSTT	I	Inputs a signal to start syndrome calculation.
42	PQKIR	O	Outputs the switching signals of the C1 and C2.
43	MUTEIN	I	Inputs the muting signal of the digital data.
44	GLUR	O	Outputs a signal to reset the ECC program counter.
45	HFCH	O	Outputs the system clock signal of the ECC.

Pin No.	Mark	I/O	Function
46	SSHIF	O	Outputs the clock signal for the syndrome calculation.
47	SLATCH	O	Outputs the latch clock signal for the results of the syndrome calculation.
48	PQRST	O	Outputs the reset pulse of the syndrome register.
49	INACP	O	Outputs the latch signal for input port A.
50 ∫ 58	A0 ∫ A8	O	These are the output terminals for memory addresses.
59	V_{CC}	I	To be connected to +5V.
60	GND	I	For ground connection.
61	RAMWE	O	Outputs the write enable signal for memory.
62 ∫ 64	A9 ∫ A11	O	These are the output terminals for memory addresses.
65	RAMOE	O	Outputs the output enable signal for memory.
66	A12	O	These are output terminals for memory addresses.
67	A13	O	
68	VCOPL	I	Not used, open.
69	PLL4	O	Not used, open.
70	PLL3	O	Not used, open.
71	PLL2	O	Not used, open.
72	PLL1	O	Not used, open.
73	PLLD	O	Not used, open.
74	PLLC	I	
75	EXOR	O	Outputs the PLL phase comparison signal for the master clock.
76	CK28M	I	Inputs a signal of 28.224 MHz generated by PLL.
77	HEACH	O	Outputs the switching signal for the head amplifier.
78	PBSG	I	Inputs the playback signal.
79	RCSG	O	Outputs the recording signal.
80	TSCK	O	Outputs the drum PG synchronization signal of 33.33 Hz.
81	LEVDA	I/O	Inputs the serial control data and outputs the serial level meter data.
82	LEVSY	I	Inputs the enable signal of the control data.
83	LEVSF	I	Inputs the shift clock signal of the control data.
84	HSW	I	Inputs the drum PG signal.

Pin No.	Mark	I/O	Function
85	GND	I	For ground connection.
86	ATFMAD	O	Outputs the ATF ID signal of 130kHz.
87	SEGCP	O	Outputs the segment clock signal of 66.66Hz.
88	DFLAG	I/O	This is the terminal for error flag of digital signal.
89	MUTE	O	Outputs the muting signal of the D/A converter. (Not used, open)
90	ADDAT	I	Inputs the A/D data.
91	LR	I	Outputs the switching signal to L or R channel.
92	DLOAD	I	Outputs the data load clock signals for D/A and A/D.
93	DSIFT	I	Outputs the data shift clock signals for D/A and A/D.
94	DADAT	I	Outputs the D/A data.
95	PLLCP	O	Not used, open.
96	DEMCOD	O	

14-2 IC-102 "SAQ0002-1"(DEM=Demodulator)

Pin No.	Mark	I/O	Function
1	DIG-I	I	This terminal inputs the digital signal.
2	SIDSH	I	This terminal inputs the shift clock signal for the sub-code ID.
3	SIDDA	I/O	This terminal inputs and outputs the serial data for the sub-code ID.
4	MID-S	I	This terminal inputs the shift clock signal for the main ID.
5	MID-D	I/O	This terminal inputs and outputs the serial data for the main ID data.
6	MICONW	I	This terminal inputs the writing request signal for the PACK data from the microcomputer.
7	MICONR	I	This terminal inputs the reading request signal for the PACK data from the microcomputer.
8 ∫ 11	PD0 ∫ PD3	I/O	These are buses of the PACK data for the microcomputer (LSB~).
12	GND	I	For ground connection
13 ∫ 16	PD4 ∫ PD7	I/O	These are buses of the PACK data for the microcomputer (~MSB).
17 ∫ 26	ADR0 ∫ ADR9	O	These are addresses of the sub-code RAM.

Pin No.	Mark	I/O	Function
27	R-WE	O	This terminal outputs the enable signal to write the sub-code RAM.
28	R-OE	O	This terminal outputs the enable signal to output the sub-code RAM.
29	NC	—	No connection
30 ∫ 37	MD7 ∫ MD0	I/O	These are buses of the sub-code RAM (LSB~MSB).
38	GND	I	For ground connection
39	C1FLAG	I	This terminal inputs the C1 flag for calculating error rate.
40 ∫ 47	IDB7 ∫ IDB0	I	These are internal buses of ECC (LSB~MSB).
48	ORB	I	This terminal inputs the latch pulse of output port B.
49	ORA	I	This terminal inputs the latch pulse of output port A.
50	NEXTP	I	Inputs the next page increment signal for calculating the syndrome of the sub-code.
51	SND-S	I	Inputs a signal for starting the syndrome calculating for the sub-code.
52	DIRQT	O	Outputs the data of the main ID during recording. Outputs the writing request signal of the demodulated data during playback.
53	DEMDAT	O	Outputs a signal to latch calculated syndrome results for the sub-code during recording. Outputs the demodulated data of pin. 8-10 during playback.
54	DREST	O	Outputs a signal to clear the register for the syndrome calculation of the sub-code during recording. Outputs a signal to clear the data symbol counter in the block during playback.
55	ADLOAD	O	Outputs a signal to reset the ECC address counter of the sub-code during recording. Outputs a signal to load the block number of the playing data during playback.
56	MLACH	O	Outputs the clock signal for syndrome calculation of the sub-code during recording. Outputs the latch clock signal of 8 bits of playing data during playback.
57	DCP	O	Outputs the shift clock signal of the main ID during recording. Outputs the shift clock signal of the playing data during playback.
58	CDCP	O	Outputs the data of the digital IN during recording. Outputs the shift clock signal of ID code during playback.
59	V_{CC}	I	For connection to +5V.
60	GND	I	For ground connection.
61	TEST	I	Inputs the control signal of external access to the sub-code RAM.
62	PCMMAD	I	Inputs the window signal to calculate C1 of the sub-code.
63	SUBOE	I	Input the latch signals of sub-code datas SD7~SD0 during recording.

Pin No.	Mark	I/O	Function
64 ∫ 71	SD7 ∫ SD0	O	These are data buses of the sub-code (LSB~MSB).
72	DEMCOD	I	Inputs the NPZI-demodulated playback signal by PLL.
73	PLLCP	I	Input the shift clock signal of the DEM code.
74	D-DATA	I	Inputs the data for D/A.
75	D-SIFT	O	Outputs the shift clock signals for D/A and A/D.
76	D-LOAD	O	Outputs the load clock signals for D/A and A/D.
77	LR2	O	Outputs the double-length clock signal of L/R channels (96kHz).
78	LSRR	O	Outputs the switching signal of L or R channel (48kHz). At "High" level...left channel At "Low" level...right channel
79	LR4	O	Outputs the quadruple-length signal of L/R channel (192kHz).
80	D-FLAG	I/O	This terminal is for output and input of the error flag of digital signal.
81	H-SW	I	Inputs the PG of the drum.
82	FS-SIF	I	Inputs the shift clock signal of the FS-DAT.
83	FS-SYN	I	For identification of the FS-DAT. At "Low" level...Control data At "High" level...level meter data
84	FS-DAT	I/O	Inputs the control data (recording or playback and so on) and outputs the level meter data.
85	GND	I	For ground connection.
86	CXAI	I/O	Crystal terminal (12.288MHz)
87	CXAO		
88	CXBI	I/O	Crystal terminal (11.2896MHz)
89	CXBO		
90	VCOIN	I	Inputs the PLL clock signal for digital input.
91	VCOA	O	Outputs the PLL phase comparison signal for digital input. (A)
92	VCOB	O	Outputs the PLL phase comparison signal for digital input. (B)
93	DIG-O	O	Outputs the digital signal.
94	FRAME	O	Outputs the frame signal of the playback signal.
95	MSYNC	O	Outputs the synchronous detection signal of the playback signal.
96	IDP	O	Outputs a signal for the parity check of the ID code.

14-3 IC-103 "SAQ0003-1"(ECC=Error Correction)

Pin No.	Mark	I/O	Function
1 ~ 8	IDB0 ~ IDB7	I/O	These are for ECC internal busses (LSB~MSB).
9	GND	I	For ground connection.
10	GND		
11	NC	—	No connection.
12	S-RST	I	This is the input terminal to reset the program counter of the sub-code.
13	S-DF1	I	Inputs the done flag 1 signal of the sub-code.
14	S-DF2	I	Inputs the done flag 2 signal of the sub-code.
15	S-CLR	I	This is the input terminal to clear the syndrome register of the sub-code.
16	S-LACT	I	Inputs the latch clock signal for the results of the syndrome calculation of the sub-code.
17	S-SCLK	I	Inputs the clock signal for syndrome calculation of the sub-code.
18 ~ 25	SDB0 ~ SDB7	I	Input the sub-code data (LSB~MSB).
26	SST1	O	For output of the ST-1 signal of the sub-code (not used, open).
27 ~ 30	TD0 ~ TD3	O	For output test (not used, open).
31 ~ 38	TD4 ~ TD11	O	For output test (not used, open).
39	TEST	O	For IC test (these are normally for ground connection).
40	TDS-A		
41	TDS-B		
42	NC	—	No connection.
43	IBS-A	O	For output test of the internal bus select signal.
44	IBS-B		
45	IBS-C		
46	IBS-D		
47	IBS-E		
48	PQ2	I	Inputs the recording and playback signals.
49	V_{CC}	I	To be connected to +5V.

Pin No.	Mark	I/O	Function
50	GND	I	For ground connection.
51	GND		
52	SUB1	I	Inputs the select signal of the sub code.
53	SUB2	I	Normally to be connected to +5V or for input of the select signal of the sub-code.
54	PQ1	I	Inputs C1 area signal of the sub-code.
55	PG	I	Normally to be connected to +5V or for input the gate control signal for the parity calculation.
56	INA-CP	I	Inputs the latch pulse to input port A.
57	CLR	I	This is the input terminal to reset the register for the syndrome calculation.
58	LATC	I	Inputs the latch signal for the results of the syndrome calculation.
59	SCLK	I	Inputs the clock signal for the syncrome calculation.
60	CK	I	Inputs the system clock signal.
61	RST	I	This is the input terminal to reset the ECC program counter.
62	DF-1	I	Inputs the termination signal of the syndrome calculation.
63	DF-2	I	Inputs the C1 and C2 switching signals.
64	ST0	O	This is the output terminal to start the syndrome calculation.
65	ST1	O	This is the output terminal for the page increment of the syndrome calculation.
66	ST2	O	Outputs the memory read request signal.
67	ST3	O	Outputs the memory write request signal.
68	ST4	—	Not used, open.
69	ST5	O	Outputs the results of C1 check.
70	ORA	O	Outputs the latch clock signal of output port A.
71	ORB	O	Outputs the latch clock signal of output port B.
72	ORC	O	Outputs the latch clock signal of output port C.
73 ∫ 80	DB0 ∫ DB7	I	Input the data of LSB~MSB.

14-4 IC-104 "MN52080SDH"(Main Servo)

Pin No.	Mark	I/O	Function
1	V_{SS}	I	For ground connection.
2	CYFG	I	Inputs the signal of the cylinder FG (40 pulses/rev).
3	RLFGT	I	Inputs the signal of the take-up reel FG (40 pulses/rev).
4	RLFGS	I	Inputs the signal of the supply reel FG (40 pulses/rev).
5	CPFG 2	I	Inputs the signal of the capstan FG (250 pulses/rev).
6	FILSL 0	O	Outputs the control signal of the capstan motor driving.
7	FILST 1	—	Not used, open.
8	CPFG 1	I	Inputs the signal of the capstan FG (250 pulses/rev).
9	CYPG 1	I	Inputs the signal of the cylinder PG (1 pulse/rev).
10	V_{DD}	I	To be connected to +5V.
11	NC	—	Not used, open.
12	V_{SS}	I	For ground connection.
13	TC	—	Not used, open.
14	SP1	O	Output the sample hold control signal.
15	SP2		
16	SPE		
17	SRVDL	O	Outputs the signal to connect the ATF circuit.
18	SYNC	I	Inputs the RF detection signal.
19	ATFWDN	O	Outputs the data about the ATF area.
20	NC	—	Not used, open.
21	V_{DD}	I	To be connected to +5V.
22	V_{SS}	I	For ground connection.
23	TSTEN	—	Not used, open.
24 ~ 26	TSTSL 0 ~ TSTSL 2	—	Not used, open.
27	ATFSL	—	Not used, open.
28	NC	—	Not used, open.
29	NC		
30	NC		
31	V_{SS}	I	For ground connection.

Pin No.	Mark	I/O	Function
32	NC	—	Not used, open.
33	V_{DD}	I	To be connected to +5V.
34	NC	—	Not used, open.
35	SP2D	O	Outputs the sample hold control signal.
36	ROT	I	Input the ROT (SEGCP) of 66.66Hz.
37	CLK	I	Inputs the system clock signal of 9.408MHz.
38	ROT 2	I	Inputs the 1/2 ROT of 33.33Hz.
39	HSW	O	Outputs the head switch signal of 33.33Hz.
40	TRK 1	O	Outputs the synchronous data of the ATF.
41	OROT 2	—	Not used, open.
42	V_{DD}	I	To be connected to +5V.
43	V_{SS}	I	For ground connection.
44	NRLSL	I	Inputs the SRVD latch command of the reel.
45	NCPSL	I	Inputs the SRVD latch command of the capstan.
46 ~ 51	SRVD 0 ~ SRVD 5	I	Input the summed data of the reel FG speed.
52	V_{SS}	I	For ground connection.
53	NLNROK	—	Not used, open.
54	V_{DD}	I	To be connected to +5V.
55	NCPK	O	Outputs the data of the capstan lock.
56	CAPER	O	Outputs the data of the rotation direction of the capstan.
57	NCYK 1	O	Outputs the data of the cylinder lock.
58	NCYK 0		
59	SPEMSK	I	Inputs the data of the PCM playback.
60	SRVMD	I	Inputs the switching signal of the CAP servo mode.
61	TPH	I	Inputs a signal for the track pitch. (At a "High" level...13.6μm At a "Low" level...20.4μm)
62	NRST 2	I	Inputs the reset signal at a low level.
63	V_{DD}	I	To be connected to +5V.
64	V_{SS}	I	For ground connection.
65	NC	—	Not used, open.

Pin No.	Mark	I/O	Function
66	SNVLD 0	—	Not used, open.
67	SNVLD 1		
68	NC	—	Not used, open.
69	TSTCLK	I	For input test (normally for ground connection).
70 ∫ 72	TEST 0 ∫ TEST 2	I	For input test (normally for ground connection).
73	V_{DD}	I	To be connected to +5V.
74	NC	—	Not used, open.
75	V_{SS}	I	For ground connection.
76	TEST P	I	For input test (normally for ground connection).
77	TEST S	O	This is the input terminal of the signal to switch to the cut-off frequency for the compensating circuit when the capstan servo rotates slowly.
78	COSL	O	
79	TL	O	Outputs the torque limit signal of the capstan motor.
80	CAPED	O	Outputs the command for the rotation direction of the capstan.
81	PWMCAP	O	Outputs the 73.5kHz PWM of the capstan motor.
82	CYLED	O	Outputs the command for the rotation direction of the cylinder.
83	PWMCYL	O	Outputs the 73.5kHz PWM of the cylinder motor.
84	V_{DD}	I	To be connected to +5V.

14-5 IC-105 "MN53020DF"(IFGA=Interface Gate Alley)

Pin No.	Mark	I/O	Function
1 ∫ 7	SBPD1 ∫ SBPD7	I	Input signals to set the muting.
8	DLOCK2	—	——
9	DFSSEL	I	——
10	SVDD	I	To be connected to +5V.
11	PLDT	I	——
12	SV_{SS}	I	For ground connection.
13	PLCK	I	Inputs the clock signal.
14	MCW	I	Inputs the PACK data write request signal.

Pin No.	Mark	I/O	Function
15	OFSCP	O	——
16	CLREN	I	——
17	NREC	I	Inputs the high level signal during playback and inputs the low level signal during recording.
18	DSCP	I	——
19	MCK7	O	Outputs the master clock signal.
20	NBLK	O	Outputs the signal that detects the signalless mode.
21	BLKSEL	I	Inputs the switching signal of the non-recorded segment level. (At −60dB level, this signal will be inputted at high. At −40dB level, this signal will be inputted at low.)
22	APR	I	Inputs the switching signal of the recording and playback of the amplifier.
23	NRST2	I	Connects the +5V power terminal for the reset signal.
24	MCK3R5	O	Outputs the master clock signal for the panel control of the microcomputer.
25	SVSGCP	O	Outputs the SEGCP signal of 66.66Hz.
26	SP2	I	Inputs the sample hold control signal.
27	SRPR	O	Outputs the switching signal of the recording and playback. (At a "High" level...recording At a "Low" level...playback)
28	TEST 1	I	For input test (normally for ground connection).
29	TEST 2		
30	TEST 3		
31	GND	I	For ground connection.
32	TP1	I	For input test (not used, open).
33	VDD2	I	To be connected to +5V.
34	TP2	I	For input test (not used, open).
35	TP3	I	
36	PLL VAR	O	——
37	PLL18M	I	——
38	ADD	I	Inputs the A/D data.
39	DFD	O	Outputs the D/A data.
40	DSM	O	Outputs the switching signal of the D/A parallel R/L channels. At a "High" level...right channel
41	DOD	O	Outputs the digital data signal.
42	DID	I	Inputs the digital data signal.

Pin No.	Mark	I/O	Function
43	ADDAT	O	Outputs the A/D data.
44	DADAT	I	Inputs the D/A data.
45	TIDP	O	Outputs terminal for the flag counter (not used).
46	MCK28	I	Input a signal of 28.224 MHz generated by the PLL.
47	MEACH	I	Inputs the switching signal for the head amplifier.
48	LR2	I	Outputs the double-length clock signal of L/R channels (96 kHz).
49	LR	I	Outputs the switching signal of L or R channel (48 kHz). (At "High" level...left channel At "Low" level...right channel)
50	SEGCP	I	Inputs the segment clock signal of 66.66 Hz.
51	HSW	I	Inputs the drum PG signal.
52	GND	I	For ground connection.
53	DSIFT	I	Inputs the shift clock signal of the A/D and D/A data.
54	SVDD	I	To be connected to +5V.
55	TSCK	I	Inputs the drum PG synchronization signal of 33.33 Hz.
56	HFCH	I	Inputs the ECC system clock signal.
57	CDCP2	O	Outputs the digital data during recording. Outputs the ID code shift clock signal during playback.
58	DREST	I	This is the input terminal to clear the syndrome calculation register of the sub-code during recording. Inputs the signal to clear the data symbol counter in the block during playback.
59	DCP	I	Inputs the shift clock signal of the main ID code during recording. Inputs the 8-bit latch clock signal of the playback data.
60	CDCP 1	I	Inputs the digital data during recording. Inputs the shift clock signal of the ID code during playback.
61	D-LOAD	I	Inputs the load clock signal for the D/A and A/D data.
62	DSYNC	I	Inputs the quadruple-length signal of L/R channel (192 kHz).
63	VCDIV	O	Outputs the PLL clock signal for the digital input.
64	DIG0	I	Inputs the digital signal.
65	MSYNC	I	Inputs the synchronous detection signal of the playback signal.
66	IDP	I	Inputs a signal for the parity check of the ID code of the playback signal.
67	DIGI	O	Outputs the digital signal.
68	MICOMW	O	Outputs the PACK data write request signal.
69	SOE	I	Inputs the RAM input enable signal of the sub-code.

Pin No.	Mark	I/O	Function
70	SWE	I	Inputs the RAM write enable signal of the sub-code.
71	SAD 9	I	These are the sub-code RAM addresses (~MSB).
72	SAD 8		
73	VDD	I	To be connected to +5V.
74	SAD 7	I	This is a sub-code RAM address.
75	GND	I	For ground connection.
76 ~ 82	SAD6 ~ SAD0	I	These are sub-code RAM addresses (LSB~).
83	D24M	I	Inputs the PLL clock signal for the digital input.
84	SBPD 0	I	Inputs a signal to set the muting.

14-6 IC-106 "MN18982SDT" (SBP=Sub Code Processor)

Pin No.	Mark	I/O	Function
1	V_{SS}	I	For ground connection.
2 ~ 9	SPDT0 ~ SPDT7	I/O	These are addresses and data buses.
10	NSPSTB	I	Inputs the strobe signal for signal processing.
11	OFSCP	I	——
12	NSPRDY	O	This is the output terminal for the data transfer.
13	SBPTST	—	Not used, open.
14	TRK1	I	Inputs the ATF synchronization data.
15	FLGCK	O	Outputs the strobe pulse.
16	FLGDA	O	PACK OK, undetected PCMID and PND, SUBID valid, PLL data, SID OK and speed mode.
17	TEST	O	Outputs the control signal of external access to the sub-code RAM.
18	CLEAN	O	——
19	NREC	O	Outputs the high level signal during playback and outputs the low level signal during recording.
20	DSCP	O	——

Pin No.	Mark	I/O	Function
21	TXD	—	Not used, open.
22	RXD		
23	TRCLK		
24	TCIQ		
25	IRQB		
26	NSPCS	I	Inputs the chip select signal for the signal processing.
27	$\overline{EX1}$	—	For control of the chip extension (not used, open).
28	$\overline{EX2}$		
29	7MCK	I	Input the master clock signal of 7.056 MHz.
30	OSC2	—	Not used, open.
31	RST	I	Inputs the reset signal.
32	VDD	I	For power connection.
33 ∫ 40	SBPD0 ∫ SBPD7	O	Output signals to set the muting.
41	HSW	I	Inputs the head switching signal.
42	TSCK	I	Inputs the drum PG synchronization signal of 33.33 Hz.
43	SEGCP	I	Inputs the segment clock of 66.66 Hz.
44	DLOCK2	—	——
45	LEVSY	O	Outputs the control data enable signal.
46	LEVSF	O	Outputs the control data shift clock signal.
47	LEVDA	I/O	Inputs the serial control data and outputs the serial level meter data.
48	DFSSEL	O	——
49 ∫ 56	PD0 ∫ PD7	I/O	These are the terminals for the PACK data busses for computer (LSB~MSB).
57	PLDT	O	——
58	PLCK	O	Outputs the clock signal.
59	MICONR	O	Outputs the PACK data read request signal.
60	MICONW	O	Outputs the PACK data write request signal.
61	SIDSH	O	Outputs the shift clock signal of the sub-code ID.
62	SIDDA	I/O	Inputs and outputs the serial data of the sub-code ID.
63	MID-S	O	Outputs the shift clock signal of the main ID.
64	MID-D	I/O	Inputs and outputs the serial data of the main ID.

14-7 IC-107 "MN188322SDK"(System Control)

Pin No.	Mark	I/O	Function
1 ∫ 3	NC	—	Not used.
4	RFENV	I	Inputs the envelope signal for detection of the tape end and beginning.
5	NBLK	I	Inputs the signal that detects the signalless mode.
6	NCYLOK 0	I	Input the cylinder lock signal.
7	NCYLOK 1		
8	CAPER	I	Inputs commands for the rotation direction of the capstan servo.
9	NCAPLOK	I	Inputs the capstan lock signal.
10 ∫ 12	TH3 ∫ TH1	I	Inputs the tape hole detection signal.
13	NC	—	Not used, open.
14	NC		
15 ∫ 17	TH6 ∫ TH4	I	Inputs the tape hole detection signal.
18	NCAPSL	O	Outputs the latch signal for the capstan servo.
19	NRELSL	O	Outputs the latch signal for the reel servo.
20	CY GAIN	O	Outputs the gain down control signal of the cylinder servo.
21	RLTLK	O	This is the output terminal to control the speed and phase of the capstan servo.
22	NC	—	Not used, open.
23	M MOD	O	Output signals to control the rotation speed and direction of the mode and cassette loading motors.
24	M FWD		
25	M REV		
26	GND	I	For ground connection.
27	NC	—	Not used, open.
28	NRST 1	I	Inputs the reset signal at a low level.
29 ∫ 34	NC	—	Not used.
35	BOT	I	Inputs the tape beginning detection signal.
36	EOT	I	Inputs the tape end detection signal.
37	OPEN	I	Inputs the open/close detection signal.
38	CLOSE		

Pin No.	Mark	I/O	Function
39	DEW	I	Inputs the detection signal for the dew sensor.
40 ∫ 42	MMOD 2 ∫ MMOD 0	I	Input the tape mode detection signal.
43	NPRDY	I	Inputs the transfer command of the data from the panel control.
44	7 MCK	I	Inputs the master clock signal.
45	NC	—	Not used, open.
46	V_{SS}	I	For ground connection.
47	NC	—	Not used, open.
48	NC		
49	V_{DD}	I	To be connected to +5V.
50	NPMUT	I	Inputs the power mute signal.
51	RLFGTU	I	Inputs the FG pulse of the take-up reel.
52	RLFGSU	I	Inputs the FG pulse of the supply reel.
53 ∫ 59	SPDT 7 ∫ SPDT 1	I/O	These terminals are addresses and data buses.
60 ∫ 65	NC	—	Not used.
66	SPDT 0	I/O	Address and data bus.
67 ∫ 70	NC	—	Not used, open.
71	TRCLK	I/O	For input and output of the serial data.
72	RXD	I	Inputs the serial data.
73	TXD	O	Outputs the serial data.
74	NSPSTB	O	Outputs the strobe signal for signal processing.
75	NSPCS	O	Outputs the chip select signal for signal processing.
76	RST OUT	O	Outputs the reset signal.
77	NC	—	Not used, open.
78	INH (COPY)	I	For ground connection.
79	—	—	This is a test terminal.
80	TEST	I	This is a test terminal.
81	NSPRDY	I	Inputs the data transfer command.

Pin No.	Mark	I/O	Function
82	NC	—	Not used, open.
83	TP	O	Outputs the track pitch signal.
84	AF REC	—	Not used, open.
85	SRVMD	O	Outputs the data of the servo mode.
86	SPEMSK	O	Outputs the data of the PCM playback.
87	NC	—	Not used, open.
88	RHHET	O	Outputs the signal to turn on the heater.
89	AR/$\overline{P}$	O	Outputs the recording/playback switching signal of the amplifier.
90	SG MTG	O	Outputs the signal to set the muting.
91 ∫ 96	NC	—	Not used.
97	ATT	O	Outputs the attenuator signal.
98	BLKSEL	O	Outputs the switching signal of the non-recorded segment level. (At −60dB level, this signal will be inputted at high. At −40dB level, this signal will be inputted at low.)
99	NC	—	Not used.
100	NEMP	O	Outputs the emphasis signal.
101 • 102	NC	—	Not used.
103 ∫ 108	SRVDT 5 ∫ SRVDT 0	O	Output the summed data of the reel FG speed.
109	V_{DD}	I	To be connected to +5V.
110 ∫ 118	NC	—	Not used, open.
119	V_{SS}	I	For ground connection.
120	TSCK	I	Inputs the timing clock signal of 33.33Hz.
121	HSW	I	Inputs the head switching signal of 33.33Hz.
122 ∫ 124	NC	—	Not used.

14-8 IC-201 "AN8320S"(Sub Servo & ATF)

Pin No.	Mark	I/O	Function
1	CAPFG 1	O	Outputs the capstan FG signal.
2	CAPFG 1	I	Inputs the capstan FG signal (250 pulses/rev).
3	NFC	I	This is the input terminal to connect with the condenser of the NF loop.
4	CYLDPG	O	Outputs the cylinder PG signal (1 pulse/rev).
5	PGWA	I	This is the input terminal to connect with the VR for adjustment of the pulse width of the PG signal.
6	CYLPG	I	Inputs the cylinder PG signal (1 pulse/rev).
7	GND	I	For ground connection.
8	SVRF	I	Inputs the envelope detection signal.
9	CDD	I	This is the input terminal for connection with the detection circuit for the pilot signal's peak.
10	PD0	O	Outputs the detection signal for the pilot signal's peak.
11	PD1	I	Inputs the detection signal for the pilot signal's peak.
12	SP1	I	Inputs the sample hold control signal.
13	SP2		
14	Vspe	I	Inputs the reference voltage for the detection circuit of the difference of the pilot voltages.
15	SPE	I	Inputs the sample hold control signal.
16	CSH	I	Input terminal for connection with the condenser in the detection circuit for the peak voltage of the pilot signal .
17	ATFTER	O	Outputs the ATF control signal.
18	NFC	I	This is the input terminal to connect with the condenser of the NF loop.
19	VCC 1	I	To be connected to +5V.
20	SRVDL	I	This is the input terminal to connect with the ATF circuit.
21	NC	—	Not used, open.
22	Vref	I	This is the input terminal to set the reference voltage.
23 ∫ 26	NC	—	Not used, open.
27	CYLDFG	O	Outputs the cylinder FG signal (40 pulses/rev).
28	CYLDFG	I	Inputs the cylinder FG signal (40 pulses/rev).
29	CYLDFG	O	Outputs the cylinder FG signal (40 pulses/rev).

Pin No.	Mark	I/O	Function
30	CYLFG	I	Inputs the cylinder FG signal (40 pulses/rev).
31	STNDBY	I	To be connected to +5V.
32	RLFGT	I	Inputs the take-up reel FG signal (40 pulses/rev).
33	RLFGT	O	Outputs the take-up reel FG signal (40 pulses/rev).
34	RLFGT	I	Inputs the take-up reel FG signal (40 pulses/rev).
35	RLDFGT	O	Outputs the take-up reel FG signal (40 pulses/rev).
36	RLDFGS	O	Outputs the supply reel FG signal (40 pulses/rev).
37	RLDFGS	I	Inputs the supply reel FG signal (40 pulses/rev).
38	RLFGS	O	Outputs the supply reel FG signal (40 pulses/rev).
39	RLFGS	I	Inputs the supply reel FG signal (40 pulses/rev).
40	V_{CC} 2	I	To be connected to +5V.
41	CAPFG 2	O	Outputs the capstan FG signal (250 pulses/rev).
42	CAPFG 2	I	Inputs the capstan FG signal (250 pulses/rev).
43	CAPFG 2	O	Outputs the capstan FG signal (250 pulses/rev).
44	CAPFG 2	I	Inputs the capstan FG signal (250 pulses/rev).
45	CAPDFG 2	O	Outputs the capstan FG signal (250 pulses/rev).
46	CAPFIL	I	Inputs the control signal for the capstan motor driving.
47	CAPDFG 1	O	Outputs the capstan FG signal (250 pulses/rev).
48	CAPDFG 1	I	Inputs the capstan FG signal (250 pulses/rev).

14-9 IC426 IC-501 "SM5805P"(Digital Filter)

Pin No.	Mark	I/O	Function	
1	CKIN	I	This is the input terminal of the clock signal that is a basis of the system clock.	
2	$\overline{\text{CKSE}}$	I	This is the input terminal of the signal for the rate of the frequency division. (At a "High" level or when this terminal is open...f CKIN=256fs At a "Low" level...f CKIN=192fs)	
3	WDCK	I	This is the input terminal of the dual-rate clock signal (2fs).	
4	DINL	I	Inputs the left-channel data.	When the serial data of the right and left channels, both terminals are short-circuited.
5	DINR	I	Inputs the right-channel data.	
6	$\overline{\text{IPARA}}$	I	This is the input terminal of the signal for the timing of the input data word. (At a "High" level or when this terminal is open ...LR serial At a "Low" level...LR parallel)	
7	$\overline{\text{ILSB}}$	I	This is the input terminal to select the order of the input data bits. (At a "High" level or when this terminal is open ...MSB is the first At a "Low" level...LSB is the first.)	
8	IBCK	I	Inputs the bit clock signal of the input data.	
9	IBO	O	This is the output terminal of the bit clock for the internal input data.	
10	$\overline{\text{IBPOL}}$	I	This is the input terminal to select the polarity of the bit clock for the bit clock.	
11	U/$\overline{\text{O}}$	I	This is the input terminal to select the decibel meter or interpolater operation mode. At a "High" level or when this terminal is open...the decibel meter operates in the recording mode. At a "Low" level...the interpolater operates in the playback mode.	
12	LRCK	I	This is the input terminal of the clock signal of the basic sample rate (fs).	
13	$\overline{\text{LRPOL}}$	I	This is the input terminal to select the polarity of the LRCK. At a "High" or when this terminal is open...the left channel is "Low" and the right channel is "High" . At a "Low" level...the left channel is "High" and the right channel is "Low"	
14	V_{SS}	I	For ground connection.	
15	$\overline{\text{OFB}}$	I	This is the input terminal to select the form of the input data when U/O=H, or the form of the output data when U/O=L. (At a "High" level or when this terminal is open...the datas are in two's complement form. At a "Low" level...the datas are in offset bynary form.)	
16	SH	O	Outputs the converter control signal.	The ADC control signal is out-putted when the recording mode is U/O=H. The DAC control signal is out-putted when the playback mode is U/O=L.
17	CC	O	Outputs the converter control signal.	
18	BBC	O	This is the output terminal of the bit clock for the PCM 77 Burr Brown A/D-D/A converter.	
19	$\overline{\text{OBPOL}}$	I	This is the input terminal to select the polarity of the bit clock for the output data.	

Pin No.	Mark	I/O	Function
20	OBO	O	This is the output terminal of the bit clock for the internal output data.
21	OBCK	I	This is the input terminal of the bit clock of the output data.
22	$\overline{\text{OLSB}}$	I	This is the input to select the order of the output data bits. (At a "High" level or when this terminal is open...MSB is the first. At a "Low" level...MSB is the first.)
23	$\overline{\text{OPARA}}$	I	This is the input terminal of the signal for the timing of the output data word. (At a "High" level or when this terminal is open...LR serial. At a "Low" level...LR parallel.)
24	DOR	O	Outputs the data of the right channel (OPARA=L). The deglitch signal of DAC (OPARA=H).
25	DOL	O	Outputs the data of the left channel (OPARA=L). Output the data of the left/right channel (OPARA=H).
26	$\overline{\text{ODLY}}$	I	This is the input terminal of the signal for the timing of the output data word. (At "Low" level when this terminal is delayed. At "High" level when this terminal is not delayed.)
27	OLE	O	This is the output terminal of the output data.
28	V_{DD}	I	To be connected to +5V.

14-10 IC-603 "M50754-430FP"(Panel Control)

Pin No.	Mark	I/O	Function
1	V_{SS}	I	For ground connection.
2	P27 (LEVSF)	I	Inputs the control data shift clock signal.
3	P26 (LEVDA)	I	Inputs the level meter data.
4	P25	O	This is the output terminal for the digital LED display.
5	P24	O	This is the output terminal for the analog LED display.
6 ∫ 9	P23 ∫ P20	I	Input the key-return signal.
10	NC	—	Not used.
11	NP RDY	O	Outputs the ready signal.
12	NTRCLK	I/O	Inputs and outputs the clock signal of the serial data.
13	RXD	O	Sends the serial data.
14	TXD	I	Receives the serial data.
15 ∫ 18	P33 ∫ P30	O	Outputs the signals for LED displays. (P33: edit display P32: pause display P31: recording display P30: playback display)
19	INT 1	I	Inputs the remote control signal.
20	INT 2 (LEVSY)	I	Inputs the control data enable signal.
21	CNV_{SS}	I	For ground connection.
22	$\overline{RESET}$	I	Input the reset signal at a low level.
23	NC	—	Not used, open.
24	X_{IN} (MCK3R5)	I	Inputs the master clock signal.
25	X_{OUT}	O	Not used, open.
26	NC	—	Not used, open.
27	X_{CIN}	I	For ground connection.
28	X_{COUT}	O	Not used.
29	X_{SS}	I	For ground connection.
30	NC	—	Not used, open.
31 ∫ 34	P57 ∫ P54	I	Input the key-return signal.
35	VP	I	To be connected to −27V.

Pin No.	Mark	I/O	Function
36 • 37	P51 • P50	O	Output the signal for the display tube.
38 ∫ 45	P17 ∫ P10	O	Output the signal for the display tube.
46	NC	—	Not used, open.
47 ∫ 54	PO7 ∫ PO0	O	Output the signal for the display tube.
55 ∫ 62	P47 ∫ P40	O	Output the signal for the display tube.
63 • 64	V_{CC}	I	To be connected to +5V.
65	V_{SS}	I	For ground connection.
66 ∫ 71	P65 ∫ P60	O	Output the signal for the key scan and the display tube.
72	NC	—	Not used, open.

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