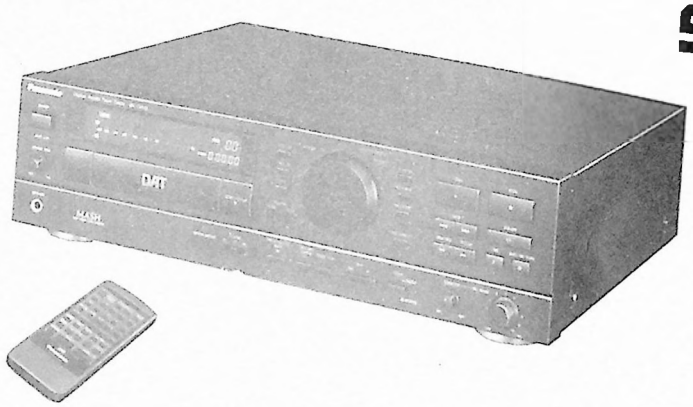
ORDER NO. AD9009273G0

Technical Guide

Digital Audio Tape Deck DAT

SV-DA10



SV-3700

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BASICS OF DAT

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BASICS OF DAT

1. What Is DAT?

* DAT is an abbreviation of Digital Audio Taperecorder. The DAT is based on a totally new concept of tape recording. It temporarily converts analog musical signals into digital code and records it on a cassette tape. During playback, it converts the digital code on the tape back into a high-quality analog signal.

* The conventional cassette equipment directly records input analog signals on tapes. As a result, depending on the tape characteristics and/or head performance, the conventional cassette equipment suffers form various problems that adversely affect total quality in the process of recording and playback.

* Included in these problems are narrowed dynamic and/or frequency range, wow & flutter, tape hiss, distortion, and others. The conventional cassette equipment has already reached theoretical and cost limits in resolving those problems.

* The DAT provides a solution to all of these problem by recording musical signals in the form of digital code.

* The DAT contains A/D and D/A converters to convert analog signal into digital code before recording takes place, and to convert recorded digital code back into the original analog signal before feeding it to the output jacks. With digital input/output jacks, the DAT allows digital dubbing through which only minute degradation of total quality occurs.

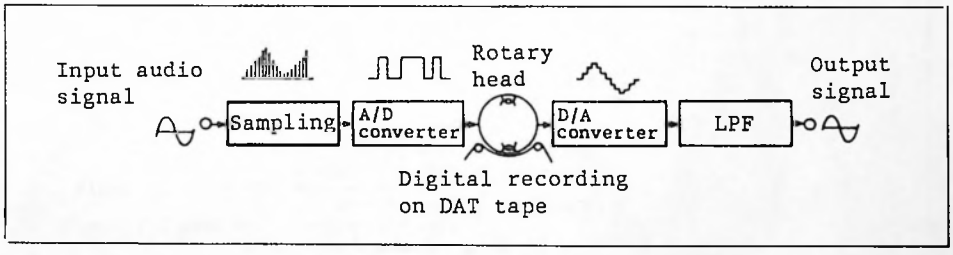


Fig. 1–1

1) R-DAT and S-DAT

* R-DAT: refers to the Rotary-head DAT. R-DAT uses the helical scan recording system with a rotary head, as used in the VCR.

* S-DAT: refers to the Stationary-head DAT. The S-DAT equipment uses a stationary head as used in conventional audio cassette equipment

* The S-DAT allows simple mechanisms and both-way tape transport at the same tape speed (4.76 cm/sec.) as conventional cassette equipment, but it requires a larger cassette size than the R-DAT. Also it requires sophisticated head manufacturing techniques to provide 22 tracks on a half width of a tape. In addition, it has some problems with recorded tape compatibility. For these reasons, the development of the S-DAT has been postponed until the techniques for it are more feasible.

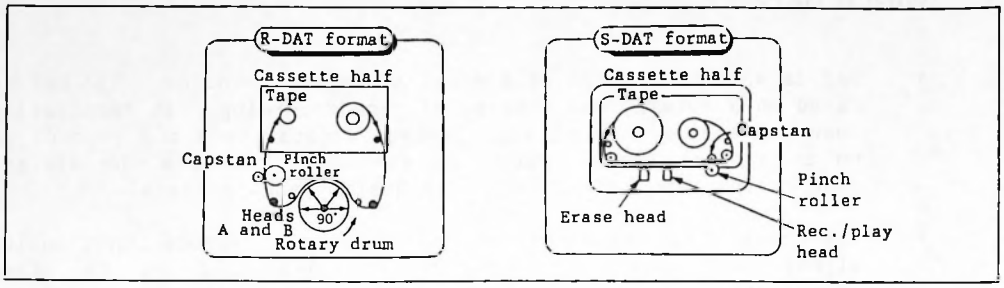


Fig. 1–2

2. How It Records

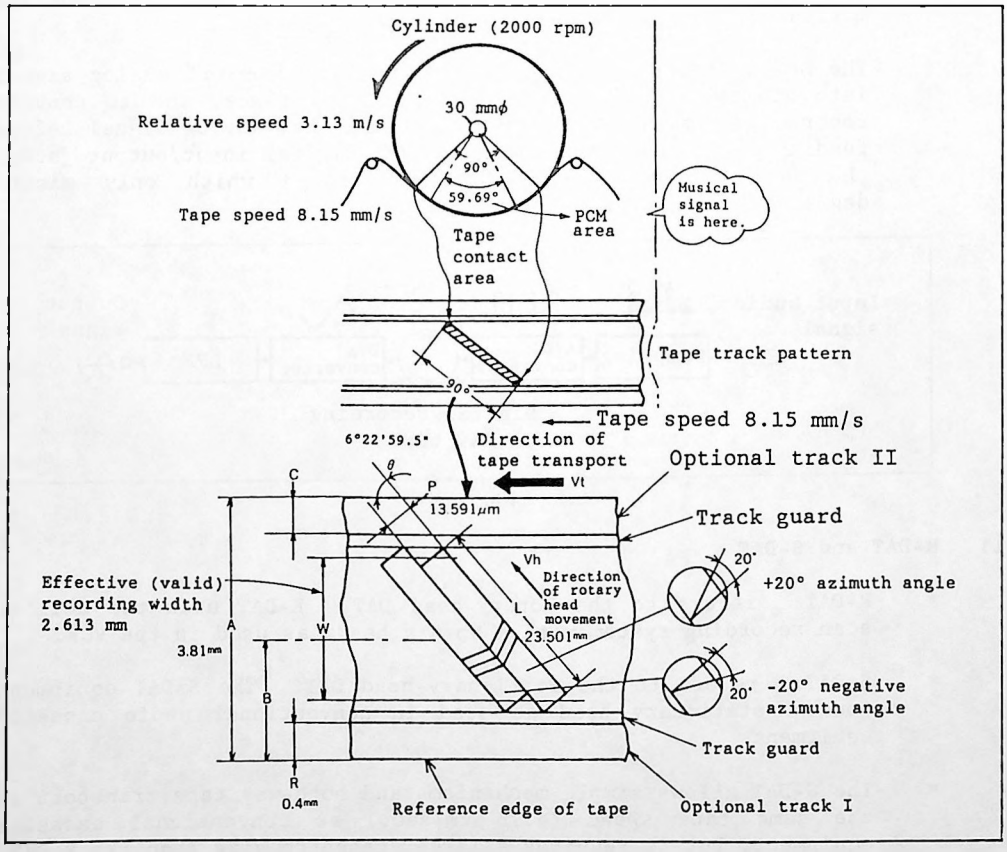


Fig. 1–3

The R-DAT equipment has a rotary cylinder on which two heads (A and B) are mounted. As the cylinder rotates (at 2000 rpm), data is alternately recorded by the two heads.

The relative tape speed to the heads is 3.13 meters per second, which depends on the absolute tape speed (8.15 mm per second) and cylinder's rotation rate. This low absolute tape speed explains why the DAT tape has a recording duration of up to 2 hours with a compact cassette design.

To achieve long recording time with limited length of tape, heads A and B perform guard band-less recording.

1) Analog to Digital Conversion

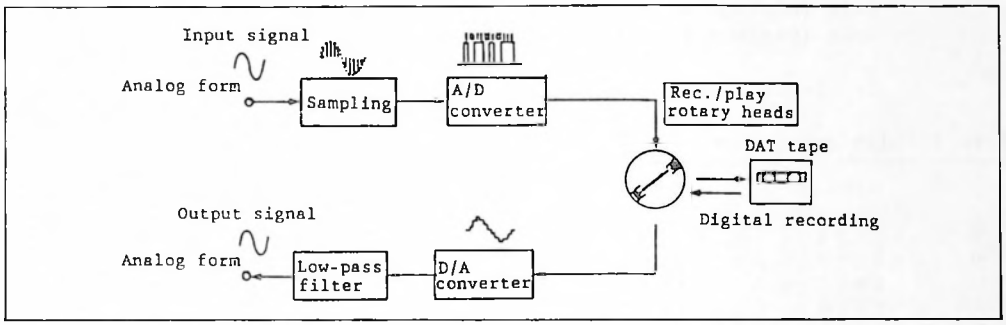


Fig. 1–4

* For digital recording, the input analog signal must first be converted into digital code.

* For this conversion, the input signal is sampled at a rate of 48 kHz. This means that the signal is divided into 48,000 segments every second.

* Next, to represent the signal level of each of these segments in numerical form, the signal is quantized at an accuracy of 16 bits (2 = 65,536). This means that signal levels are represented by 65536 steps.

* The digitalized signal is binary data comprised of a string of "0" and "1". We can record this binary data on a magnetic tape by designating pole N to, say, value 0 and pole S to value 1. However, if many zeros or ones consecutively occur in the recording data, we will not be able to restore the original data during playback as we cannot discriminate one bit from the next.

* To avoid this inconvenience, we record on magnetic tape using 8-10 modulation (ETM) in which 8 bit data (256 values) is converted into 10 bit data (1024 values), and 256 values out of the 1024 values are used.

2) 8-10 Modulation (ETM)

In the course of recording, each 8 bit data word is converted (modulated) into a signal 10 bit word. We call this modulation scheme 8-10 modulation as we convert 8 bit data into 10 bit data. The modulated data contain more 0 to 1 and 1 to 0 transitions that the original 8 bit data, and allows easier data restoration (playback).

During data recording on tape, logical "1" is identified by low to high or high to low transition.

After 8 to 10 modulation, data is recorded on tape at four different inverting intervals (recording wavelengths) of 0.8T to 3.2T.

λmin (minimum inverting interval) = 0.67 μm
λmax (maximum inverting interval) = 2.66 μm

T: 1-bit interval (0.8T is equal to 1Tch)

8 to 10 bits conversion

	Data (MSB··LSB)	Code (MSB·····LSB)
00	0 0 0 0 0 0 0 0	0 1 0 1 0 1 0 1 0 1
01	0 0 0 0 0 0 0 1	0 1 0 1 0 1 0 1 1 1
02	0 0 0 0 0 0 1 0	0 1 0 1 0 1 1 1 0 1
03	0 0 0 0 0 0 1 1	0 1 0 1 0 1 1 1 1 1
04	0 0 0 0 0 1 0 0	0 1 0 1 0 0 1 0 0 1
05	0 0 0 0 0 1 0 1	0 1 0 1 0 0 1 0 1 1
06	0 0 0 0 0 1 1 0	0 1 0 1 0 0 1 1 1 0
07	0 0 0 0 0 1 1 1	0 1 0 1 0 1 1 0 1 0
F8	1 1 1 1 1 0 0 0	1 1 1 1 1 0 0 1 0 1
F9	1 1 1 1 1 0 0 1	1 1 1 1 1 0 0 1 1 1
FA	1 1 1 1 1 0 1 0	1 1 1 1 1 0 1 1 0 1
FB	1 1 1 1 1 0 1 1	1 1 1 1 1 0 1 1 1 1
FC	1 1 1 1 1 1 0 0	1 1 1 1 1 1 1 1 0 0 1
FD	1 1 1 1 1 1 0 1	1 1 1 1 1 1 1 1 0 1 1
FE	1 1 1 1 1 1 1 0	1 1 1 1 1 1 1 1 1 1 0
FF	1 1 1 1 1 1 1 1	1 1 1 1 1 0 1 0 1 0

Table 1–1

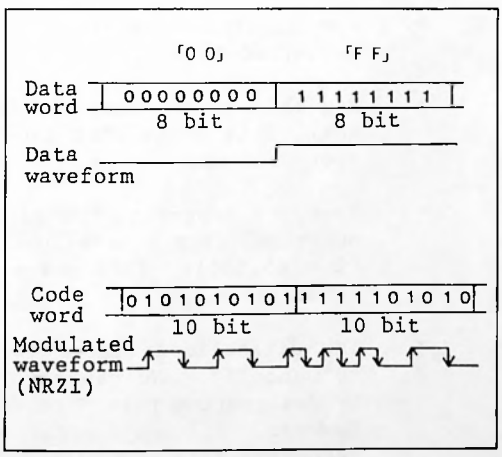


Fig. 1–5

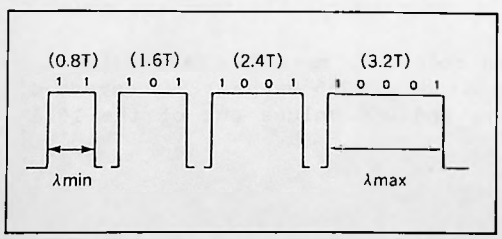


Fig. 1–6

<Data Bits and Channel Bits>

The data before 8-10 conversion consists of bits called "data bits" and the bits after conversion are called "channel bits."

Data bits are usually used in the description of the DAT format. For convenience, 8 bits are grouped into a unit called a symbol. (1 symbol = 8 data bits) Therefore, a 16- bit PCM signal represents 2 symbols.
When recorded onto tape, 10 channel bits represent 1 symbol.

The relationships between symbols, blocks and tracks are given below.
(1) 1 symbol = 8 data bits = 10 channel bits
(2) 1 block = 36 symbols = 288 data bits = 360 channel bits
(3) 1 track = 196 blocks = 56,448 data bits = 70,560 channel bits

3) Rotary Transformer Function

The R-DAT uses rotary heads for recording/playback. Signals are transferred to/from the rotating magnetic heads from/to amplifiers via rotary transformers. The rotary transformers are built into the head cylinder.

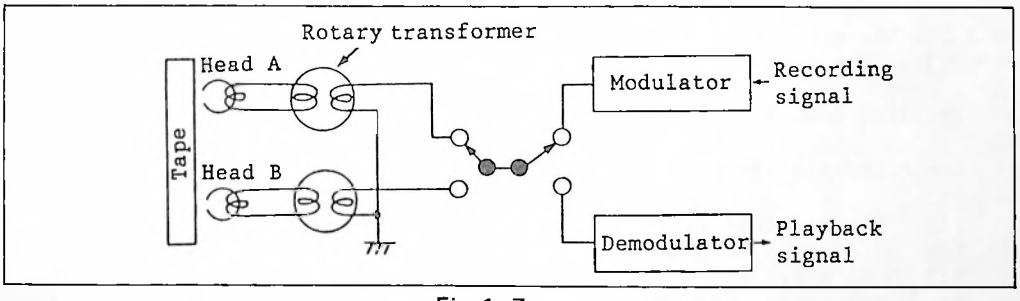


Fig. 1–7

(1) Cylinder construction

Recording and playback signals are transferred to/from the heads via the rotary transformers (coils) provided on the upper (rotary) and lower (stationary) cylinders.

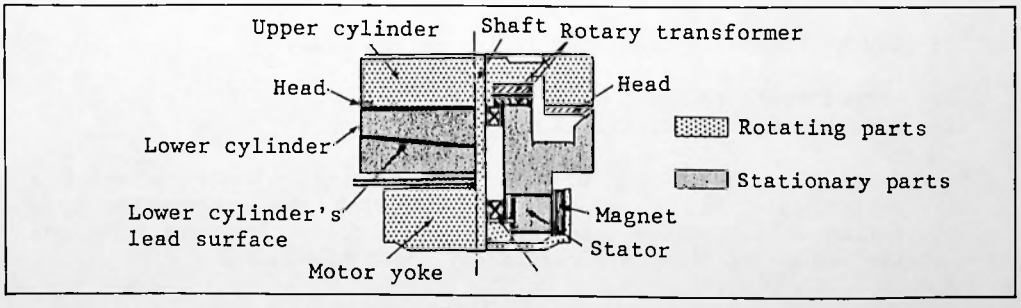


Fig. 1–8

(2) Frequency response

If consecutive zeros or ones were recorded on tape, the playback signal would be a DC level, and we could not tell how many zeros or ones are contained in the playback signal. To prevent this, the R-DAT uses rotary transformers to block the DC component contained in recording/playback signals. The rotary transformer has an output frequency response as shown in figure 1-9. The response extends into the high frequency range up to 4.7 MHz.

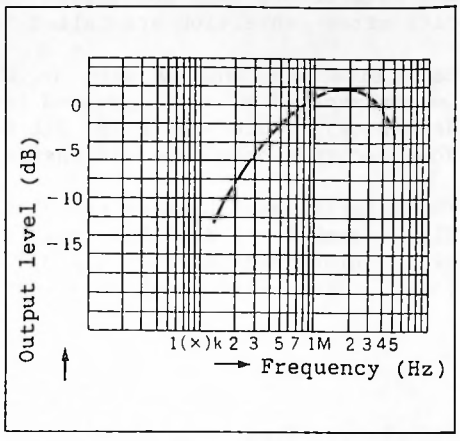


Fig. 1–9

3. R-DAT Specifications

The R-DAT has six standard specification modes (functions). These modes are automatically switched from one to another.

1) REC/PLAY Modes

The R-DAT has the following four REC/PLAY modes:

(1) Standard mode (also covers broadcasting satellite B mode)
(2) Option (1) mode (also covers broadcasting satellite A mode)
(3) Option (2) mode (long REC/PLAY mode)
(4) Option (3) mode (4 channel mode)

Option modes (2) through (4) will be provided in future DAT equipment as broadcasting satellite (BS) programs and other software and hardware become available in coming years. So the standard mode (48 kHz sampling frequency) will be the most popular mode for the time being.

2) PLAY Only Modes

The play-only modes include the following two modes:

(1) Normal track (2 hour) mode
(2) Wide track (contact print) mode

* Contact print in one of DAT tape dubbing methods in which a source tape is in physical contact with the destination tape during dubbing process for mass program production. In this mode the recording time is a relatively short 80 minutes.

Mode / Item	Rec./Play mode				Play-only mode	
	Standard mode	Option (1)	Option (2)	Option (3)	Normal track	Wide track
Specific application	BS (B) mode	BS (A) mode	Long rec./play mode (twice as long)	4-ch. mode	2 hours (13 μm tape)	Allows mass production by contact print.
Sampling frequency	48 kHz	32kHz	32 kHz	32 kHz	44.1 kHz	44.1 kHz
Upper limit of playback frequency	22 kHz	15 kHz	15 kHz	15 kHz	20 kHz	20 kHz
No. of quantization bits	16-bit, linear	16-bit, linear	12-bit, non linear	12-bit, non linear	12-bit, 16-bit linear	16-bit, linear
No. of channels	2 ch	2 ch	2 ch	4 ch	2 ch	2 ch
Recording time	2 hours	2 hours	4 hours	2 hours	2 hours	80 minutes
Tape speed	8.15 mm/s	8.15 mm/s	4.075 mm/s	8.15 mm/s	8.15 mm/s	12.225 mm/s

Table 1–2

4. R-DAT Recording Format

1) Track Format

The figure below shows the recording format for one track on the DAT tape.

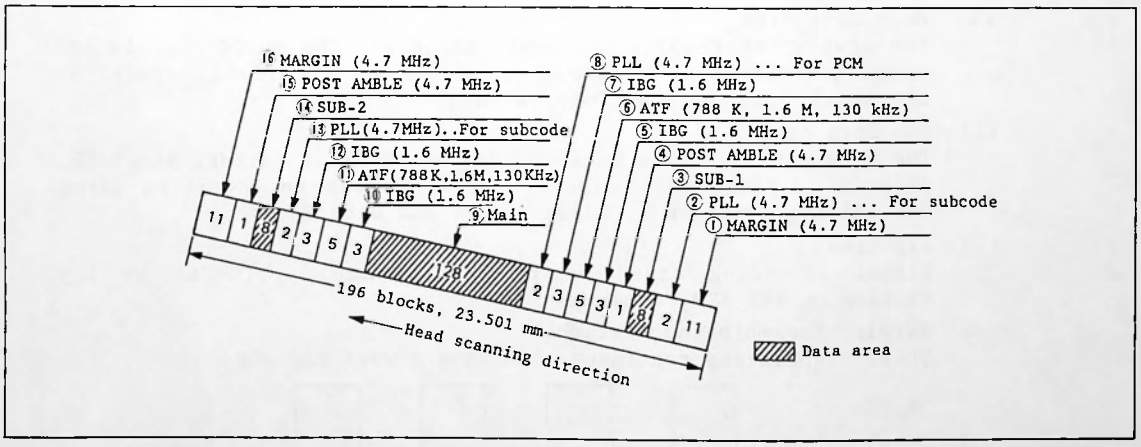


Fig. 1–10

Each of data items shows above contain the signals shows in table 1-3.

		Signal	Angle (deg.)	Number of block	Period (μs)
(1)	MARGIN	1/2 f ch	5.051	11	420.9
(2)	PLL (SUB)	1/2 f ch	0.918	2	76.5
(3)	SUB-1		3.673	8	306.1
(4)	POST AMBLE	1/2 f ch	0.459	1	38.3
(5)	IBG	1/6 f ch	1.378	3 (2)	114.8
(6)	ATF		2.296	5 (7.5)	191.3
(7)	IBG	1/6 f ch	1.378	3 (1.5)	114.8
(8)	PLL (PCM)	1.2 f ch	0.918	2	76.5
(9)	Main		58.776	128	4898.0
(10)	IBG	1/6 f ch	1.378	3 (2)	114.8
(11)	ATF		2.296	5 (7.5)	191.3
(12)	IBG	1/6 f ch	1.378	3 (1.5)	114.8
(13)	PLL (SUB)	1/2 f ch	0.918	2	76.5
(14)	SUB-2		3.673	8	306.1
(15)	POST AMBLE	1/2 f ch	0.459	1	38.3
(16)	MARGIN	1/2 f ch	5.051	11	420.9
	Total		90	196	7500

Recording density ..... 61.0 KBPI
f ch ..... 9.408 MHz

*Calculated under the condition that 30 ϕ - 90° deg. wrap angle, 2000 rpm cylinder is used.

( ): Wide track

Table 1–3

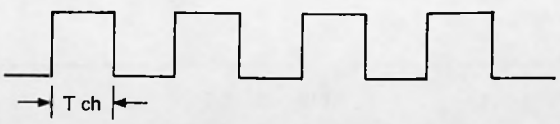
Each track has a length of 23.501 mm (7.5 ms) and contains 196 blocks. The track shown in the figure consists of the main data area (128 blocks), ATF area (10 blocks), and Sub data area (16 blocks): a total of 154 blocks. The remaining 42 blocks are used for data reading signals.

(1) Main Data Area
The area which records the music signals. The music signals and error correction codes are interleaved and recorded. (Refer to the section on the Main Data Format.)

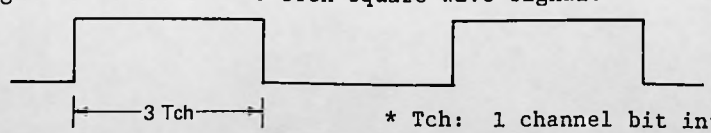
(2) Sub Data Area
The area which records data consisting of track number, start ID, skip ID, A-time, etc. These data items can be rewritten using the editing function. (Refer to the Sub Data Format.)

(3) ATF Area
Signal recording area for tracking control. (Refer to the section on the ATF Format.)

(4) Margin, Preamble and Postamble
These signals are continuous Tch square wave signals.

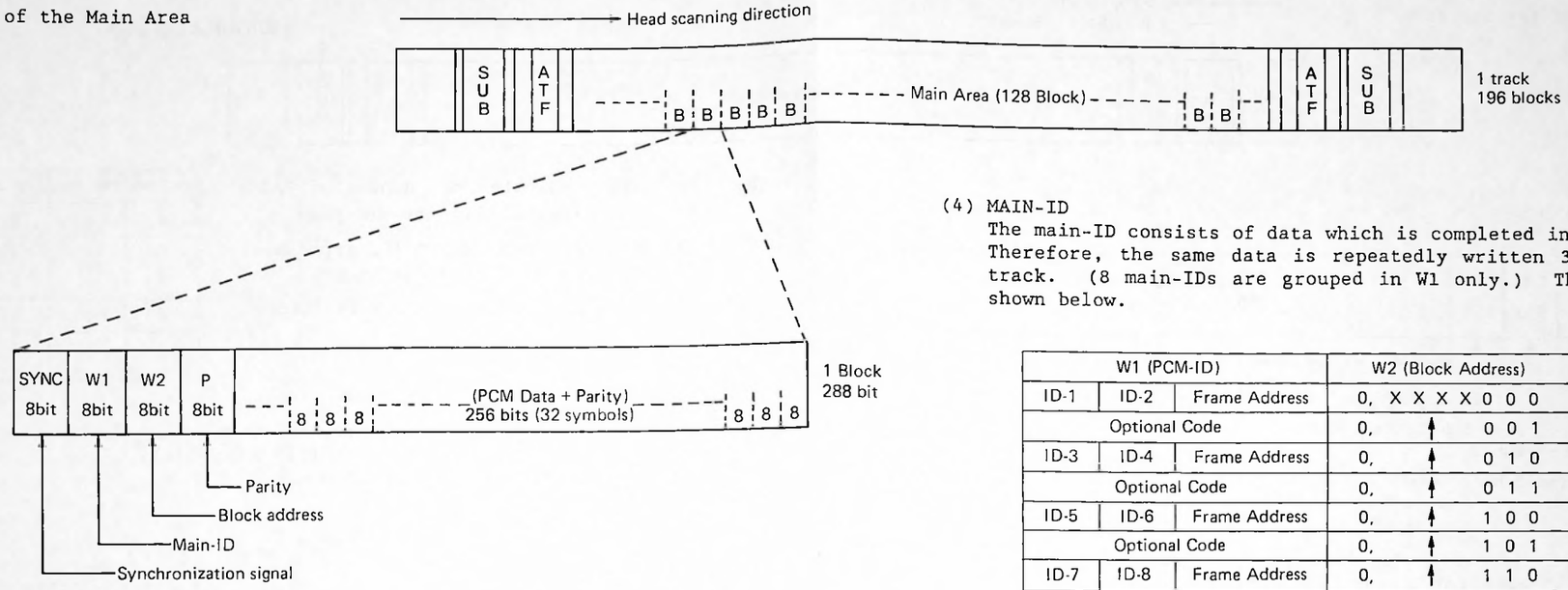


(5) Interblock Gap (IBG)
This signal is a continuous 3Tch square wave signal.



* Tch: 1 channel bit interval

2) Data Format of the Main Area

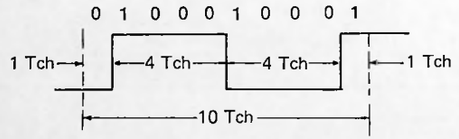


1. Main Area

The data in the Main area consists of the items shows in the figure. The data area contains the music data and the C1 and C2 error-correcting codes. The data shows in the figure above is found 128 times in one track. However, unlike the subcode data in which the same data is repeated, the track contains interleaved music data which is arranged in sequence. Main-ID (W1) in the Main area contains the Main area format shows in figure.

2. Block Format

(1) Synchronization Signal Pattern
The 8-bit synchronization signal has a 10 channel bit length as shown below.



(This pattern may also be reversed.)

(2) Block Address
The 7 bits from the LSB in W2 represent the block address (0-127) in one track. The MSB (1 bit) is an ID bit which identifies the main data block or sub data block. (0: Main data block)

(3) Parity
P, the MAIN-ID parity, is an error detect sign for W1 and W2.

(4) MAIN-ID
The main-ID consists of data which is completed in 8 block units. Therefore, the same data is repeatedly written 32 times in one track. (8 main-IDs are grouped in W1 only.) The contents are shown below.

W1 (PCM-ID)			W2 (Block Address)
ID-1	ID-2	Frame Address	0, X X X X 0 0 0
Optional Code			0, ↑ 0 0 1
ID-3	ID-4	Frame Address	0, ↑ 0 1 0
Optional Code			0, ↑ 0 1 1
ID-5	ID-6	Frame Address	0, ↑ 1 0 0
Optional Code			0, ↑ 1 0 1
ID-7	ID-8	Frame Address	0, ↑ 1 1 0
Optional Code			0, ↑ 1 1 1
MSB		LSB	MSB LSB

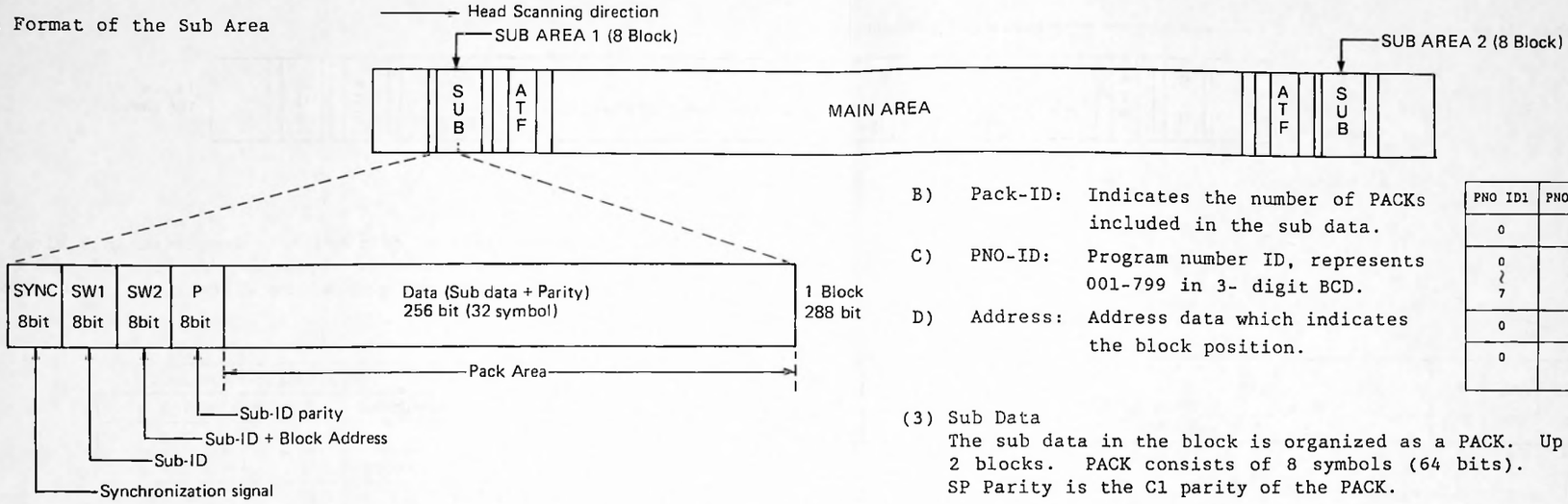
ID-1 (format)	ID-2 ~ ID3	Connection
0 0 (Audio use)	ID-2 (Emphasis)	00: off 01: Pre-Emp 10, 11: Reserved (for orther Pre Emph)
	ID-3 (Sampling freq.)	00: 48 kHz 44.1 kHz 10: 32 kHz 11: reserved
	ID-4 (No. of CH)	00: 2 CH 01: 4 CH 10, 11: reserved
	ID-5 (Quantization)	00: 16bits linear 01: 12 bits non-liner 10.11: reserved
	ID-6 (Track pitch)	00: 13.6μm 01: 20.4μm 10: 11: reserved
	ID-7 (Copy inhibit)	00: Digital copy permitted 01: reserved 10: Digital copy prohibited 11: Digital copy once
	ID-8	32 ID-8's constitute PACK.

A) Frame Address
Two tracks in one frame have the same frame address (0000 to 1111 is repeated).

B) ID-1 Format ID
Category code which indicates the purpose of the main data and main-ID. (00: Audio, 01: Data)

3. Main Data
One main data block consists of 32 symbols. Data and data parity (P, Q) are interleaved in the 32 symbols.

3) Data Format of the Sub Area



1. Sub Area

There are 2 sub areas in one track, sub-1 and sub-2. Each contains 8 blocks for a total of 16 blocks. The sub data is located in the sub-ID and pack area, and consists of A-time, program number, start ID, etc. The data in this area can be rewritten during post recording.

2. Block Format

(1) Synchronization Signal Pattern: Same as the main data block.

(2) Sub-ID

The sub-ID and sub data are completed in 2 blocks. The data contents are shown below.

	SW1		SW2			SUB-ID Parity	Sub Data			
SYNC	Control ID	Data ID (0000)	1	Pack ID	Address XXX0	Sub-ID Parity	Pack 1	Pack 3	Pack 5	Pack 7
SYNC	PNO ID3	PNO ID2	1	PNO ID1	Address XXX1	Sub-ID Parity	Pack 2	Pack 4	Pack 6	SP Parity

A) Control ID (DATA ID = 0000: For audio use) Pack ID

3	2	1	0

TOC-ID	1	This program is entered in the TOC.
	0	This program is not entered in the TOC.
Shortening ID (skip ID)	1	The beginning of shortening play, 33 3 frames (the end of shortening play is S - ID = 1).
	0	Not the beginning of shortening
Start-ID	1	The start of a program, recorded 300 30 frames continuously.
	0	Middle of program
Priority-ID	1	PNO-ID is recorded and is well defined program number where priority-ID = 1.
	0	PNO-ID is not recorded or is ambiguous.

B) Pack-ID: Indicates the number of PACKs included in the sub data.

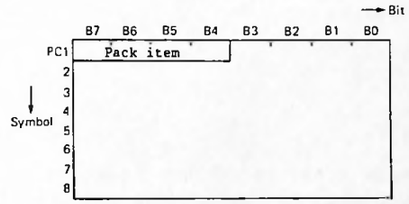
C) PNO-ID: Program number ID, represents 001-799 in 3- digit BCD.

D) Address: Address data which indicates the block position.

PNO ID1	PNO ID2	PNO ID3	
0	0	0	No program number
0 ≀ 7	0 ≀ 9	1 ≀ 9	Program number in 3-digit BCD
0	B	B	Read in area
0	E	E	Read out area (END ID uses this)

(3) Sub Data

The sub data in the block is organized as a PACK. Up to 7 can be recorded every 2 blocks. PACK consists of 8 symbols (64 bits).
SP Parity is the C1 parity of the PACK.



* PACK format (8 bytes) The first 4-bit ITEM represents the contents of the PACK.

Item	Mode	Contents
0000	No information	PC1 - PC8 all are "0"
0001	Program time	PNO, Index and continuous time code within program
0010	Absolute time	PNO, Index and continuous time code on a tape
0011	Running time	PNO, Index and continuous time code within one recording
0100	TOC	The table of contents
0101	Calender	Year, Month, Day, The day of the week, Hour, Minute, Second
0110	Catalog	The catalog number of the cassette
0111	ISRC	The international-standard-recording code
1000	Pro-binary	Professional use
1001	Character	Character or symbol information
1010	Reserved	
1011	Reserved	
1100	Reserved	
1101	Reserved	
1110	Reserved	
1111	Reserved	Defined by the pre-recorded tape

3. The data in the sub code is completed in 2 blocks. Therefore, the same data is repeatedly recorded 8 times in one track (4 times in sub area 1 and 4 times in sub area 2). The DAT data is completed in one frame and the same data is recorded 8 times in the other track for a total of 16 times.

5. Error Correction Mechanism on R-DAT

Audio signals are sampled at a frequency of 48 kHz and quantized at an accuracy of 16 bits. Digitalized audio data is subjected to various processings (such as 16 8 + 8 and 8-10 modulation) before being recorded on tape.

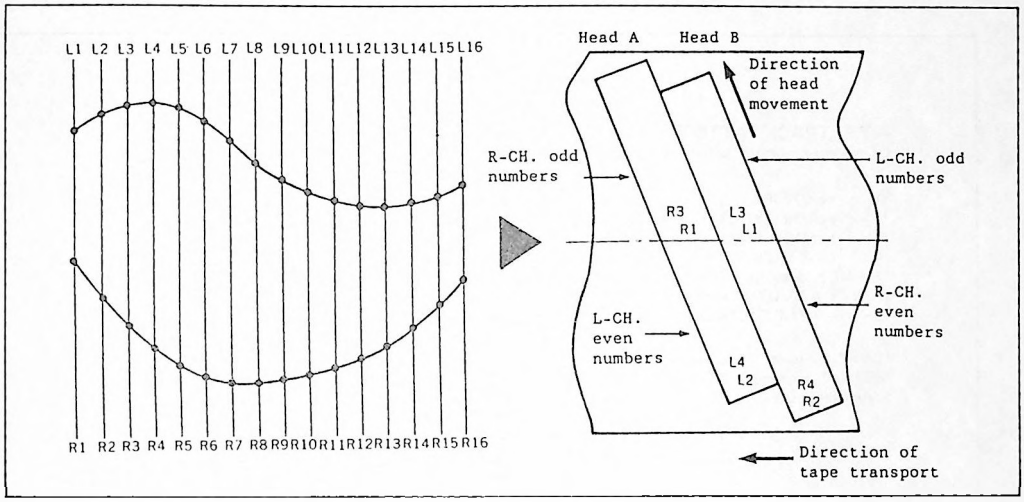


Fig. 1—11

The interleave technique is used for data recording, in which recording data is scattered to separate area on tape so that data dropouts may be interpolated in the course of playback.

The DAT uses double interleave: i.e. inter track interleave and intra track interleave. This means that two scans and two tracks are required to complete an interleave sequence. The following figure shows correctable areas and interpolatable areas. If data dropouts have consecutively occurred along the length of a tape, up to 22 blocks or up to 796 symbols are correctable. Also up to 74 blocks or 2664 symbols can be interpolated.

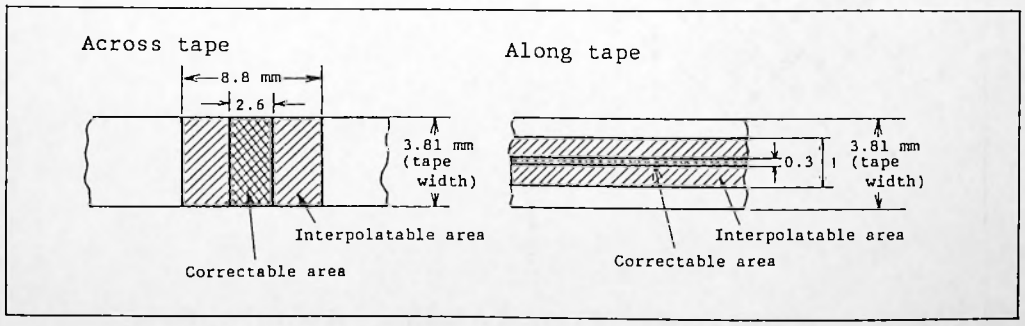
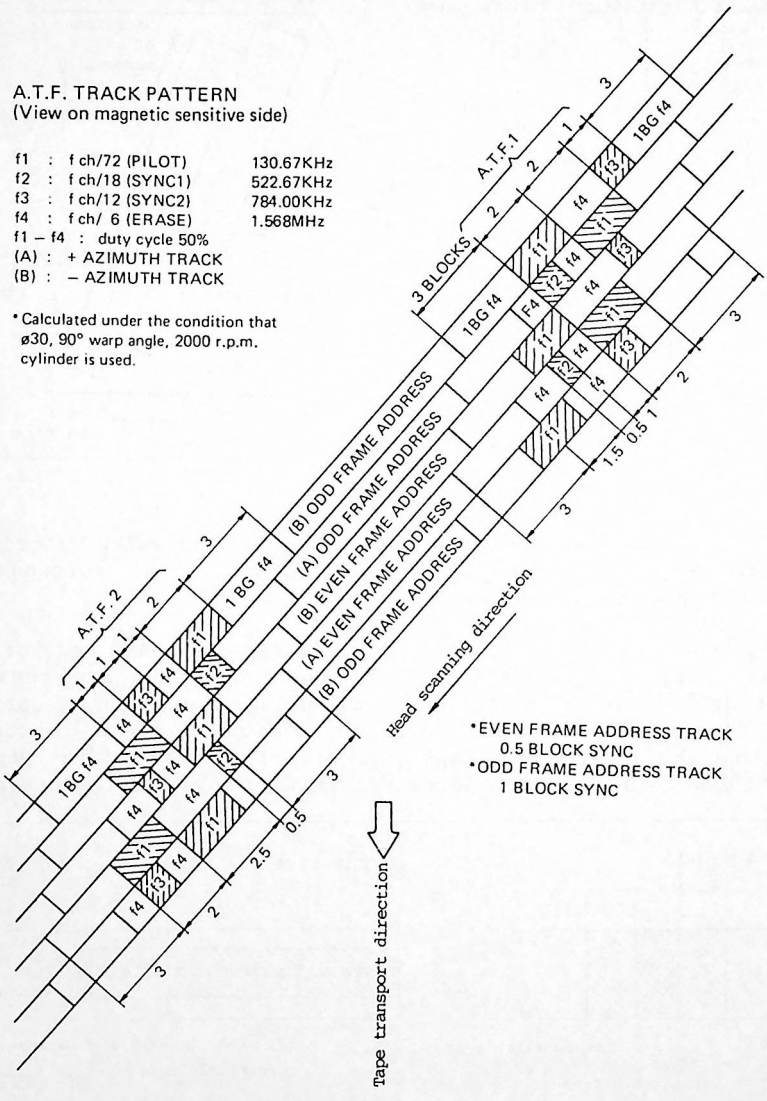


Fig. 1—12

Theoretically, this type of data arrangement permits the sound to be output even if one of the two heads becomes disconnected.

6. ATF (Automatic Track Finding) Operation Mechanism

1) The ATF is an automatic tracking servo mechanism that controls the heads to properly trace the track (each 13.6 μm wide). This technique is also called the area division ATF which uses the ATF signal prerecorded on tapes.



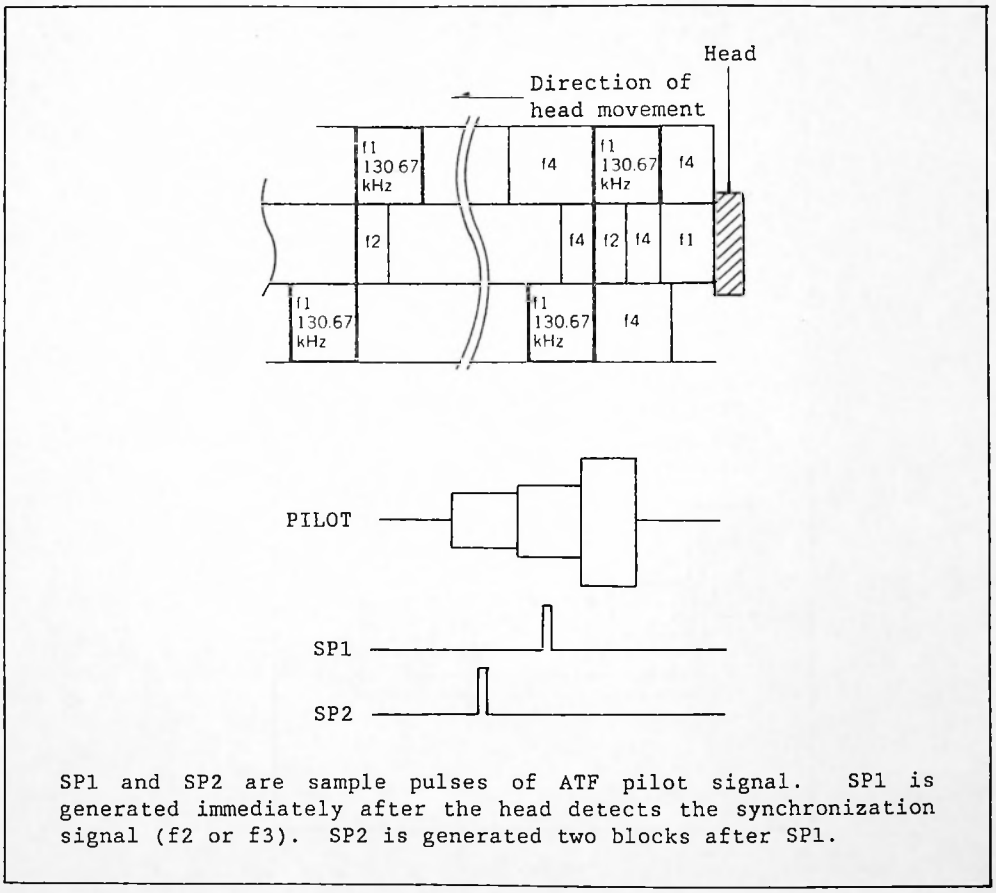
There are four types of ATF recording patterns. These four patterns prevent the ATF from locking across the opposite azimuth track. These patterns are repeatedly recorded.

Fig. 1–13

2) The ATF signal consists of ATF1, data signal, and ATF2. It is a combination of four signals with frequencies of f1 (130.67 kHz), f2 (522.67 kHz), f3 (784 kHz), and f4 (1.568 MHz). On both sides of the ATF signal block are marginal spaces called IBG (inter block gap).

Signal f1 is a pilot signal which provides the major ATF function, while signals f2 and f3 are synchronization signals.

The following figure is an expansion of a part of the ATF track pattern (head A track just below the top track).

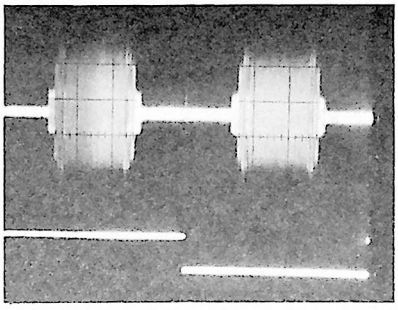


SP1 and SP2 are sample pulses of ATF pilot signal. SP1 is generated immediately after the head detects the synchronization signal (f2 or f3). SP2 is generated two blocks after SP1.

Fig. 1—14

3) When the head is tracing a head A track, it picks up the f1 signals on the adjacent tracks (upper and lower tracks in the figure above) as inter track crosstalks. The servo can control tracing so that the crosstalk from both adjacent tracks is always equal. The tracking error signal is fed back to the capstan motor driver to control capstan rotation speed.

4) RF Playback Signal



The head reads data off the tape over a cylinder angle of 90 deg.
The bursts in this photo are the signals read off the tape.

Fig. 1–15

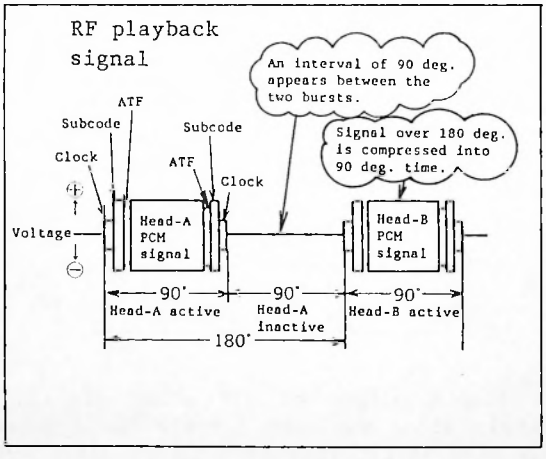


Fig. 1–16

In a 30 mm diameter cylinder system, the tape's wrap angle is 90°. The data recorded on or played from the tape is compressed by 1/2 into an intermittent signal.

7. R-DAT Tape Construction

The R-DAT tape cassette has a sealed construction to prevent contamination from dusts, fingerprints, etc.

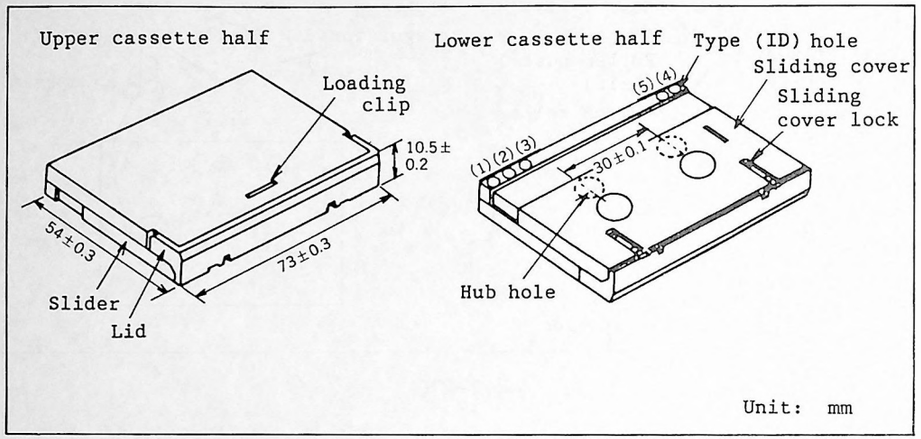


Fig. 1–17

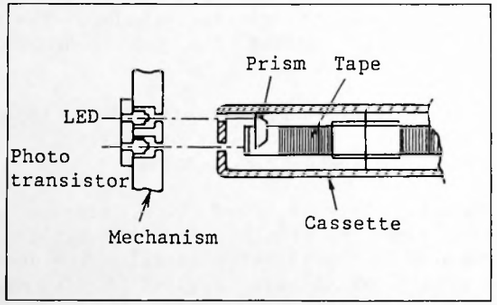


Fig. 1–18

Clear leading tapes are spliced at the beginning and end of the tape so that the deck can detect them. For this purpose the tape cassette contains a prism. An external LED beam transmitted through the clear leading tape is folded back through the prism, and detected by a phototransistor. The deck automatically stops the tape at the beginning and end of the tape to prevent tape break accidents.

The metal tape coating is ultra fine alloy particles composed of iron, nickel, and cobalt.
The tape cassette contains a braking mechanism which prevents tape slack. Also it has five type (identification) holes. Erasure prevention is achieved by closing the sliding cover that covers the erasure prevention hole at the back of the cassette.

"1": Hole present
"0": No hole

ID hole (1)	ID hole (2)	ID hole (3)	
0	0	0	Metal tape or equivalent; tape thickness 13 μm
0	1	0	Metal tape or equivalent; thin tape
0	0	1	Track pitch 1.5 times; tape thickness 13 μm
0	1	1	Track pitch 1.5 times; thin tape
1	x	x	Auxiliary

ID hold (4)	
1	Prerecorded music tape
0	Normal blank tape (for rec./playback)

ID hole (5)	Erasure prevention hole

Table 1–4

8. R-DAT Mechanism Description

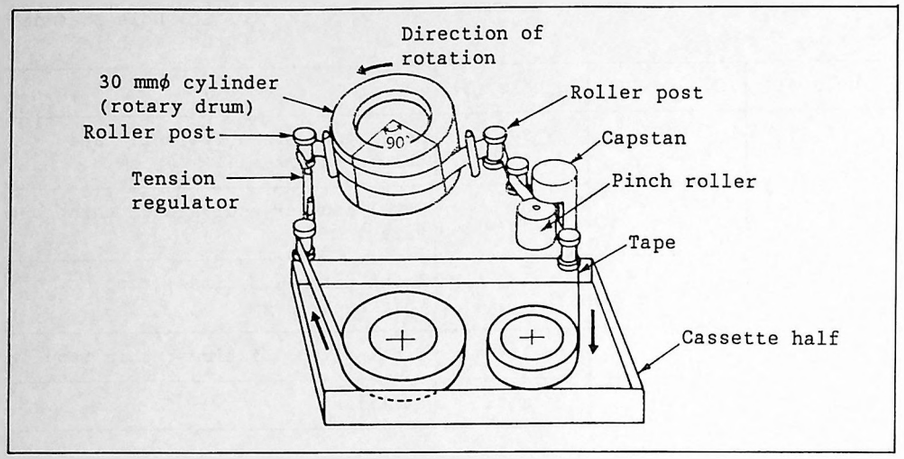


Fig. 1–19

The R-DAT equipment employs the helical scan (diagonal recording) system using rotary cylinder. Long recording duration is achieved with the guard band less recording technique. In order to prevent inter track crosstalk, the equipment also employs the azimuth technique.

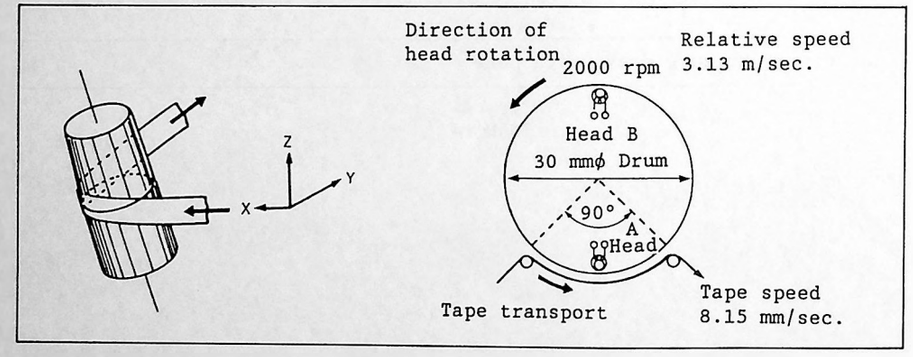


Fig. 1–20

The tape is wrapped on the cylinder over an angle of 90 degree. The cylinder has a diameter of 30 mm, and rotates at a speed of 2000 rpm.

Since the absolute tape speed is 8.15 mm/sec., the relative tape speed to the heads is 3.13 m/sec.

1) Tape Transport Mechanism

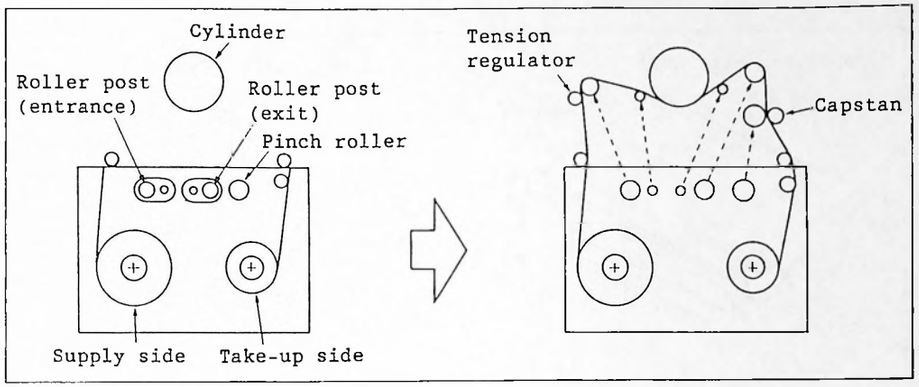


Fig. 1–21

* The roller posts pick up the tape out of the cassette and brings it into contact with the rotary cylinder. The tension regulator moves sidewise to control the tape tension applied to the cylinder to a constant value.

* Like the conventional audio cassette decks, tape transport on the DAT is accomplished by a capstan and roller.
The absolute tape speed is 8.15 mm/sec.

* Tape information (presence of tape, erasure prevention, music tape, blank tape, material, and thickness) is identified by ID holes provided in the cassette itself. The deck has six ID hole sensing inputs which are applied to a system controlling processor.

In order to ensure that the heads properly trace the tacks on the tape, the capstan is servo controlled. Proper tracking is achieved by controlling the capstan rotation speed and thus controlling tape transport speed.

9. R-DAT System Configuration

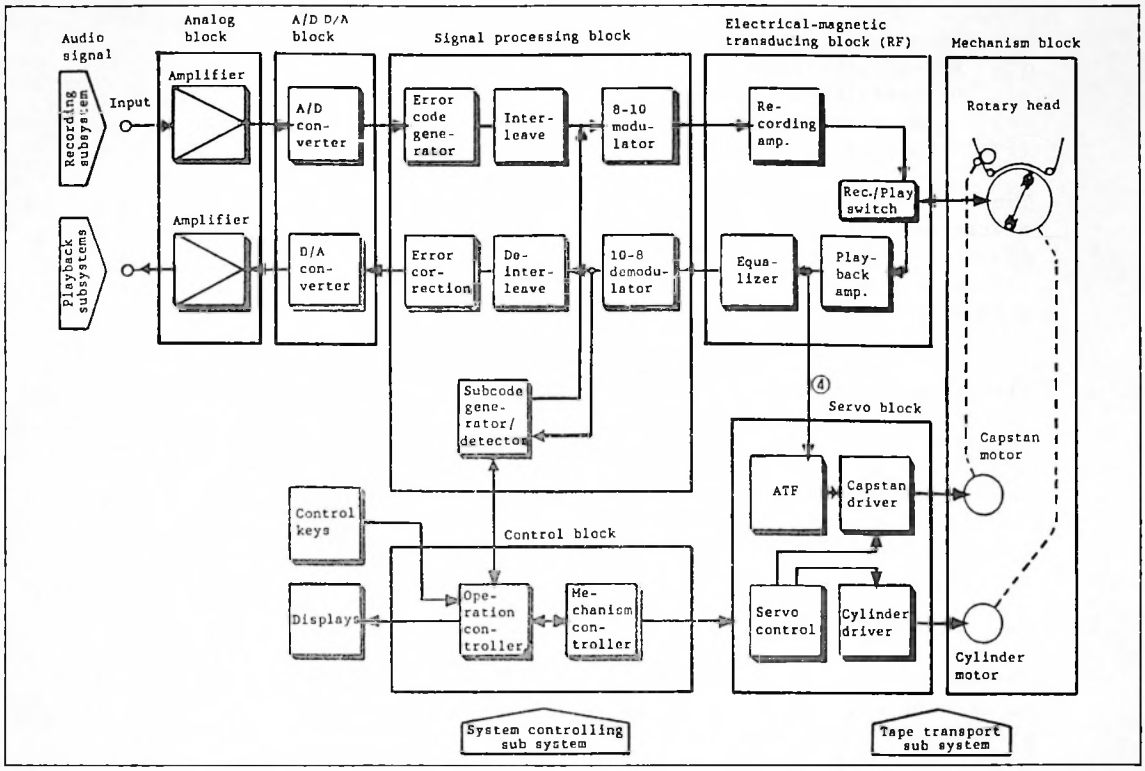


Fig. 1–22

The R-DAT system consists of 6 major blocks.

1) A/D and D/A Block

The A/D converter converts the audio signal into a PCM signal. The sampling frequency is 48 kHz in the standard mode. Quantization is performed in 16 bits. The digital data bits for the left and right channels are sent in serial to the signal processor.
The D/A converter converts the 16-bit data from the signal processor to an analog signal.

2) Signal Processing Block

This block performs all the signal processing operations for the R-DAT system. Usually, this block consists of a signal processing LSI chip and externally connected RAM.

<Main Operations During Recording>
(1) Parity code generation for error correction
(2) Interleave
(3) 8-10 conversion
(4) Sub code data generation (sub ID, main ID, sub data)
(5) ATF signal generation, generation of signals such as synchronization signal, address signal, etc.
(6) Creation and output of compressed data in the R-DAT format

<Main Operations During Play>

(1) 10-8 conversion
(2) Error correction
(3) De-interleave
(4) Separation and demodulation of PCM data and sub code data
(5) Output of 16-bit left and right serial data

Thus, the signal processing block performs many digital data processing operations in a short time. Beside these operations, clocks and master clocks required for the various sampling frequencies (32 kHz, 44.1 kHz, 48 kHz) are generated. A modulator and demodulator for digital I/O are also provided.

3) Electromagnetic Converter Block

Usually called the RF circuit. During recording, the recording amplifier controls the signal supplied to the head. During playback, the played signal is amplified, waveshaped and equalized, and converted to digital data. This block handles digital signals having a wide range of frequencies from 130 kHz to 4.7 MHz.

4) Control Block

This block consists of the system microcomputer, mechanism microcomputer, etc. The system microcomputer controls the overall system such as mode setting for the various blocks, FL meter display, key inputs, etc. The mechanism microcomputer controls the operation of the mechanism based on information from the system microcomputer.

5) Servo Block

This block consists of a servo circuit which rotates the cylinder motor and capstan motor at fixed speeds. The motors which were started based on information from the system control rotate at fixed speeds as a result of speed control and phase control using the FG and PG signals. During playback, the capstan motor is controlled by ATF control and tracking control is performed so that the head travels properly in the center of the track. During FF/REW, the reel servo mode is activated using the reel FG signal. The servo functions so that the sub code information can be read even during FF/REW.

6) Mechanism Block

Very similar in construction to a video recorder, a precision mechanism is used to allow the head to properly trace the extremely narrow track (13.6 μm). The mode setting for the mechanism is performed by command from the mechanism microcomputer using the mode motor and mode detect switch.

10. R-DAT Servo Control System

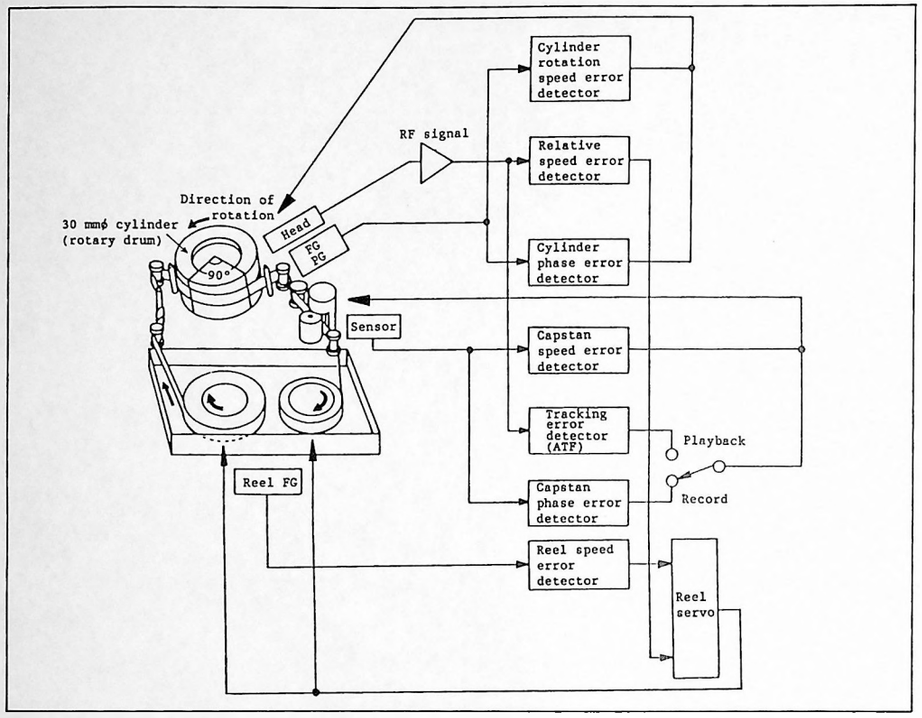


Fig. 1–23

The R-DAT's servo system includes three servo subsystems: cylinder, capstan, and reel servos. Each of these servos uses the digital servo technique that feeds back motor speed (detected by FG, PG, etc.) to the motor driving voltage. Since the rotary cylinder must cover a broad range of speed from 1000 to 3000 rpm, the cylinder servo uses the FG and PG for better speed accuracy.

Cylinder Servo

1) REC/PLAY: Speed and phase control (2000 rpm and, 100/3 Hz in the standard mode).
2) FF/REW: Speed control by FG detection. Step-up and step-down increments: 25, 50, 75, 100, 150, and 200 times to normal speed. 2000 - 3000 rpm in FF mode; 2000 to 1000 rpm in REW mode.

Capstan Servo

1) REC: Speed and phase control (tape speed 8.15 mm/sec.)
2) PLAY: Speed and ATF control (tape speed changes if tracking error occurred).

11. Q&A

Question	Answer
How are audio signals digitally recorded?	The input "analog" audio signal is first sampled at a rate of 48 kHz. Individual signal levels of the sampled segments are digitally coded into 16-bit data and recorded on a tape. Digitally-coded audio data is recorded in the form of a series of ones and zeros, as with the case of compact discs.
How are recorded tapes erased without an erase head?	Tape erasure is accomplished by overwriting new data on old data. So no erase head is needed.
Doesn't the tape sustain damage at the 200-times faster transport speed?	Since the normal tape speed in Rec./Play mode is a very slow 8.15 mm/sec., the 200-times faster tape speed is 1.63 m/sec. which is comparable to that in FF mode on conventional cassette decks. At the beginning and end of tape, the tape slows down to 100-times faster speed to prevent possible damage to the tape.
What are the digital input/output connectors for?	These digital I/O connectors allow the user to directly input/output digital audio data without going via the deck's internal A/D or D/A converters. They give the deck a compatibility with future completely digitalized audio systems. These connectors may also be used for digital dubbing from one DAT to another.
What types of pre-recorded music tapes will be available?	Prerecorded digital music tapes use the same sampling frequency as that for compact discs: 44.1 kHz. They are available in normal- and wide-track tapes. The wide-track tapes require a tape speed 1.5 times faster (12.225 mm/sec.) than the normal-track tapes and have a maximum play time of 80 min.
To what level are errors on a contaminated or damaged tape correctable?	The error correction feature corrects read errors. Also the interpolation feature corrects up to about 25,000 bits of dropout. Should the head gap in one of the two heads get clogged, the deck can reproduce a signal nearly equal to the original signal.
What is digital dubbing?	Digital dubbing means to copy one digitally-recorded tape to another in digital form, without converting it into analog form.
Is it possible to copy from compact discs?	No, because DAT's recording sampling frequency (48 kHz) is different from the CD's sampling frequency (44.1 kHz).

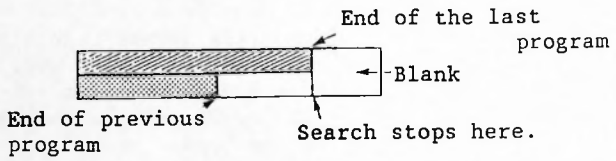
Question	Answer
Is it possible to program rec./play with timer?	With an optional audio timer, yes. The deck requires an overhead time of about 20 seconds before it starts recording after power on. When setting the timer, take this interval into account.
Is there any means of cleaning the rotary heads?	A cleaning tape (RT-RCL) designed for DATs is available. Use it one per month or any time if the playback sound has noise or distortion.
How does the end search feature function?	If the previous program has not been erased, search stops at the end of the previous program. 
Are there any precautions during installation?	The deck should be installed in a place isolated from ambient vibration sources. Also it should not be tilted more than 5 deg. longitudinally.

Table 1–5

– MEMO –

1. Overviews

1-1 Overview of the SV-DA10

1) Switches and Functions

2) Display

1-2 Operations

1) Play and Search

2) Recording

3) Subcode Post-Recording

1-3 Serial Copy Management System (SCMS)

1) Overview and Purpose of SCMS

2) SCMS

3) Functions of the SCMS

4) Description of SCMS

1-1 Overview of the SV-DA10

1) Switches and Functions

a. Basic Switches
open/close
play
stop: Can also be used as a program clear key.
reverse music skip: If pressed during pause, pauses after search.
reverse music skip: If pressed during stop or play, plays after search.
rew/rev: If pressed during stop or x400 rew, rewinds at x225. If pressed during x250 rew, rewinds at x400.
ff/cue: If pressed during stop or x400 ff, fast forwards at x250. If pressed during x250 ff, fast forwards at x400.

b. Timer Related Switches
timer rec
timer play

c. Recording Related Switches
analog/digital input
select: LED is ON during digital input.
fade in: If pressed during rec pause, rec play starts and the level increases at the set time constant.
fade out: If pressed during rec play, the level decreases at the set time constant, auto rec mute turns ON and then rec pause.
PNO/start-ID auto: Auto mode when power is turned ON.

d. Play and Search Related Keys
skip play cancel: Skips play mode when power is turned ON.
end search: Searches for OEE (end mark) or an approximately 7 cm continuous blank portion.
shuttle switch: Functions even at the pause position. (Pause after cue/rev.)

Start mode	← center →
play	-15.-9.-5.-3 .play .+3 .+5.+9.+15
pause	- 3.-2.-1.-1/2.pause.+1/2.+1.+2.+ 3

e. Post-Recording Related (For details, see E. Subcode Post-Recording.)
start-ID: Sets the start-ID post-recording mode
skip-ID: Sets the skip-ID post-recording mode
end: Sets the end post-recording mode
ID write: ID write start command
ID erase: ID erase start command

f. Counter Related
counter mode: A-time → P-time → remain → TOC display → counter
counter reset:

2) Display

a. FL

1. Level Meter
   Over to -60 dB is displayed in 26 segments. Provided with an approximately one second auto peak hold function.

2. Counter
   The display changes as follows each time the counter mode key is pressed.
   - <1> A-time: Displayed from the subcode play value. If A-time cannot be played, tape travel display is shown.
   - <2> P-time: Displayed from subcode play value or calculated value. If P-time is invalid, tape travel display is shown.
   - <3> remain: The remaining tape time is calculated from the rotational speed of the reel and displayed. Displayed to nearest minute. (To the nearest second for TOC recorded tape or prerecorded tape.) Tape travel display is shown during time calculation.
   - <4> TOC: Total time is displayed only for tapes on which R-TOC and U-TOC have been recorded. During play, Fs is flashed if a signal which does not permit digital copying is output.
   - <5> counter: Eight counts are displayed for each rotation of the take-up reel. Counter reset is valid only in this display mode.

3. PNO
   - <1> PNO: Normally the program number of the current tape position. Target PNO during direct search or program search. Number of skips during skip (skip program).
   - <2> TOC: Total number of programs is displayed only when the counter mode is TOC.

4. Sampling Frequency Display
   Sampling frequency for play or recording is displayed. Flashes when a tape that does not permit digital copying is played in the TOC display mode.

5. ID Display
   - <1> start-ID: ON during play or recording. Flashes during standby or erase.
   - <2> end: ON when end is reached at play or x250 ff in end search.
   - <3> erase: Flashes during standby and ON during erase.

6. Others
   - <1> repeat: ON for all or program repeat mode.
   - <2> cleaning: ON when the error rate is 10-1 or more in five seconds to indicate head cleaning is required.
   - <3> dew: Dew (condensation) warning indication.

b. LED

1. Modes of Operation

<1> play:	Normal play	ON
	Search	Fast flashing
	Play during music scan	Slow flashing
<2> pause:	Normal pause or rec pause	ON
	Search (when entering the pause mode after search)	Flashing
	Still protection	Flashing
<3> rec:	Normal rec play or rec pause	ON

2. Others

<1> PNO/start-ID auto:	Auto mode (at power on) ..	ON
<2> skip play cancel:	Invalid skip-ID	ON
<3> digital:	Digital input selected	ON
	Digital input recording inhibited ..	Flashing

1-2 Operations

1) Play and Search

1. Normal Play
When the play key is pressed, the play indicator turns on and play begins.

a. Error Rate During Play
When the error rate exceeds 10^{-1} for 5 seconds or more, the cleaning indicator turns on. When the error rate increases further, muting is activated.

b. Auto-Rewind Function
The end of tape is determined in the following situations and auto-rewind is activated.
1. When the end mark (PNO-ID=0EE) was played.
2. When the very end of the tape was reached.

c. Counter Display
The display changes in the following manner each time the counter mode key is pressed.

Note 1 Note 2

Absolute time (A-time) → Program time (P-time) → Remaining time (remain) → Total time (TOC) → Tape counter

Note 1:
Absolute time (A-time) is displayed when the power is turned on or when the tray is open.
Note 2:
Fs is flashed while a copy inhibited tape is played with the serial copy management system.

d. Tape Travel Display
The tape travel display is shown in the following situations.
1. When playing an unrecorded portion.
2. When a valid value cannot be obtained in the A-time, P- time or TOC display modes (if the subcode has not been recorded).
3. When calculating the time in the remain display mode.
4. When ff or rew is performed at x400.

2. FF/REW

a. FF
1. If pressed during stop or x400 ff, the mode switches to x250 ff.
If pressed during x250 ff, the mode switches to x400 ff.
2. x250 ff: Forwards tape while reading subcodes.
3. x400 ff: High-speed fast forward.

b. REW
1. If pressed during stop or x400 rew, the mode switches to x225 rew.
If pressed during x225 rew, the mode switches to x400 rew.
2. x225 rew: Rewinds tape while reading subcodes.
3. x400 rew: High-speed rewind.

The speed is reduced near the tape's beginning and end to protect the tape.

3. Skip Search
   1. Skips to the nth program when ◀◀ or ▶▶ is pressed n times during stop, play or pause.
   2. While searching during skip, the PNO display shows the number of skips with ±n.
   3. The search proceeds at x250 based on the start-ID.
      The play or pause indicator flashes during search. (This also applies to the search operations below.)
   4. The PNO display is restored after search.
   5. If programs are skipped during pause or if the pause key is pressed during search, the pause mode is selected after the search.
   6. If programs are skipped during stop or play or if the play key is pressed during search, the play mode is selected after the search.

4. Direct Search
   1. If the PNO is specified with the numeric keys on the remote controller and the play key is pressed, the program with the PNO which was directly set is searched for and play begins from the beginning of the specified program.
   2. If the PNO is specified with the numeric keys on the remote controller and the pause key is pressed, the program with the PNO which was directly set is searched for and play pauses at the beginning of the specified program.
   3. The display during search is the same as in program search.

5. Program Search
   1. The PNO is specified with the numeric keys on the remote controller and programmed with the memory key.
   2. A total of up to 32 programs can be programmed in the same manner.
   3. When the play key is pressed after programming, play begins in the programmed sequence.
   4. When the pause key is pressed after programming, the first programmed program is searched for and the pause mode is entered.
   5. The ▶▶ key during program play searches for the next program.
      The ◀◀ key during program play searches for the previous program.
      (Searches the program being played if pressed only once.)
   6. The recall key on the remote controller permits the programmed sequence to be confirmed.
   7. When the stop key is pressed, the programmed sequence is cleared.
   8. If a blank, start-ID skip-ID end, end of tape, missing skip-ID envelope is detected, the next programmed program is searched for.

6. Repeat Play
   1. When the repeat key on the remote controller pressed, the repeat play mode is entered.
   2. If programs have been programmed, the programmed programs are played repeatedly for 16 times.
   3. If programs have not been programmed, all programs are played repeatedly for 16 times.
   4. The B. 1. b. auto-rewind function also operates during repeat play.
   5. When the stop key is pressed, the repeat play is cleared.

7. Cue/Rev

a. Shuttle Search (variable speed cue/rev)

When the shuttle dial is rotated in the play or pause mode, the play (cue/rev) changes to the speed shown below corresponding to the angle of rotation.

Initial Mode	rev				CENTER			cue	
pause	-3	-2	-1	-1/2	PAUSE	+1/2	+1	+2	+3
play	-15	-9	-5	-3	PLAY	+3	+5	+9	+15

b. Normal Cue/Rev

The play (cue/rev) changes to x3 only while the ff key or rew key is pressed in the play mode.

2) Recording

1. Mode Setting

a. Input Switching: Analog/Digital Selection

1. Analog or digital is selected with the input selector (locking switch) on the front panel. (The digital indicator turns on when digital is selected.)
2. After digital is selected, the optical input or coaxial input connector is selected with a rear panel switch.

b. PNO (start=ID) Recording Mode Setting

1. Auto Recording Mode

The auto key is pressed to turn on the auto indicator. (The auto mode is selected at power on.)

<1> During analog recording or digital recording from a non-DAT source, the PNO (start-ID) is automatically recorded as the audio begins output after a blank portion (-60 dB or less) continues for 2 seconds or more.

<2> During digital recording from a DAT source (category code is DAT), the start-ID is copied to the same position as the master tape.

Notes:

1. Same as (1) even for DAT if from the SV-3500, 360, SV-225 and 260A, since a general-purpose category code is output.
2. If P-time is 18 seconds or less, the next start-ID cannot be recorded.

2. Manual Recording Mode

<1> The auto key is pressed to turn off the auto indicator.

<2> The PNO (start-ID) is recorded each time the play key is pressed in the rec pause, rec play, or auto rec mute mode.

<3> If P-time is 18 seconds or less, the next start-ID cannot be recorded.

2. Adjustment at the Start of Recording

a. Setting the Tape Position at the Start of Recording

1. Recording from the Beginning of the Tape
   The rec key is pressed after the rewind key.
   The rec and play indicators turn on, the pause indicator flashes, and a blank portion is created for a specific duration to prevent an unerased portion from remaining at the beginning of the tape or to form a lead-in area when the tape has not yet been recorded.
2. Continuing Recording from the End of the Tape
   The end search key is pressed.
   The end mark or an unrecorded portion is searched for and the stop mode is entered.
   Next, the rec key is pressed to select the rec pause mode.
3. Recording at the Middle of the Tape
   * To ensure the continuity of the absolute times (A-TIME) and program numbers (PNO), it is desirable to press the rec key while the A-TIME (absolute time) and PNO (program number) are displayed to select the rec pause mode.
   * After checking the PNO of the previous program with the r skip (▷▷) key, ff or cue is used to search for the starting point.
   * To provide a clear separator with the portion recorded previously, it is recommended that a blank portion be created by pressing the auto rec mute key.

b. Recording Level Setting (for analog recording only)

1. The input to be recorded is connected to the input connector.
2. The rec key is pressed to select the rec pause mode.
3. The input level is adjusted (the balance control is also adjusted as needed).

3. Recording

a. Recording Start

1. Analog recording: The rec key is pressed and then the play key.
2. Digital recording: The rec key is pressed and the digital indicator is checked to see that it is lit. Then the play key is pressed.
   [1] In the following situations, the digital indicator flashes and recording cannot be performed.
      <1> The digital signal is not input at the specific level.
      <2> A copy inhibit signal is input with the serial copy management system.
   [2] If the digital signal cannot lock after recording begins, the recording is continued using Fs at which the digital signal was last locked.
   [3] If a signal in <1> or <2> of [1] is input after recording begins, the recording is continued while muted. When a recordable signal is input again, the muting is disabled.

b. Recording Pause

1. The pause key is pressed to pause (stop tape travel) during recording (rec play).
2. The play key is pressed to resume recording.

c. Auto Rec Mute Function

1. When the auto rec mute key is pressed during recording (rec play), an approximately 4 second blank portion is created and the rec pause mode is entered. If pressed for longer than 4 seconds, mute recording is performed for the duration pressed.
2. When the auto rec mute key is pressed during recording pause (rec pause), an approximately 4 second blank portion is created and the rec pause mode is entered.
3. When the play key is pressed during creation of a blank portion (auto rec mute), recording is resumed immediately and the rec play mode is entered.
4. When the stop key is pressed during creation of a blank portion (auto rec mute), recording is stopped immediately and the stop mode is entered.
5. When the pause key is pressed during creation of a blank portion (auto rec mute), recording is paused immediately and the rec pause mode is entered.

4. Fade In and Fade Out Functions

a. Fade In

1. The rec key is pressed: The rec pause mode is selected.
2. The fade in key is pressed: The mute recording (rec play) mode is selected, the level is digitally raised with the specific time constant and the normal recording (rec play) mode is selected.

b. Fade Out

1. Normal recording (rec play) mode
2. The fade out key is pressed:
   <1> Level is digitally lowered with the specific time constant.
   <2> An approximately 4 second blank portion is created (auto rec mute).
   <3> The rec pause mode is selected.

5. Others

a. Erase

1. When recording is performed, the previously recorded audio and subcode are automatically erased.
2. To erase only the audio, record with the input level set at min. 0.
3. The A-time is recorded continuously while the A-time is displayed.

3) Subcode Post-Recording

1. Start-ID (S-ID)

a. Recording

1. Initial Mode
   Stop, pause or play.
2. S-ID Selection: The [start-ID] key is pressed.
   [Start-ID] flashes rapidly.
   Lights when the start-ID is present and flashes when it is not.

3. Recording Mode Selection
   Auto PNO mode is selected at power on.
   [Auto PNO] turns on in auto mode.
   The [auto PNO] key is pressed to change the mode.
   [Auto PNO] turns off in manual mode.
- 1-3 are not shown in any particular order.

4. Setting the Recording Position
   Set with the [shuttle] switch.
   Set before the interval between programs for the [auto PNO] mode.
5. Record Start Command
   The [write] key is pressed.
   [Start-ID] turns on during S-ID recording.
   If the start-ID has been recorded, the tape is rewound to a position before the start-ID and the start-ID is erased. Then, the start-ID is recorded for 9 seconds from the tape position where the [write] key was pressed (in manual mode).
   [Start-ID] flashes during S-ID erase.
6. Stop Mode
   Pause or play.
   After the start-ID is recorded, the start-ID is erased for 9 seconds and the pause mode is entered even if the initial mode is stop.
- Steps 4 - 5 are repeated to post-record the start-ID in succession.

7. Clearing the Post-Recording Mode
   The [start-ID] or [stop] key is pressed. [Start-ID] turns on.
   The [skip-ID] is selected and start-ID post-recording is cleared even in the other post-recording modes.
   Note: Recording the start-ID may erase the previously recorded skip-ID and end.

b. Erase

1. Initial Mode
   Stop, pause or play.
2. S-ID Selection
   The [start-ID] key is pressed.
   [Skip-ID] flashes rapidly.
   Lights when the skip-ID is present and flashes when it is not.
- 1 - 2 are not shown in any particular order.

3. Recording Position Setting
   Set with the [shuttle] dial.
   When the position of the recorded start-ID is reached during tape travel, the indicator turns on.
   After direct search or skip search, the Start-ID of the searched program is erased.
4. Erase Start Command
   The [erase] key is pressed.
   [Erase] turns on during S-ID erase.
   [Start-ID] remains flashing.
   Even if the erase key is pressed at a tape position after the start-ID position, the tape is fed in the rew direction and the start-ID is searched for.
5. Stop Mode
   Pause or play.
   The pause mode is entered even if the initial mode is stop.
- Steps 3 - 4 are repeated to post-record the start-ID in succession.

6. Clearing the Post-Recording Mode
The [start-ID] or [stop] key is pressed. [Start-ID] turns on.
Even if the [skip-ID] is selected, the start-ID post- recording mode is cleared.

2. Skip-ID (Shortening-ID)

a. Recording

1. Initial Mode
Stop, pause or play.
2. Skip-ID Selection
→ The [skip-ID] key is pressed.
→ [Skip-ID] flashes rapidly.
Lights when the skip-ID is present and flashes when it is not.
3. Recording Position Setting
Set with the [shuttle] switch.
• 1-2 are not shown in any particular order.
4. Recording Start Command
The [write] key is pressed.
→ [Skip-ID] turns on during recording.
If the skip-ID has been recorded beforehand, the tape is rewound to a position before the skip-ID and the skip-ID is erased. Then, the skip-ID is recorded for 1 second from the tape position where the [write] key was pressed.
5. Stop Mode
Pause or play.
The pause mode is entered even if the initial mode is stop.
• Steps 3 - 4 are repeated to post-record the skip-ID in succession.
6. Clearing the Post-Recording Mode
The [skip-ID] or [stop] key is pressed.
→ [Skip-ID] turns on.
Even if the [skip-ID] is selected, the skip-ID post- recording mode is cleared.

b. Erase
The D. 1. b. [skip-ID] key is pressed. Then, steps 3-4 are performed using the same procedure to erase the start-ID.

3. End (end mark, PNO-ID=0EE)

a. Recording: Independent recording is also the same when recording stops.
1. Recording Position Setting
It is recommended that recording be continued after auto rec mute when recording stops.
2. Initial Mode
Rec pause
3. End Selection
The [end] key is pressed.
→ The [end] indicator flashes.
4. Recording Start Command
The [play] key is pressed.
→ The [end] indicator turns on and PNO shows "EE".
<1> End (PNO-ID=0EE) is recorded for approximately 9 seconds.
<2> If music signals have been recorded, they are erased during recording.

5. Stop Mode
After the recording stops, the tape is rewound to the recording start position and the stop mode is entered.
6. Clearing the Recording Mode
Automatically cleared after end is recorded.
→ [End] turns on (indicating the end).

b. Erase
1. Erase Position Setting
The [end search] key is pressed.
→ The [pause] LED flashes.
When the position of the recorded end is reached during tape travel, the FL indicator turns on and the stop mode is entered.
2. Initial Mode
Rec pause ([rec] key is pressed).
3. Erase Start Command
The [play] key is pressed.
By performing normal recording, end is automatically erased and recording can be continued.
However, recording must be continued for at least 9 seconds.
4. Stop Command
The [stop] key is pressed.

4. Renumber

1. Initial Mode
Stop or pause.
2. Operation Start Command
The [renumber] key is pressed.
<1> The tape is rewound to its beginning.
<2> The start-ID is searched for and the PNO (program number) is written in sequence from 1.
3. Renumber Operation
a. Auto PNO Mode
The start-ID is searched for and moved to a position which exceeds -60 dB and the PNO is written.
Note:
If recorded in the auto PNO mode, the start-ID is written when -42 dB is exceeded. If the S/N ratio is excellent during renumbering, the start-ID is moved so that a more accurate program search is possible.
b. Manual PNO Mode
The PNO is written sequentially to the position of the start-ID.
If the previously recorded PNO is correct, it is skipped.
4. Stop Mode
When the end of the tape or end is reached, the renumber operation stops and the tape is rewound to its beginning (auto rewind function).

5. Retime
0. For a tape which has not been recorded with the absolute time (A-time), the tape is rewound to its beginning, the [rec] key is pressed and recording is forcibly performed from the beginning.
1. S-ID Selection
The [start-ID] key is pressed.
→ [Start-ID] flashes.

2. Auto Recording Mode Selection
The [auto PNO/start-ID] key is pressed. [auto PNO] turns on.
→ The auto PNO mode is selected at power on.
● 1-2 are not shown in any particular order.
3. The [rew] key is pressed.
The tape is rewound to its beginning (when retiming from the beginning of the tape) and the A-time until the current tape position is determined. To retime the succeeding portion, the rew operation is unnecessary.
4. Record Start Command
The [write] key is pressed.
5. Stop Mode
When the A-time is recorded until the end of tape or to a unrecorded portion, the stop mode is entered.

Notes:
<1> When retiming, all start-IDs are rerecorded in the post-recording and in the auto recording mode, and the PNO is erased.
<2> The end (PNO-ID=0EE) is not erased even if it has been recorded.

1-3 Serial Copy Management System (SCMS)

1) Overview and Purpose of SCMS

A feature of digital recording enables repeated copying without sound degradation. Since any generation copy can become a master, it is necessary, with respect to music copyrights, to limit copying so as not to interfere with the advancement of the music industry. On the other hand, for the consumer who buys the software, it is important to permit direct digital recording for backup purposes.

The serial copy management system allows copying only for one generation from CD or DAT and prevents serial copying (copying in turn from a copy). The digital source to be recorded is identified as copyrighted or non-copyrighted material. If it is copyrighted, copying is limited to one generation. If it is not copyrighted, copying for unlimited generations is permitted.

2) SCMS

1. The copy inhibit flag (1 bit) provided in the digital audio inter-face and the category code (8 bits) which identifies the type of the digital source are used. The DAT inputs the digital source and identifies it as one that is copy inhibited, one that can be copied until a certain generation, or one that can be copied freely.

2. A code which identifies the tape as one that is copy inhibited, one that can be copied for one generation, or one that can be copied freely, is recorded in the digital copy ID (2 bits) provided on the DAT tape. During play, this information is output to the digital audio interface.

3) Functions of the SCMS

1. Digital source with copy inhibit flag:
   Copying is permitted for one generation only.
2. Digital source without copy inhibit flag:
   No limit on copying.
3. Analog input:
   Digital copying is permitted for two generations from a copy.
4. A/D converter general category (regardless of copy inhibit flag):
   Digital copying is permitted for two generations from a copy.

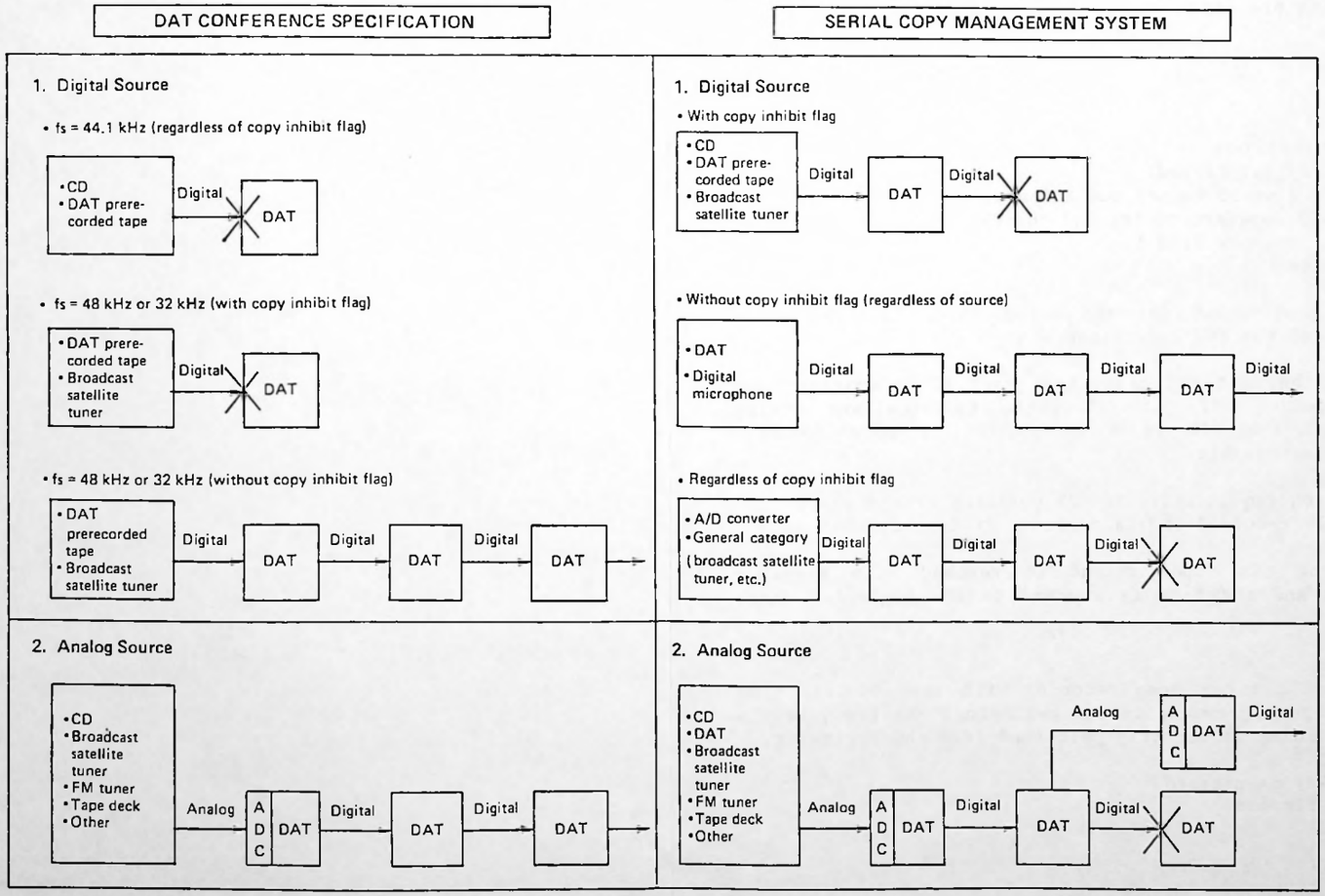


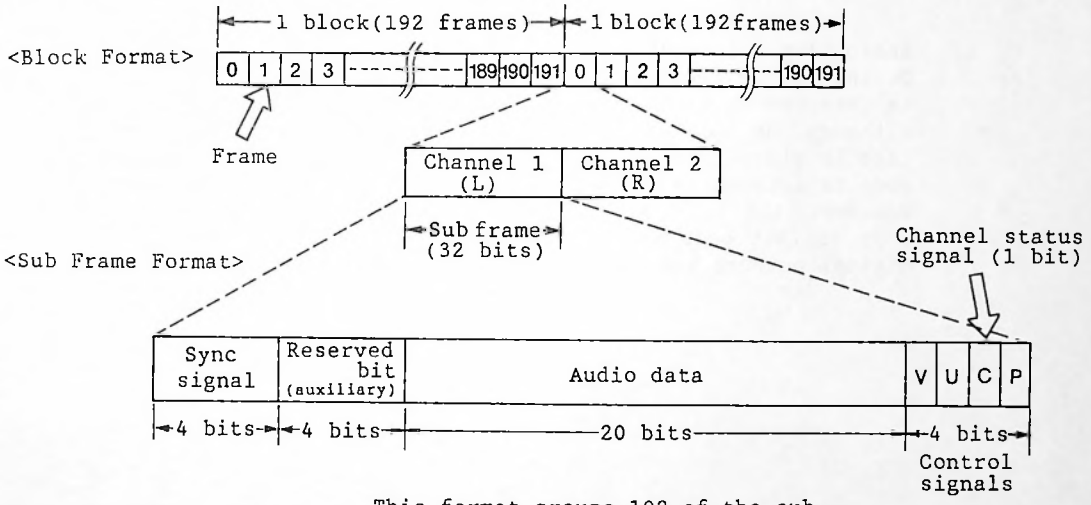
Table 1—1

4) Description of SCMS

1. The DAT copy inhibit code "ID6" is located in the main ID and defined as shown below.

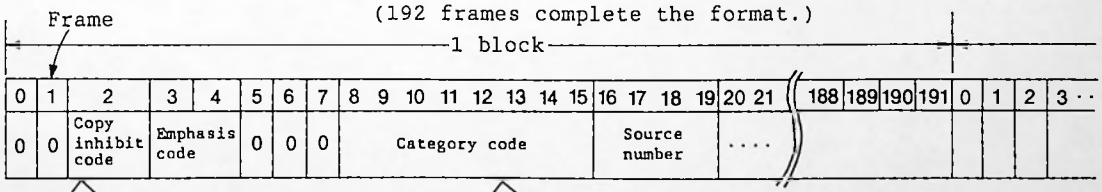
ID6	Conventional DAT	SCMS-DAT
00	Copy enabled	Copy enabled
10	Copy inhibited	Copy inhibited
11	Undefined	Copy enabled once only
01	Undefined	Undefined

2. The copy inhibit flag (1 bit) and category code (8 bits) which indicate the type of machine are determined at the digital audio interface.



<Channel Status Format>

This format groups 192 of the sub frame's 1-bit channel statuses. (192 frames complete the format.)



	Code
Copy inhibit	0
Copy enabled	1

Category Name	Code
General	0 0 0 0 0 0 0 0
CD	1 0 0 0 0 0 0 0
PCM processor	0 1 0 0 0 0 0 0
BS tuner	0 0 1 0 0 0 0 0
DAT	1 1 0 0 0 0 0 0
DAT-P	1 1 0 0 0 0 0 1

3. The channel status copy inhibit flag and category code, and the DAT copy inhibit code are used to control the SCMS. The relationship of the codes is shown below.

Copy Inhibit Code (ID6) on the DAT Tape	Digital Output		Copy Inhibit Code (ID6) after Digital Copy
	Category Code	Copy Inhibit Code	
00	DAT (11000000)	1 (Copy enabled)	00
10	DAT (11000000)	0 (Copy inhibited)	Copy disabled
11	DAT-P (11000001)	0 (Copy inhibited)	10

Table 1–2

4. Analog Input Recording
During analog recording, an ID6 of "11" (copy enabled once only) is recorded onto the tape.
Although the copy inhibit code is "0" (copy inhibited) when this tape is played, the category code is "DAT-P" and the copy inhibit code is ignored to allow digital copying.
However, ID6 is "10" (copy inhibited) on the copied tape, the copy inhibit code is "0" and the category code is "DAT" for the digital output, and subsequent digital copying is not allowed.

2. Audio Circuit

2-1 Block Diagram of the Recording Circuit

2-2 Recording Signal Flow and Circuit Operation

2-3 Block Diagram of the Play Circuit

2-4 Play Signal Flow and Circuit Operation

2-5 Voltage Supply Lines to DAC and ADC

2-1 Block Diagram of the Recording Circuit

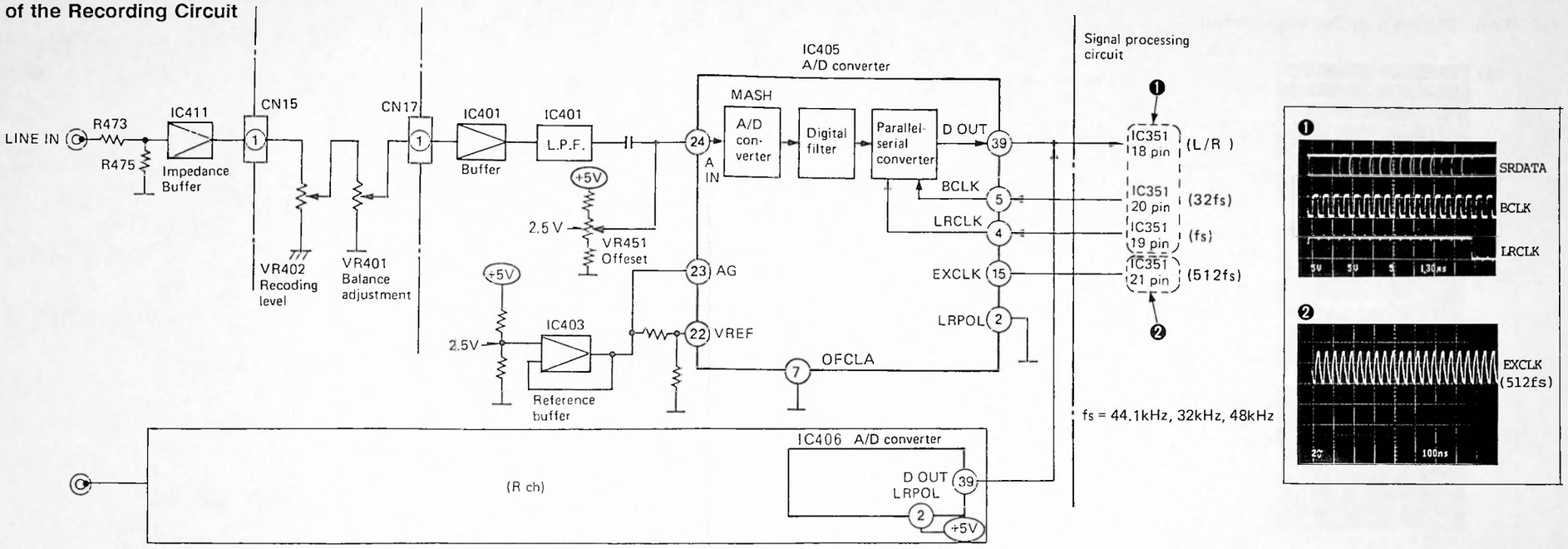


Fig. 2–1

2-2 Recording Signal Flow and Circuit Operation

The audio signal (analog signal) that is input by LINE IN is converted to a digital signal by the A/D converter IC. Data for the left and right channels is output as serial data and supplied to the signal processing circuit.

1) The audio signal that is input by LINE IN is attenuated approximately 6 dB by resistors R473 and R475 and amplified approximately 6 dB by buffer amplifier IC411 in the next stage. After the signal level is stabilized, the signal is fed to the volume circuit.

2) The signal that is input passes the recording level adjustment control VR402 and balance adjustment control VR401, and is sent to the circuit in the next stage. The balance adjustment control has a variable range of about 6 dB.

3) The signal from the volume circuit is amplified approximately 5 dB at the buffer amplifier in IC401, its unwanted noise components of 22 kHz and above are eliminated, and the signal is fed to pin 24 of the A/D converter IC.

4) The analog signal is converted to a digital signal at the MASH A/D converter circuit in IC405.

5) The MASH output is a 4-bit, 64fs digital signal which is converted to 16-bit, fs normal digital audio data at a subsequent digital filter.

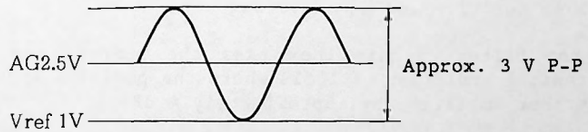
6) Then it is converted to a serial signal at the parallel/serial converter circuit and synchronized to the BCLK signal (32fs) at pin 5 and the LRCLK signal (fs) at pin 4 which are input from the signal processing circuit, and output as the DOUT signal from pin 39.

7) The timing of the output from pin 39 is controlled by the LRCLK signal which is input at pin 4. When low the DOUT signal for the left channel (IC405) is output and when high the DOUT signal for the right channel (IC406) is output. They comprise the left/right serial data sent to the signal processing circuit.
Pin 2 (LRPOL) of the D/A converter is the output select terminal. If set to low, the output is issued at the low of LRCLK.

8) IC403, supplied with 2.5 V at pin 23, sets the ground level of the analog signal which is input by AIN of IC405.

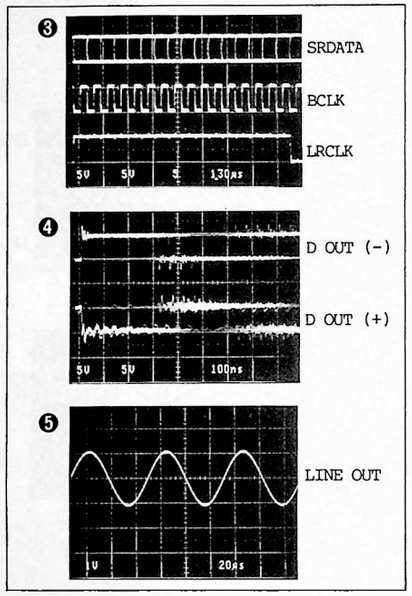
9) The input to AIN uses the 2.5 V as a center level (ground) since the power supply for IC405 is a single 5 V supply.

10) A 2.5 V signal is divided by resistors to a signal of approximately 1 V which is supplied to pin 22 of IC405. The difference between this voltage and the 2.5 V of the AG level determines the full-scale level.



11) Adjust the offset adjustment control VR451 while the level meter is deflecting regardless of whether the signal input is absent.
The unit is equipped with the automatic calibration function. If the offset is about -40 dB, it is automatically drawn to -∞.
(The automatic calibration function can be disabled by supplying a +5 V signal to OFCLR at pin 7 of IC405.)

2-3 Block Diagram of the Play Circuit



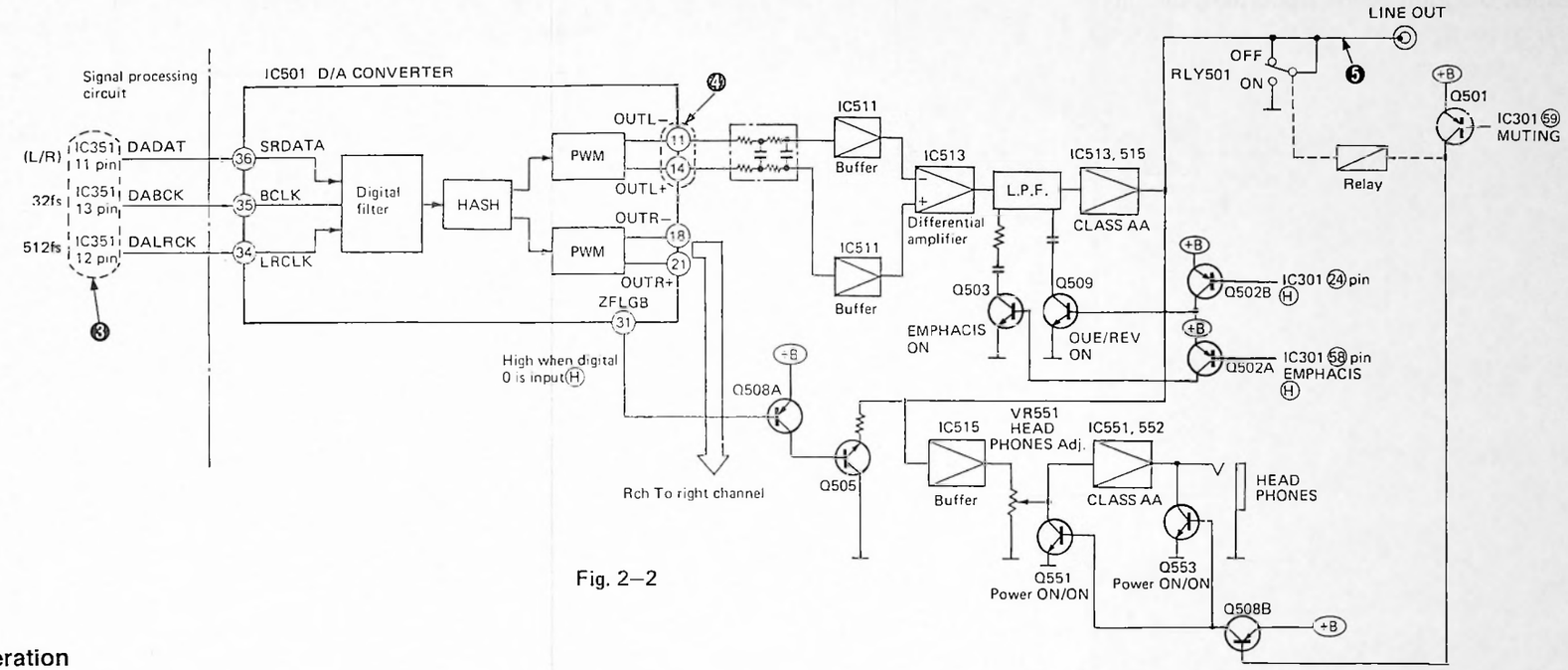


Fig. 2–2

2-4 Play Signal Flow and Circuit Operation

The DADAT signal (digital signal) which is sent from the signal processing circuit is converted to an analog signal by the D/A converter IC and output from LINE OUT and HEAD PHONES.
The circuit has practically the same configuration as the one in the SL-P777 CD player.

1) The DADAT, DABCK and DALRCK signals which are sent from the signal processing circuit are fed to pins 36, 35 and 34 of IC501.

2) For the signals which are fed to IC501, the 16-bit serial data is subjected to 4-times oversampling by the digital filter circuit and output as 18-bit data.

3) The output data is converted to 32-times oversampling, 8-value data by the MASH circuit (noise shaping system).

4) Further, it is converted to 1-bit pulse signals and output from pins 14 and 11 as positive and negative signals.

5) From the filter circuit they pass the buffers and are fed to the differential amplifier of IC513 where the positive and negative signals are further amplified by approximately 4 dB.

6) The signal has its high frequency components of 22 kHz and above eliminated at the low-pass filter in the class AA amplifier circuit consisting of a resistor, capacitors, IC513 and IC515, and is output from LINE OUT.

7) The output signal from LINE OUT passes the class AA amplifier consisting of buffer IC515, variable resistor VR551 for headphone level adjustment, IC551 and IC552, and is output from HEAD PHONES.

8) Q503 comprises a circuit used to switch to a deemphasis characteristic when a tape which has been recorded with an emphasis characteristic is played. The switching command is sent by pin 58 (NDEMP) of IC301 in the system control circuit which turns on Q502A and then Q503.

9) Q509 comprises a circuit which eliminates the high frequency components (800 Hz and above) when performing cue or rev using the shuttle dial. If the speed is x5 or more when using the shuttle dial, the switching command from pin 24 of IC301 in the system control circuit is sent as an ATT signal which turns on Q502B and then Q509 to activate muting.

10) Q505 improves the S/N ratio when a 0-level digital signal is input. The ZFLGB signal from pin 31 of D/A converter IC501 goes low which turns on Q502 and then Q505 to activate muting.

11) Q551 and Q553 perform signal muting for the headphone.
Q551 and Q553 operate on the SGMTG (signal muting) signal from IC301 and function like the relay for LINE OUT. The switching noise that results when the power is turned on is prevented by utilizing the charging characteristic of C507 and C508, which are connected to the bases of Q511 and Q512, to slow down the rise of the headphone amplifier power supply.

12) RLY501 is for LINE OUT muting. Q551 and Q553 are for HEAD PHONE output muting. This circuit activates muting when play or rec play is activated or during rec pause.
The SGMTG signal at pin 59 of IC301 goes low and Q501 turns on to drive the relay circuit. This turns on RLY501 and LINE OUT muting is activated (during rec play and play).
On the other hand, when Q501 and then Q508 turn on, this turns on Q551 and Q553 to activate headphone muting.

2-5 Voltage Supply Lines to DAC and ADC

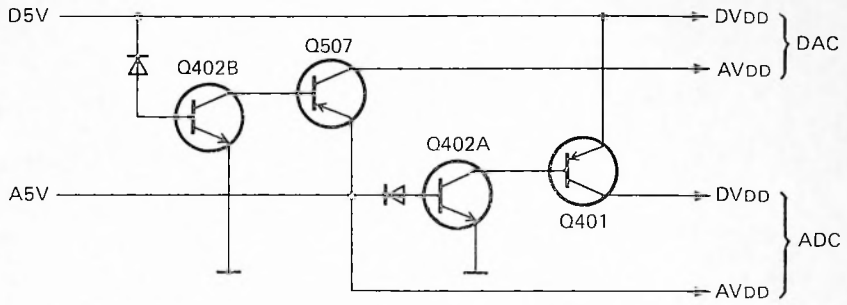


Fig.2–3

The power supply timing to DAC and ADC is such that the activation of the analog power supply and the digital power supply is slightly different for the DAC and for the ADC.
An incorrect activation sequence may damage the ICs.
For ADC, AVDD is activated and then DVDD.
For DAC, DVDD is activated and then AVDD.
For ADC, A5V turns on Q402A which turns on Q401 to output DVDD.
For DAC, D5V turns on Q402B which turns on Q507 to output AVDD.

(2. Audio Circuit for SV-3700)

2-1 Block Diagram of the Recording Circuit

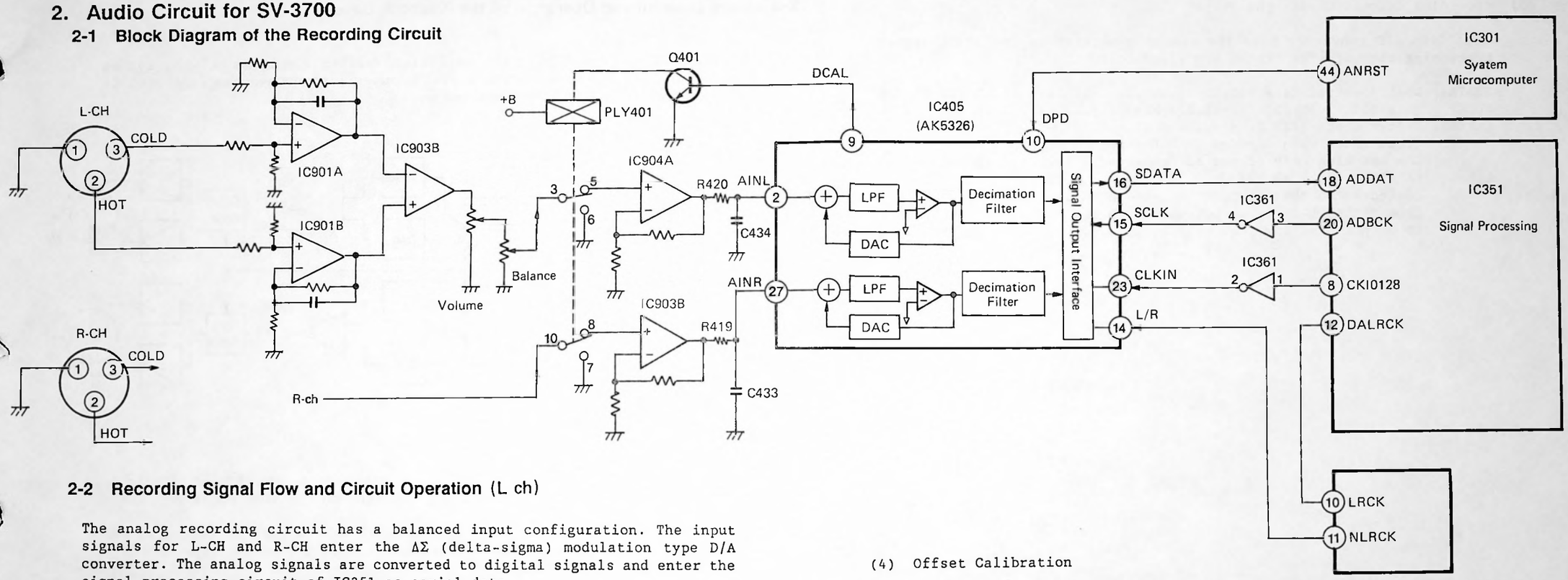
2-2 Recording Signal Flow and Circuit Operation (L ch)

2-3 Block Diagram and Operation of the Playback Circuit

2-4 Playback Circuit Opeartion

2. Audio Circuit for SV-3700

2-1 Block Diagram of the Recording Circuit



2-2 Recording Signal Flow and Circuit Operation (L ch)

The analog recording circuit has a balanced input configuration. The input signals for L-CH and R-CH enter the ΔΣ (delta-sigma) modulation type D/A converter. The analog signals are converted to digital signals and enter the signal processing circuit of IC351 as serial data.

(1) The audio signal which is input through LINE IN is added to the impedance transformer amplifier of IC901A and IC901B and amplified by +6 dB. IC903B is a balanced amplifier and comprises a differential amplifier circuit. In the same way, the signal is amplified here by +6 dB.

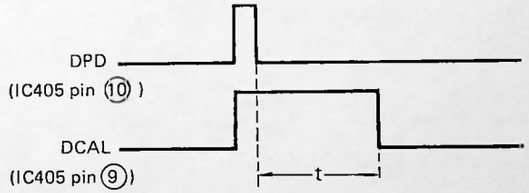
(2) The signal from IC903B passes the volume and balance controls, and enters the IC904A buffer amplifier and then the IC405 A/D converter. R420 and C434 comprise a low-pass filter which cuts off high frequency noise.

(3) Operation of IC405 (AK5326)

IC405 is an A/D converter which employs ΔΣ (delta-sigma) modulation. The input signals for L-CH and R-CH are simultaneously oversampled at 64fs and converted from analog to digital. The outputs of the ΔΣ demodulator circuits for L-CH and R-CH are in the form of 4-bit 64fs. The converted data is then converted to the usual 16-bit fs digital audio format and sent as serial data to the signal processing circuit.

(4) Offset Calibration

If the digital audio has an initial offset, a click sound can be heard when the power is turned on. For this reason, it is necessary to cancel the offset when turning on the power. Pins 9 and 10 of IC405, Q401 and relay RLY401 comprise a circuit for this purpose.



t: Calibration period (approx. 80 ms)

When the power is turned on, ANRST at pin 44 of IC301 goes momentarily high. When pin 10 of IC405 receives this signal, DCAL at pin 9 goes high, Q401 turns on and RLY401 is actuated. At this time, the input signal is switched off. Only the DC component appears at the input of IC405 and the offset error is canceled. (The input range is ±3.6 V.)

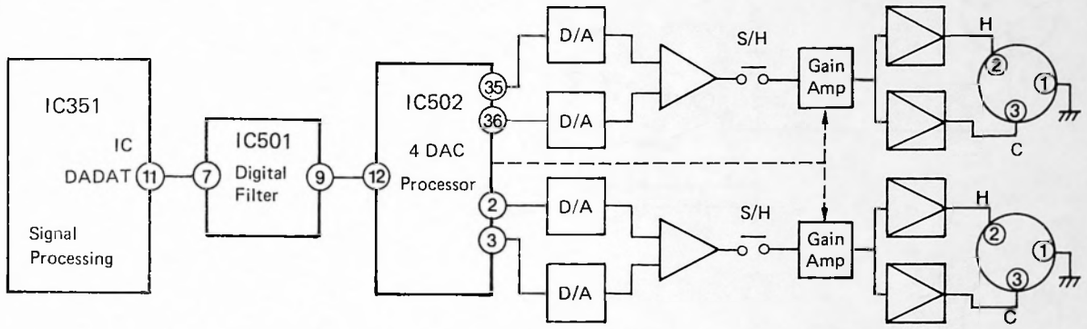
(5) Recording Circuit Clocks and Output

The IC405 A/D converter uses the clocks generated by the IC351 signal processing circuit. The clocks are given below.

SDATA: 16-bit serial data output ..... IC405 Pin (16)
SCLK: Data bit clock (32 fs = 1.536 MHz) ..... IC405 Pin (15)
CLKIN: Master clock (128 fs = 6.144 MHz)
(This clock when divided by 2 becomes
the sampling rate of the ΔΣ converter.) ..... IC405 Pin (23)
L/R: LR clock (fs = 48 kHz)
(Selects the channel for the data which is output
from SDATA. L-CH is output when high and R-CH
is output when low.) ..... IC405 Pin (14)

2-3 Block Diagram and Operation of the Playback Circuit

The D/A converter and playback amplifier section comprises a 4DAC system which uses four D/A converters. Operation uses 4 times oversampling with 18 bits. The block diagram is shown below.



(1) The digital data signal which is input from pin (11) of IC351 is subjected to 4 times oversampling and sent to the 4DAC processor.

(2) At the 4DAC processor, the input digital data signal is separated and distributed to four D/A converters according to the type of data signal.

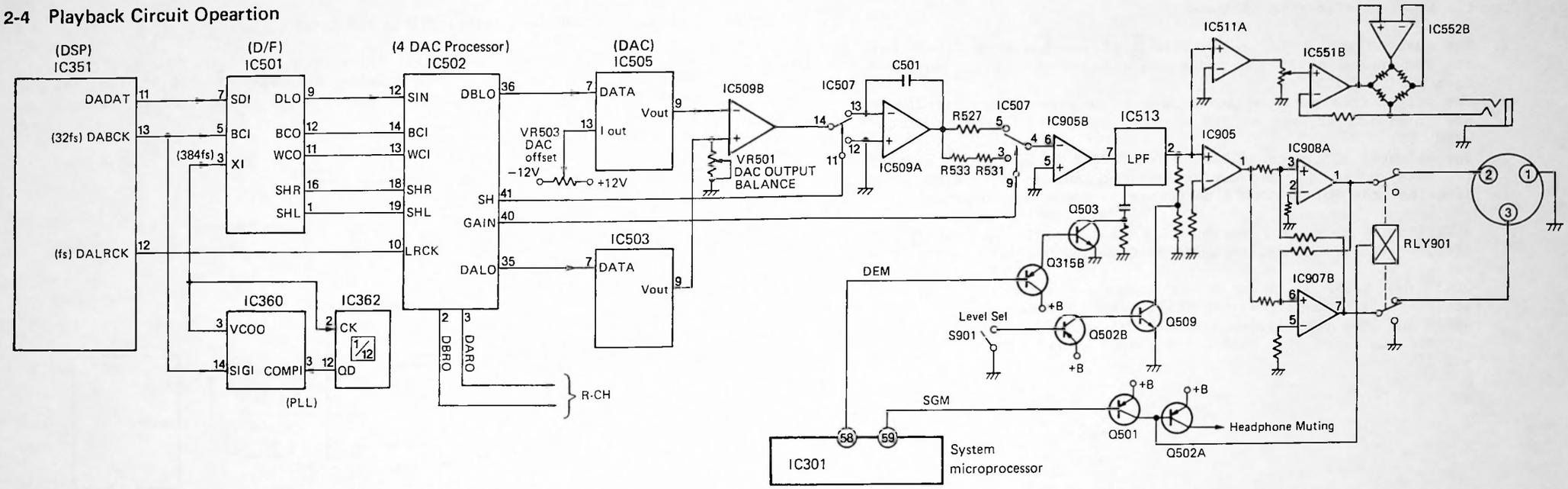
(3) At the D/A converters, the PAM signal is generated. The PAM signals are combined amplified by differential amplifier.

(4) The combined signal is sent to the sampling hold circuit to recover the recorded music signal.

(5) During operation of the 4DAC processor, the level switching amplifier output the equivalent of 18 bits data when digital data with a recording level below -12 dB is input. The level switching amplifier is provided to decrease the gain when the gain of the D/A converter increases 4 times.

(6) The music signal from the level switching amplifier is input to the low-pass filter where the components outside the audio frequency range are removed. The music signal is then sent to the amplifier in the next stage, and is output from LINE OUT.

2-4 Playback Circuit Opeartion



1) From the Digital Filter to the 4DAC Processor

(1) The digital playback data signal from pin (11) of IC351 is input by pin (7) of digital filter IC-501. It is input in sequence for the left channel and right channel with a period of each sampling frequency. Based on processing operations within IC-501, it is output from pin (9) of IC-501 with the 4 times oversampling period of 192 kHz.

(2) The playback data signal from pin (9) of IC-501 is input by pin (12) of 4DAC processor IC-502. At IC-502, the operation changes according to the input level. The operation of IC-502 is described next.

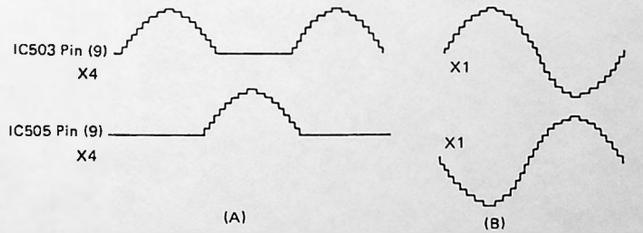
(a) When the input is a playback data signal which is lower than -12 dB with respect to the full-scale level:
The data is determined to be either positive or negative. If positive, it is output to pin (35) and sent to D/A converter IC-503. If negative, it is phase inverted, output to pin (36) and sent to D/A converter IC-505.

(b) When the input is playback data signal which is higher than -12 dB with respect to the full-scale level:
The data is output simultaneously to both pins (35) and (36), regardless of whether the data code is positive or negative. At this time, the phase at pin (36) is inverted.

2) From the D/A Converter to the Level Switching Amplifier

(1) The playback data signals which are input by pin (7) of IC-503 and pin (7) of IC-505 are D/A converted and output to pin (9) of IC-503 and pin (9) of IC-505 as PAM signals. The output PAM signals are input to pin (2) and (3) of IC-511 (A) where they are combined and then sent to the sampling hold circuit.

(2) The circuit consist of IC-507, IC501, IC-509A is sampling hold circuit. The output signal is sent to level switching amplifier IC905B in the next stage. Figure below (A) shows the PAM signals when the input playback data signals are lower than -12 dB with respect to the full-scale level, and figure below (B) shows the PAM signals when the input playback data signals are higher than -12 dB with respect to the full-scale level.



(3) Level switching amplifier IC905B is controlled by 4DAC processor IC-502. When the 4DAC processor is activated by an input signal which is lower than -12 dB with respect to the full-scale level, pin (9) of IC-507 goes high and the gain of amplifier IC905B becomes -12 dB. Further, when it is activated by an input signal which is higher than -12 dB with respect to the full-scale level, pin (9) of IC-507 goes high and the gain of the amplifier becomes -6 dB.

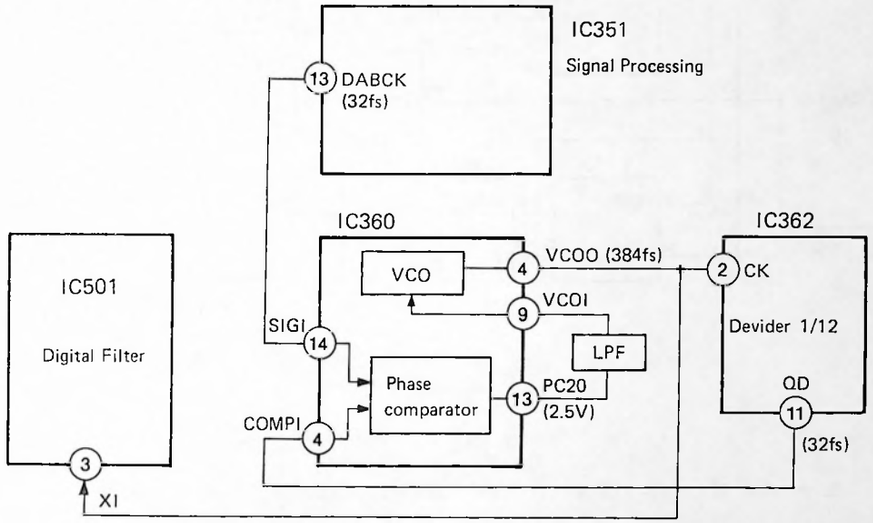
3) From the Low-Pass Filter to LINE OUT

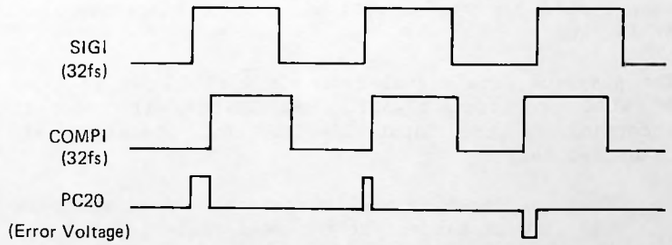
(1) The music signal which enters pin ⑦ of the low-pass filter has its components of 22 kHz and above eliminated, and is supplied from pin ② to IC905.
The output from pin ① of IC905 is used to produce positive phase and inversion signals at IC908A and IC907B which are output to LINE OUT.
The balanced amplifier of IC908A and IC907B is configured so that the same output as that during balanced output is obtained even if either the HOT or COLD side output is connected to ground.

(2) RLY901 is a relay for muting. The command from pin ⑤⑨ of the IC301 system microcomputer turns on Q501 and Q502A to actuate the relay.
Q503 and Q315B comprise a de-emphasis circuit. It is also activated by command from the IC301 system microcomputer.
Q502B and Q509 comprise an output level switching circuit. The on and off states of S901 switch the output to two levels (+4 dB and -10 dB).

4) PLL Circuit for the Digital Filter and Clock

The master clock for the digital filter requires 384fs. Since a clock at this frequency is not available anywhere, a PLL circuit is configured from IC360 and IC362 to generate the clocks corresponding to the 3 sampling frequencies.





IC360 contains a VCO and phase comparator. IC362 is a 1/12 divider. ADBCK at pin 13 of IC351 outputs 32fs. With this signal as a reference, the phase of the oscillating signal of the VCO after 1/12 division (approx. 32fs) is compared and its phase error voltage controls the VCO to form the PLL circuit.

3. RF Circuit and Play PLL Circuit

3-1 Block Diagram of the RF Circuit

3-2 RF Circuit Operation

1) Circuit Operation and Signal Flow During Play

2) Circuit Operation and Signal Flow During Record

3-3 Irec SELECT Block Operation

3-4 Block Diagram of the Play PLL Circuit

3-5 Play PLL Circuit Operation

1) Play PLL Circuit Operation and Signal Flow

2) Envelope Detection Circuit

3) ATF Filter Operation

3-6 Operating Principles of the PLL Circuit

3-7 PLL Circuit Timing Chart

3. RF Circuit and Play PLL Circuit

3-1 Block Diagram of the RF Circuit

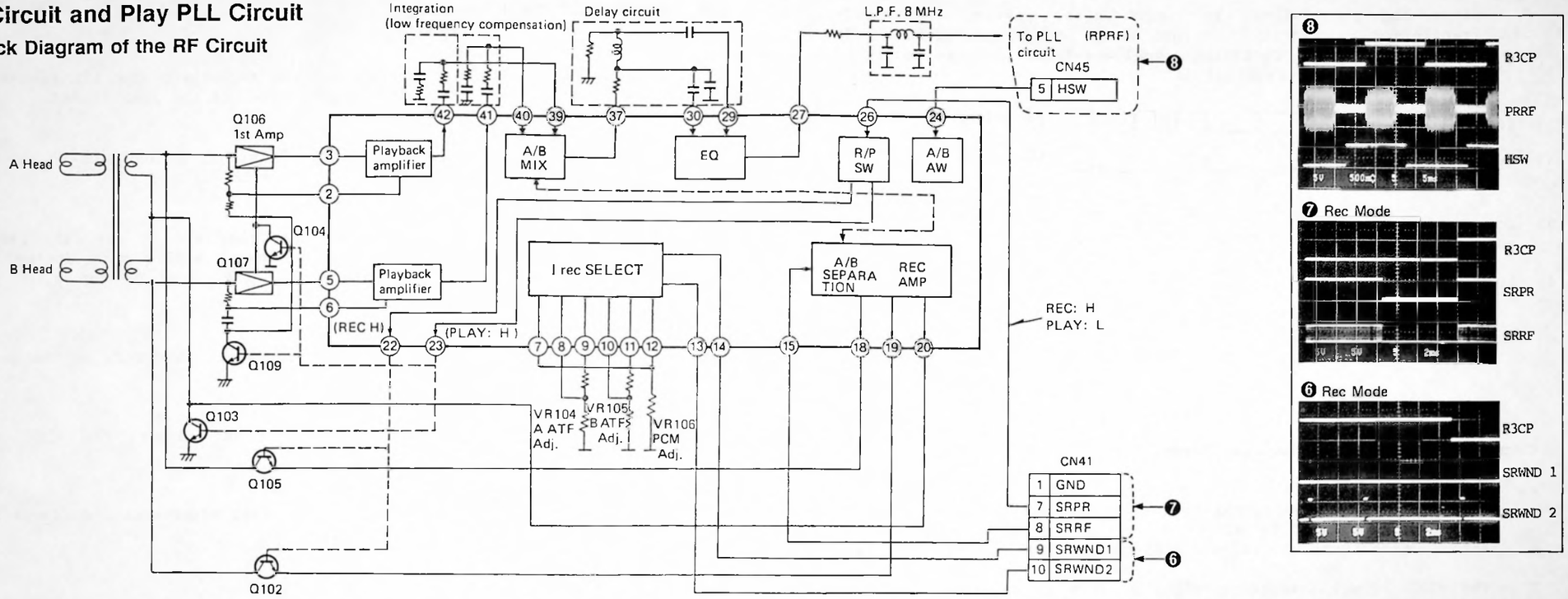


Fig. 3–1

3-2 RF Circuit Operation

During play, the RF circuit reads the data recorded on the tape, performs waveshaping, and sends the play signal to the PLL circuit. During record, the RF circuit supplies the recording signal produced by the signal processing circuit and records it onto the tape.

1) Circuit Operation and Signal Flow During Play

1 During play, the SRPR signal (recording/play switching) supplied from the signal processing circuit goes low. When it is input by pin (26) of IC101, pin (23) goes high which turns on Q103, Q104 and Q109 to select the play mode.

2 The play signal from the head rotary transformer is amplified approximately 30 dB by the 1st amplifier Q106 and input by pin (3) of IC101.

3 The signal is amplified approximately 40 dB by the play amplifier in IC101 and output to pin (42).

4 The signal output from pin (42) is low-frequency compensated by the integration circuit consisting of R104, R102, C104 and C102, and is input by pin (39).

5 The signal input by pin (39) is combined at the A/B MIXING block into a serial signal by combining the A head signal and B head signal according to the HSW (head switching) signal which is supplied from the servo circuit. The HSW signal performs switching to the left channel when high and to the right channel when low.

6 The combined serial signal is amplified approximately 20 dB and output from pin (37).

7 The signal output from pin (37) passes the delay circuit consisting of R117, R118, C105, C106, C107 and L101, is input by pins (29) and (30), and is waveform equalized at the EQ circuit.

8 After being waveform equalized, the signal is output from pin (27), its unwanted frequency components of 8 MHz and above are eliminated by the low-pass filter consisting of R151, C171, C172 and L104. The signal is input by the play PLL circuit IC102. (Low-frequency compensation at the integration circuit)

9 Since the play signal is output after passing the rotary transformer, a signal like that shown in (2) is output. To obtain the original recording signal waveform, it is necessary to pass the integration circuit.

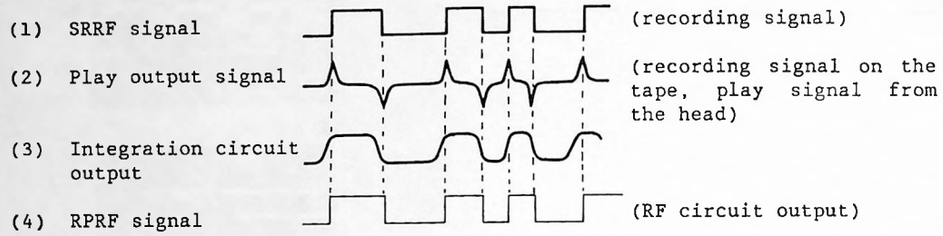


Fig. 3–2

2) Circuit Operation and Signal Flow During Record

1 During record, the SRPR (recording/play switching) signal which is supplied from the signal processing circuit goes high. When the signal is input by pin (26) of IC101, pin (22) outputs a high signal which turns on Q102 and Q105 to select the recording mode.

2 The SRRF signal (recording signal) which is supplied from the signal processing circuit is input by pin (15) of IC101.

3 The SRRF signal which is input by the A/B SEPARATION block in IC101 is separated into the A head and B head recording signals according to the HSW signal and input by the REC AMP block.

4 The REC AMP block amplifies the signals and applies them to the A channel and B channel heads with the BTL drive.

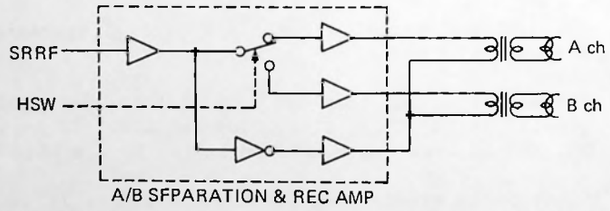


Fig.3–3

3-3 Irec SELECT Block Operation

1) This circuit comprises the block used to adjust the ATF recording signal level and PCM recording signal level of the SRRF signal.

2) The ATF signal consists of the pilot ATF signal in addition to the ATF signal. A recording current is set for each signal.

3) If these two signals are recorded onto the tape at the same level, there is the danger that the low frequency will remain during the overwrite operation. For this reason, the level of the pilot ATF signal is set low.

4) If this adjustment shifts, compatibility with other DATs may become a problem.

5) VR106 is used for PCM level adjustment and adjusts the PCM level component of the recording signal.

6) VR104 and VR105 are used for pilot ATF level adjustment and adjust the level of the pilot signal (130 kHz).

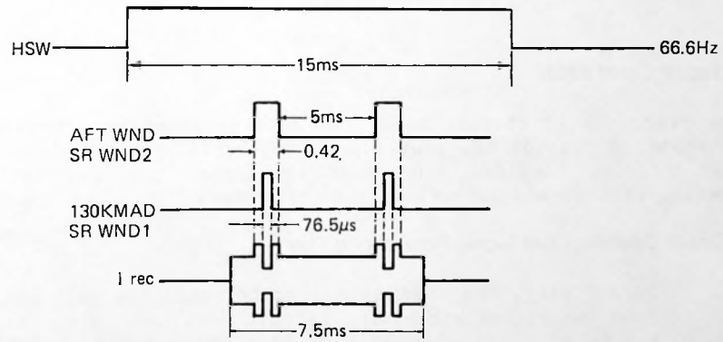


Fig. 3–4

° SRWND2 (ATFWND) is a window which goes high only during the ATF signal period. SRWND1 (130KWND) is a window which goes high only during the pilot ATF signal period.

3-4 Block Diagram of the Play PLL Circuit

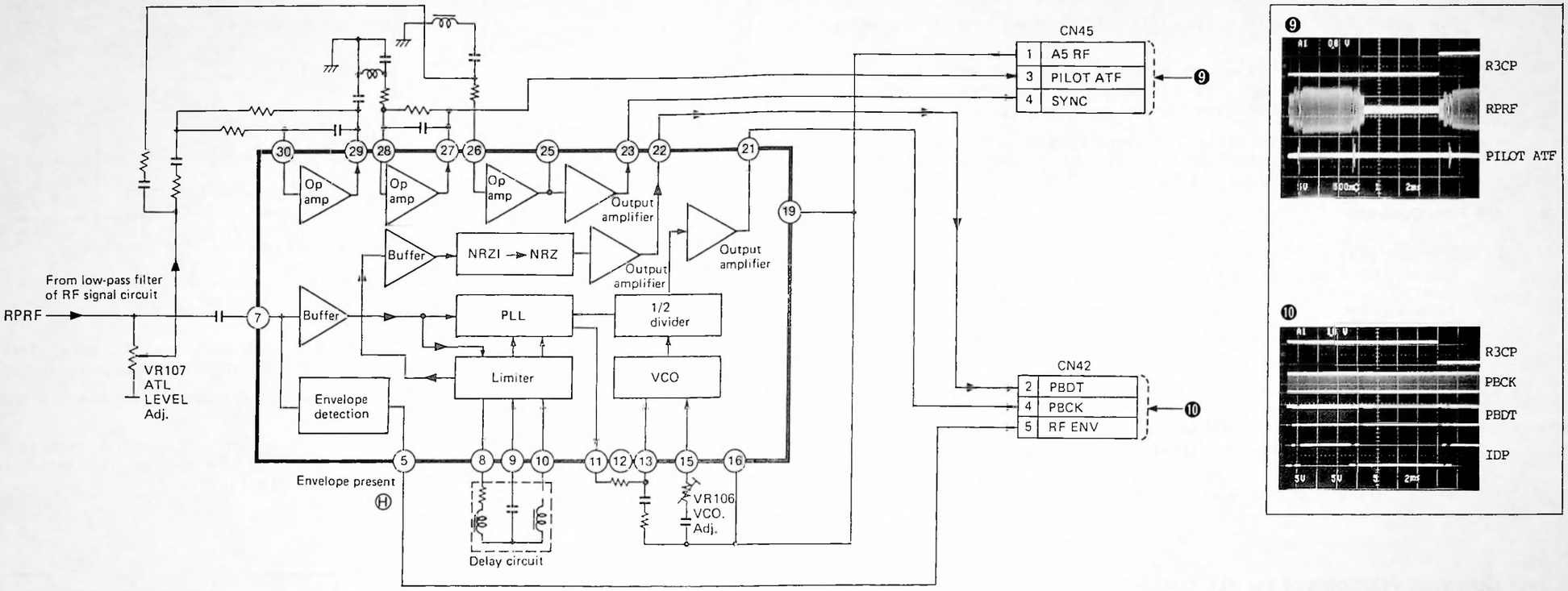


Fig. 3–5

3-5 Play PLL Circuit Operation

The play PLL circuit extracts the digital data and the clock which is synchronized to that data from the RPRF signal (play signal) which was waveform equalized at the RF circuit in the previous stage.

1) Play PLL Circuit Operation and Signal Flow

1 The RPRF signal which was waveform equalized at the RF circuit is input by pin ⑦ of IC102.

2 It passes the buffer in the IC and is output to pin ⑧.

3 The signal output to pin ⑧ passes the delay circuit consisting of L109, C177, L110 and C178, and is input by pin ⑨ with a 25 nsec delay and by pin 10 with a 50 nsec delay.

4 Then the signal at pin ⑧ and the signal at pin ⑩ are compared in the IC.

5 Further, the signal is compared with fosc/2 = 9.408 MHz which is the oscillation frequency fosc = 18.816 MHz of the VCO divided by 2, and the comparison error is output to pin ⑪ as the PD signal (phase comparison signal).

6 The PD signal has its high frequency components eliminated by the low-pass filter consisting of C179, R178 and C181, and the signal is input by pin ⑬. Supplying the signal to the VCO completes the PLL circuit.

7 After the main play signal is input from pin ⑦, it is input by the PLL circuit.

8 At the PLL circuit, the data is extracted using the clock which is synchronized to the input data and is converted to a complete digital signal .

9 Next, after the signal is demodulated at the digital converter circuit from the NRZI signal to the NRZ signal, it passes the output amplifier and is output to pin ㉒ as the DEMCON signal which is sent to the signal processing circuit.

10 A 9.408 MHz play clock is output to pin ㉑ of IC102 as the PLLCP2 and is also sent to the signal processing circuit.

11 VR108 is used for the VCO free-running frequency adjustment and is adjusted so that 10 MHz is obtained in the free-running state.

2) Envelope Detection Circuit

1 The block from pin ② to pin ⑥ in IC102 comprises the envelope detection circuit.

2 A high signal is output from pin ⑤ as the RFENV signal only during the period when the envelope of the RPRF signal (play signal) which is input from the RF circuit is present.

3 The RFENV signal is used as a detection signal during the end search operation. The tape is stopped during end search at a position where the play envelope disappears.

3) ATF Filter Operation

1 The bandpass filter, consisting of the op amp between pins ㉙ and ㉚ of IC102 and the externally connected RCL circuit, extracts the 130 kHz pilot ATF signal from the play signal and outputs it from pin ㉗.

2 The signal that is output is the ATF signal which is sent as the SVRF signal to the servo circuit.

3 The SVSYNC signal is extracted from the play signal by the high-pass filter consisting of the op amp (comparator) and output amplifier from pins ㉛ and ㉓ to pin ㉖ of IC102 and the externally connected RCL circuit, and is output from pin ㉓.

4 The signal that is output is sent to the servo circuit as the SVSYNC signal (SYNC signal for ATF).

3-6 Operating Principles of the PLL Circuit

1 The data signal that was waveform equalized at the RF circuit is input by pin ⑦ of IC102 and output to pin ⑧.

2 The delay circuit consisting of the RCL connected between between pins ⑧ and ⑩ determines the amount of delay. The delayed signals are fed to pins ⑨ (25 nsec) and ⑩ (50 nsec).

3 When signals are input at pins ⑧ and ⑩, a time window A is output from the EX OR1 circuit in the IC. Since the PLL is configured using this time window, it is called a window-type PLL.

4 The oscillation frequency of the VCO is fosc ≈ 18.816 MHz. This oscillating output is input by the D-FF1 1/2 divider in the next stage.

5 EX OR2 inputs time window A and output fosc/2=9.408 MHz from pin ㉑ and outputs B. The analog switch is on only while time window A is high, and output B passes the analog switch and is output to pin 11 as the PD signal. (The PD signal changes to produce the play clock which is synchronized to the input data.)

6 Supplying the PD signal to the VCO, after its high frequency components are eliminated by the externally connected low-pass filter, completes the PLL circuit.

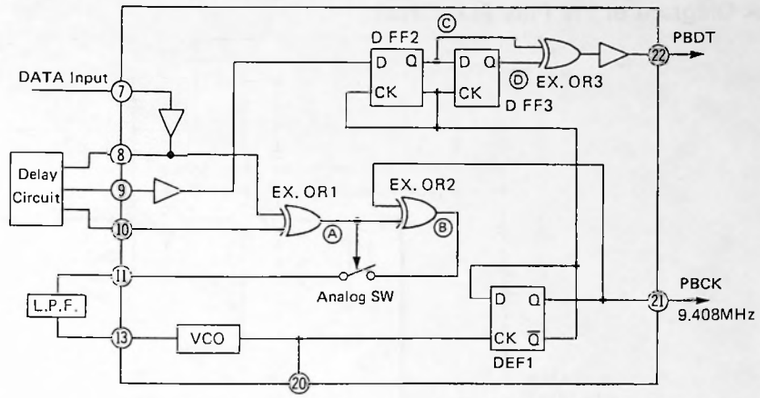


Fig. 3–6

7 As a result, the center of the channel bits in delay data 9 is extracted at the play clock PCK 21 (D-FF1 $\overline{Q}$ output of the VCO).

8 Play data C consists of the data extracted at the PLL circuit. Play data D is the Q output of D-FF3.

9 Taking the exclusive OR of play outputs C and D results in the NRZ converted output at pin ㉒. This becomes the input data to the signal processing circuit (PBDT).

3-7 PLL Circuit Timing Chart

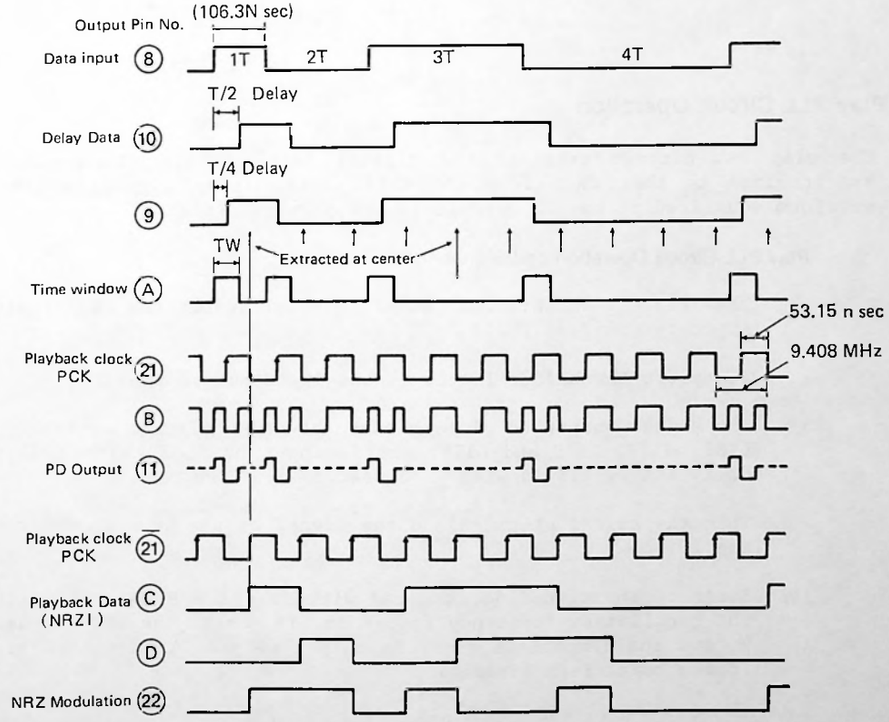


Fig. 3–7

4. Signal Processing Circuit

4-1 Overview

4-2 Main Features

4-3 Operation of the Signal Processing Block

1) Operation During Recording

2) Operation During Playback

4-4 Interface with Various Blocks

1) ADC Block

2) DAC Block

3) Digital Audio Interface Block

4) Servo Block

5) RF Block

6) Play PLL Block

7) Servo Block

8) RAM Block

9) System Control Block

10) Master Clock Oscillation Circuit Block

11) Master Clock Oscillation Circuit

12) Circuit Operation for Digital IN Recording

4. Signal Processing Circuit

4-1 Overview

The digital signal processing circuit of this unit is completely contained in a single CMOS standard cell LSI chip, the MN6624. This LSI chip contains approximately 3600 gates and has a 124-pin configuration.

The processes during recording consist of adding C1 and C2 parities and then subcodes to the PCM data from the MASH A/D converter and digital audio interface, and performing 8-10 conversion.

During play, 8-10 conversion, error correction and interpolation are performed on the play RF data. PCM data is output to the D/A converter.

Therefore, the MN6624 provides all the basic functions required for R-DAT digital signal processing on a single chip. The major functions of the MN6624 are given next.

1 Recording signal generation (8-10 conversion, synchronization signal, addition of ID, ATF signal generation)

2 C1 and C2 parity generation

3 Play signal demodulation (8-10 conversion, synchronization detection, ID parity check)

4 Error correction based on C1 and C2 parities

5 Recording and playback of subcodes

6 Address control for interleave, de-interleave and error correction

7 16-bit linear data processing

8 Interpolation and previous value hold processing

9 Peak hold detection for level meter

10 Soft mute

11 Blank detection

12 IEC standard digital audio interface I/O

13 Microcomputer interface

14 Subcode post-recording

4-2 Main Features

1 Single +5 V supply operation

2 Integration of all major R-DAT signal processing functions on a single chip

3 Pack item search

4 Compatible with fs=48 kHz, 44.1 kHz and 32 kHz

5 Built-in digital audio interface I/O function

6 3 dB step digital attenuation (up/down)

7 Cue and review compatible

8 MASH A/D and D/A compatible

9 Serial copy management system compatible (SCMS)

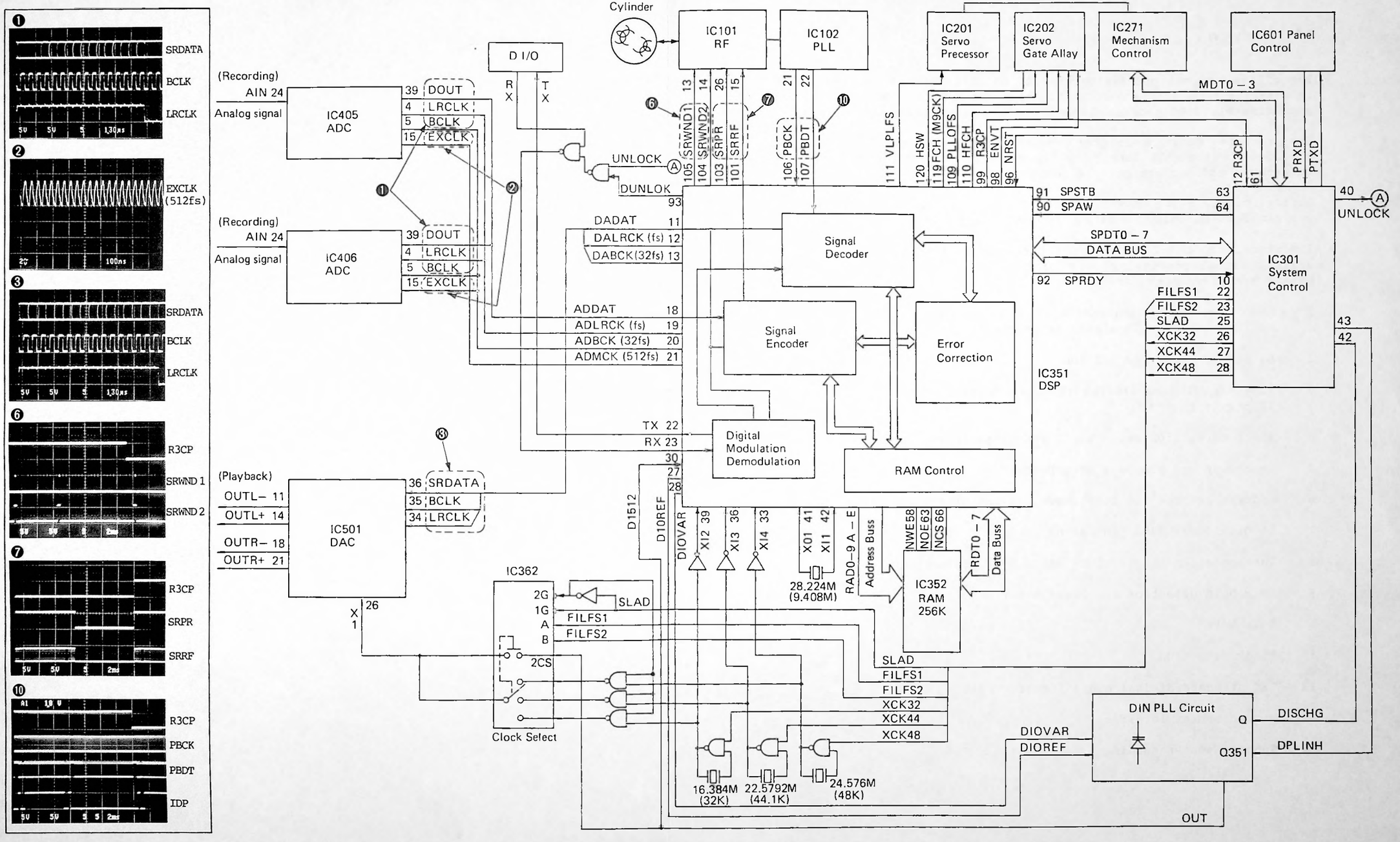


Fig. 4–1 Signal Processing Block

4-3 Operation of the Signal Processing Block

Fig. 4-1 shows the signal processing circuit and indicates the input and output signals for IC351 DSP. In addition to the single DSP IC, the signal processing circuit consists of a 256 K SRAM, 4 crystals for the master clock oscillation, and a discrete DIN PLL circuit.

1) Operation During Recording

- The analog signal is converted to 16-bit serial data by the ADC and sent to the DSP (ADDAT). The input data is written to the RAM. This data is read and the C1 and C2 parities are generated for error correction within the DSP. Then, the data and parities are again written to the RAM for the interleave.

- The subcode data generates the pack, sub ID and main ID within the DSP based on information from the system microcomputer. Like the audio data, the pack data is written to the RAM and is read for error correction to generate the C1 parity. It is then written again together with the parity.

- The data items described above are read under RAM control of the DSP. Then, the signals necessary for the DAT format produced within the DSP (ATF signal, synchronization signal, etc.) are added, 8-10 conversion is performed, and the result is output to the RF circuit as serial recording data.

- In this manner, the time compressed DAT recording signal is produced at the signal processing circuit.

2) Operation During Playback

- The data recorded on the tape is waveshaped at the RF circuit, extracted at the PLL circuit and converted to a digital signal (PBDT). Simultaneously, the playback clock (PBCK 9.408 MHz) which is synchronized with the data is generated.

- The playback data is sent to the DSP and synchronization signal detection is performed first and then 10-8 bit conversion. Then, it is separated into main data and subcode data and processed.

- The main data and pack data are written to the RAM. The data written to the RAM is read and parity based error correction is performed. It is then written again to the RAM.

- Because the main data is interleaved during recording, the DSP address control de-interleaves the data to restore it to the original audio data. This is then output to the DAC as 16-bit serial data (DADAT).

- The separated subcode data (main ID, sub ID, pack read from RAM) is sent to the system microcomputer and used for mode setting of the various blocks and FL display information.

4-4 Interface with Various Blocks

1) ADC Block

The analog signal is converted to PCM by the MASH ADC and input by the DSP as serial data.

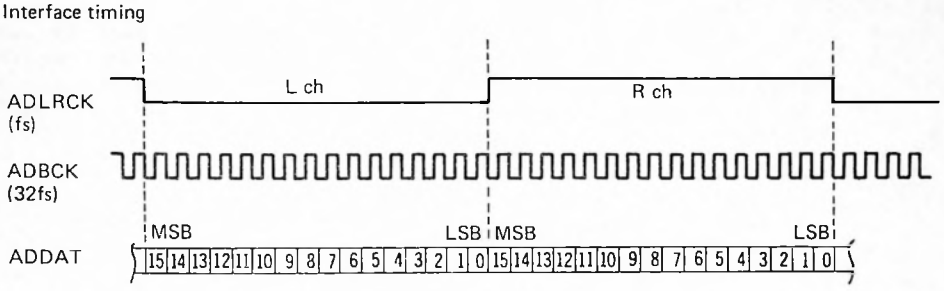


Fig. 4–2

ADMCK is the master clock for the ADC and outputs 512Fs. (Fs = 48 kHz .... 24.576 MHz)

2) DAC Block

The 16-bit serial data (DADAT) from the DSP is converted to an audio signal by the MASH DAC.

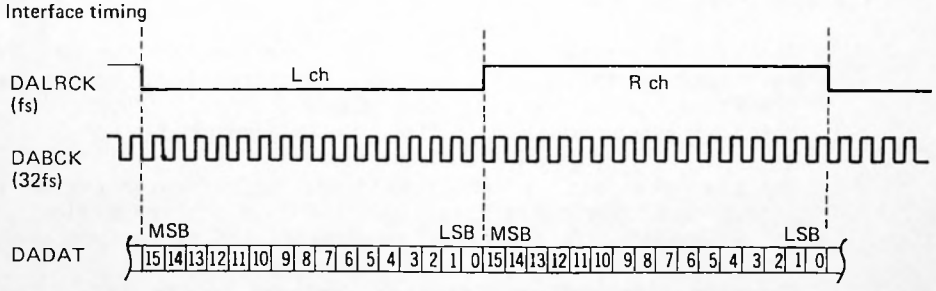


Fig. 4–3

DADAT comprises the play data during play and the source monitor data during recording.
The master clock for the DAC is the signal input by X1 to which 512 fs is applied.
Normally, for DIN (digital input), the output of the DIN PLL is switched and the signal from the crystal is used as the master clock.

48 kHz ..... 24.576 MHz
44.1 kHz .... 22.579 MHz
32 kHz ..... 16.384 MHz

3) Digital Audio Interface Block

When the input switch is set to digital, the DIN PLL circuit begins operation with DINSEL at pin (41) of system microcomputer IC301. DIOVAR and DIOREF control the DIN PLL clock frequency so that the DIN PLL output clock and digital interface input lock.

RX:	Digital interface input (Biø modulation)	IC351 Pin (23)
TX:	Digital interface output (Biø modulation) ...	IC351 Pin (22)
DI512:	Oscillation input (512 fs) of DIN PLL VCO ...	IC351 Pin (30)
DIOREF:	Reference voltage output of DIN PLL phase comparator	IC351 Pin (27)
DIOVAR:	Control voltage output of DIN PLL phase comparator	IC351 pin (28)
DUNLOK:	Out of sync indication of digital interface PLL (high when out of sync)	IC301 Pin (40)

If the DIN PLL does not lock, DUNLOK goes high (UNLOCK is high during lock detection) and the digital interface input is stopped.

4) Servo Block

Clocks and timing pulses required by the servo circuit are supplied from the DSP to the servo block. The head switch (HSW) created at the servo circuit is input and used as the signal processing timing clock.

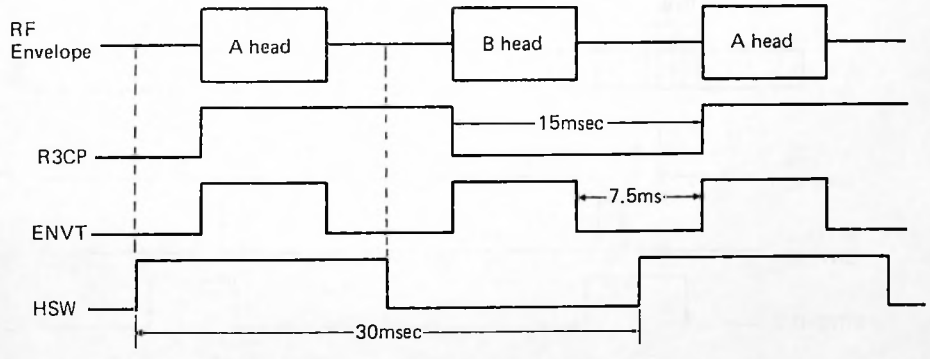


Fig. 4–4

R3CP:	Frame reference signal (33.3 Hz)	IC351 Pin (99)
ENVT:	Envelope section signal (66.6 Hz)	IC351 Pin (98)
HSW:	A/B head switching signal (33.3 Hz)	IC351 Pin (120)
M9CK:	Master clock of the servo block (9.408 MHz)	IC351 Pin (119)
NRTRST:	Rotation reset signal (initializes R3CP and ENVT)	IC351 Pin (96)

5) RF Block

The record/play switching signal (SRPR), recording signal (SRRF) when recording, and ATF window signals (SRND1, SRWND2) used for ATF level adjustment are supplied to the RF block.

(1) SRPR (record/play switching signal)

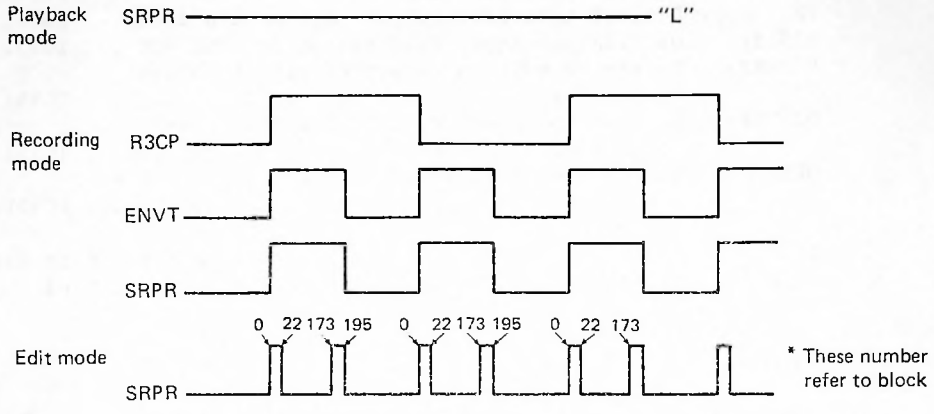
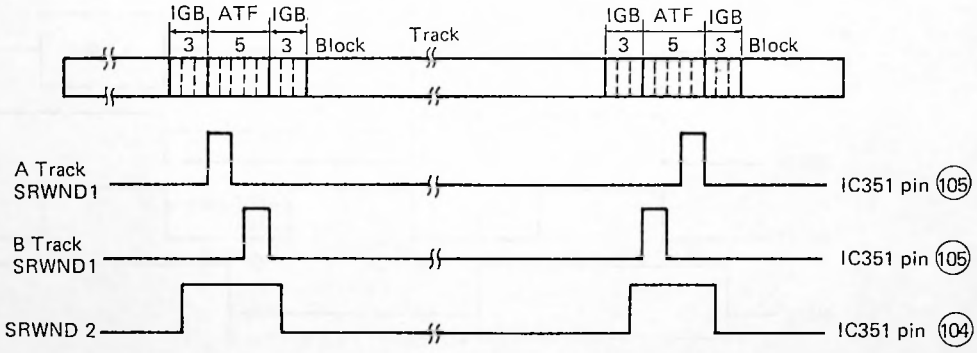


Fig. 4–5

(2) SRWND1 and SRWND2



SRWND1: PILOT interval signals for the A head and for the B head. (The positions of the PILOT signals written by the A head and by the B head differ.)

SRWND2: ATF interval signal

Fig. 4–6

6) Play PLL Block

The RF signal from the head is extracted by the PLL circuit and fed to the DSP as NRZ digital data.

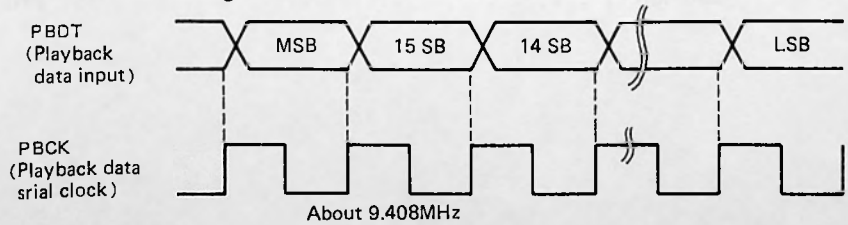


Fig. 4–7

7) Servo Block

The timing clock, master clock and PLL offset information are supplied to the servo block.

FCH (M9CK): Master clock of the servo block (9.408 MHz) ..... IC351 Pin (115)

PLLOFS: PWM signal corresponding to the deviation with respect to the target for the bit rate of input data PBDT. The tape speed in the reel mode is corrected from this data. ..... IC351 Pin (109)

VFPLFS: High when the PLLOFS data is valid ..... IC351 Pin (111)

HFCH: Frequency of PLLOFS serial bit clock FCH/2 (4.704 MHz) ..... IC351 Pin (110)

8) RAM Block

Controls the externally connected RAM (IC352) used for encoding and decoding audio data and subcode PACK data.

RDT 0-7: 8-bit data bus for the RAM

RAD 0-9, A-E: 15-bit address control bus for the RAM

NCS: Standby at RAM chip select high ..... IC351 Pin (66)

NWE: RAM write command ..... IC351 Pin (58)

NOE: RAM read command ..... IC351 Pin (63)

9) System Control Block

The setting of operating modes for the various blocks and the transfer of system data are performed by the system control block.

SPDT: Bidirectional data bus. The transferred data is given below.

(1) System control to signal processing
- Operating mode (recording, play, search, post-recording, etc.)
- Main ID to be recorded (Fs, copy inhibit, etc.)
- Subcode ID to be recorded (program no. start ID, etc.)
- Subcode information for digital out (C bit, U bit information)

(2) Signal processing to system control
- Peak level meter data
- Main ID
- Sub ID
- C1 flag error information
- Subcode information for digital input

NSPSTB: Control signal to indicate data transfer ... IC351 Pin (91)

SPAW: Address line signal from the system microcomputer ..... IC351 Pin (90)

SPRDY: Transfer enable status to the system microcomputer ..... IC351 Pin (92)

10) Master Clock Oscillation Circuit Block

Four crystals are used by the DSP to produce the master clocks for the sampling frequencies.

XI0, XI1: 28.224 MHz crystal for the M9CK master clock. ..... IC351 Pin (41), (42)
XI2: 16.384 MHz crystal for the fs=32 kHz master clock. ..... IC351 Pin (29)
XI3: 22.5792 MHz crystal for the fs=44.1 kHz master clock. ..... IC351 Pin (36)
XI4: 24.576 MHz crystal for the fs=48 kHz master clock. ..... IC351 Pin (33)

The crystals at XI2-XI4 are selected by the system microcomputer to oscillate only when required. These oscillation outputs are selected according to the sampling frequency and supplied not only to the DSP but to IC501 (DAC).

11) Master Clock Oscillation Circuit

The master clock is produced at the IC351 signal processor circuit. The 28 MHz crystal connected to XI0 and XI1 at pins ㊶ and ㊷ of IC351 is for the master clock for IC351.

(1) Analog Recording and Playback

Three crystal oscillators corresponding to the different sampling frequencies are connected and are controlled by the IC301 system microcomputer. The master clocks from these crystals are used to perform operations during analog recording and playback.

The oscillation for one of the sampling frequencies of 32 kHz, 44.1 kHz and 48 kHz in the current operation is activated and the other oscillations are stopped. The unnecessary clocks are turned off to improve the performance of MASH. This control is performed by pins ㉖, ㉗ and ㉘ of IC301 (goes high during operation).

(2) Digital Recording

In digital recording, the signal from the VCO oscillator within the DIN PLL circuit is used for the master clock. This is supplied to the IC351 signal processor and the IC501 MASH D/A converter. (See the next section for details.)

(3) Master Clock for the IC501 D/A Converter

Like the IC351 signal processor, the master clock for the MASH D/A converter also switches to one produced from a crystal for analog recording and playback, and to one produced from the DIN PLL circuit for digital recording.

IC362 consists of 2 analog switches with 4 contacts each. Switch 2 operates during analog recording and playback and switch 1 operates during digital recording. This operation is selected by SLAD at pin ㉕ of IC301 which, during digital recording, goes high and selects the circuit for switch 1.

The 32 kHz, 44.1 kHz and 48 kHz master clocks are switched by switching the switch contacts according to the 2-bit combination of FILFS1 and FILFS0 of pins ㉒ and ㉓ of IC301.

	FILFS0	FILFS1
32 kHz	L	H
44.1 kHz	H	L
48 kHz	H	H

The state of each pin is shown.

	IC301						IC362				IC362 switching output
	㉕	㉓	㉒	㉖	㉗	㉘	①	⑮	②	⑭	
32 kHz play, analog recording	L	L	H	H	L	L	L	H	L	H	Pin ⑤ input → pin ⑦ output
44.1 kHz play, analog recording	L	H	L	L	H	L	L	H	H	L	Pin ④ input → pin ⑦ output
48 kHz play, analog recording	L	H	H	L	L	H	L	H	H	H	Pin ③ input → pin ⑦ output
Digital recording	H	-	-	H	H	H	H	L	-	-	Pin ⑬ input → pin ⑨ output

Clock Selector Circuit

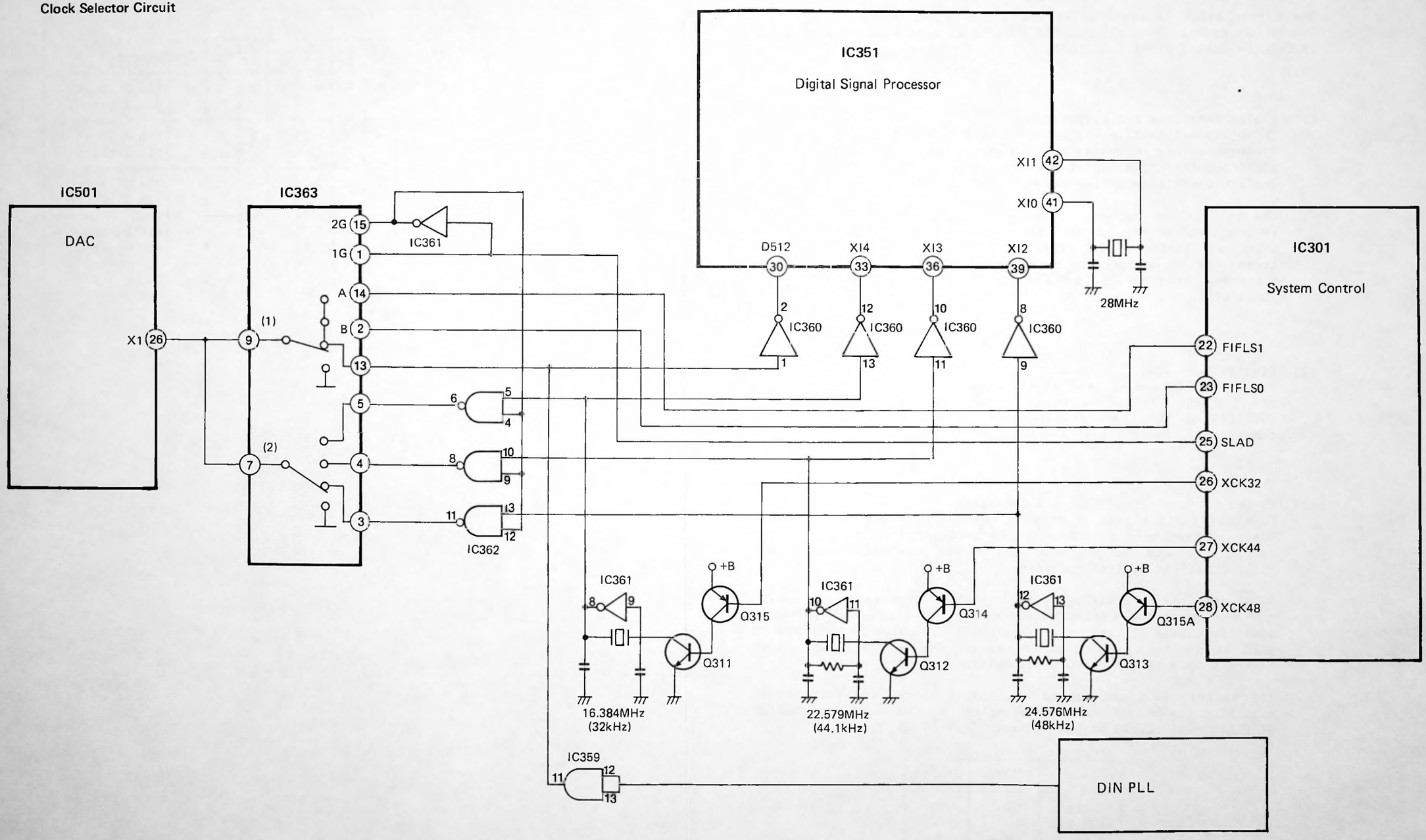


Fig. 4–8

12) Circuit Operation for Digital IN Recording

Digital IN recording operates using the master clock produced from the DIN PLL circuit. A clock, synchronized in phase to the digital data for the digital audio interface which is input from RX (IN), is produced at the PLL circuit.

The circuit configured from discrete components consists of a VCO and an integration circuit for the oscillation frequency control signal. The IC351 signal processor contains a phase comparison circuit and the result of the phase comparison of the digital input data and VCO output is supplied to the integration circuit to form a PLL circuit.

1. DIN PLL Circuit
When the DIGITAL/ANALOG switch on the front panel is set to DIGITAL, DPLINH at pin (43) of IC301 system control goes low and the DIN PLL circuit activates. Then the digital input data and VCO output have their phases compared, a DIN PLL circuit is formed and the master clock is produced.

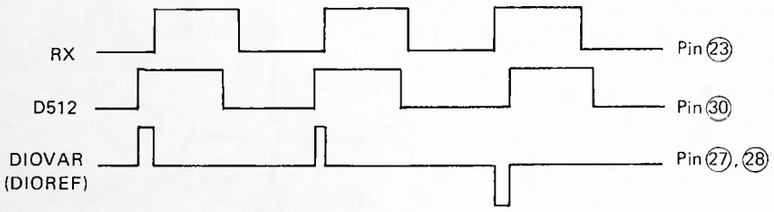


Fig. 4–9

2. Digital IN/OUT Switching Circuit
The NANDs at the input and output comprise a switching circuit for digital IN/OUT.
IC351 pin (60) P74 ARNP:
During digital recording ..... H
IC351 pin (93) DUNLOCK:
PLL unlock detect signal when unlocked ..... H
IC301 pin (40) UNLOCK:
PLL unlock detect signal when unlocked ..... H
IC301 pin (25) SLAD:
Digital/analog input switching at digital ..... H

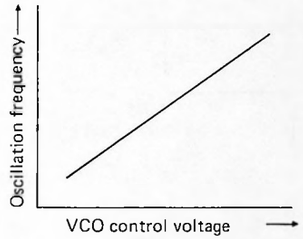
During digital recording, the output of IC359B is high and the RX digital input signal is supplied to pin 23 of IC351.

Since pin (2) of IC358A and pin (5) of IC358B both go high, RX (IN) is directly supplied to TX (OUT). This becomes a digital monitor signal during digital IN recording.

3. Operation When the PLL Does Not Lock
If the PLL unlocks for some unknown reason, the operations below are performed and the digital input is reset.

1) When the DIN PLL unlocks, unlock detection is performed within IC351 and DUNLOCK at pin (93) is set high. This unlock detect information is transferred to IC301 through the data bus and UNLOCK at pin (40) is set high.
As a result, pin 8 of IC359B goes low and the RX digital input is turned off.

2) Next, DISCHG at pin (42) of IC301 goes momentarily high which turns on Q352 in the DIN PLL circuit and temporarily lowers the VCO control voltage to its lowest level. (Discharge operation: Minimizes the oscillation frequency)



* The DIN PLL has a wide range of control to handle the sampling frequencies of 32 kHz, 44.1 kHz and 48 kHz.

3) Next, UNLOCK at pin (40) goes low when DISCHG at pin (42) resets to low. Then pin (8) of IC359B goes high and the digital input signal is input by pin (23) of IC351.

4) The VCO's phase and the input data start the phase comparison and the VCO control voltage gradually increases until the PLL finally locks.

5) When the PLL achieves phase lock, DUNLOCK at pin (93) of IC351 goes low and SLAD at pin (25) of IC301 goes high for digital input. The high at pin 3 of IC359C turns on Q351B. This is used to narrow the PLL lock range which stabilizes the DIN PLL operation when the PLL locks.

6) When the PLL unlocks during digital IN recording, the 3 crystals are in the operating state for backup purposes so that the master clock can be supplied immediately from the crystal.

Digital IN/OUT Circuit

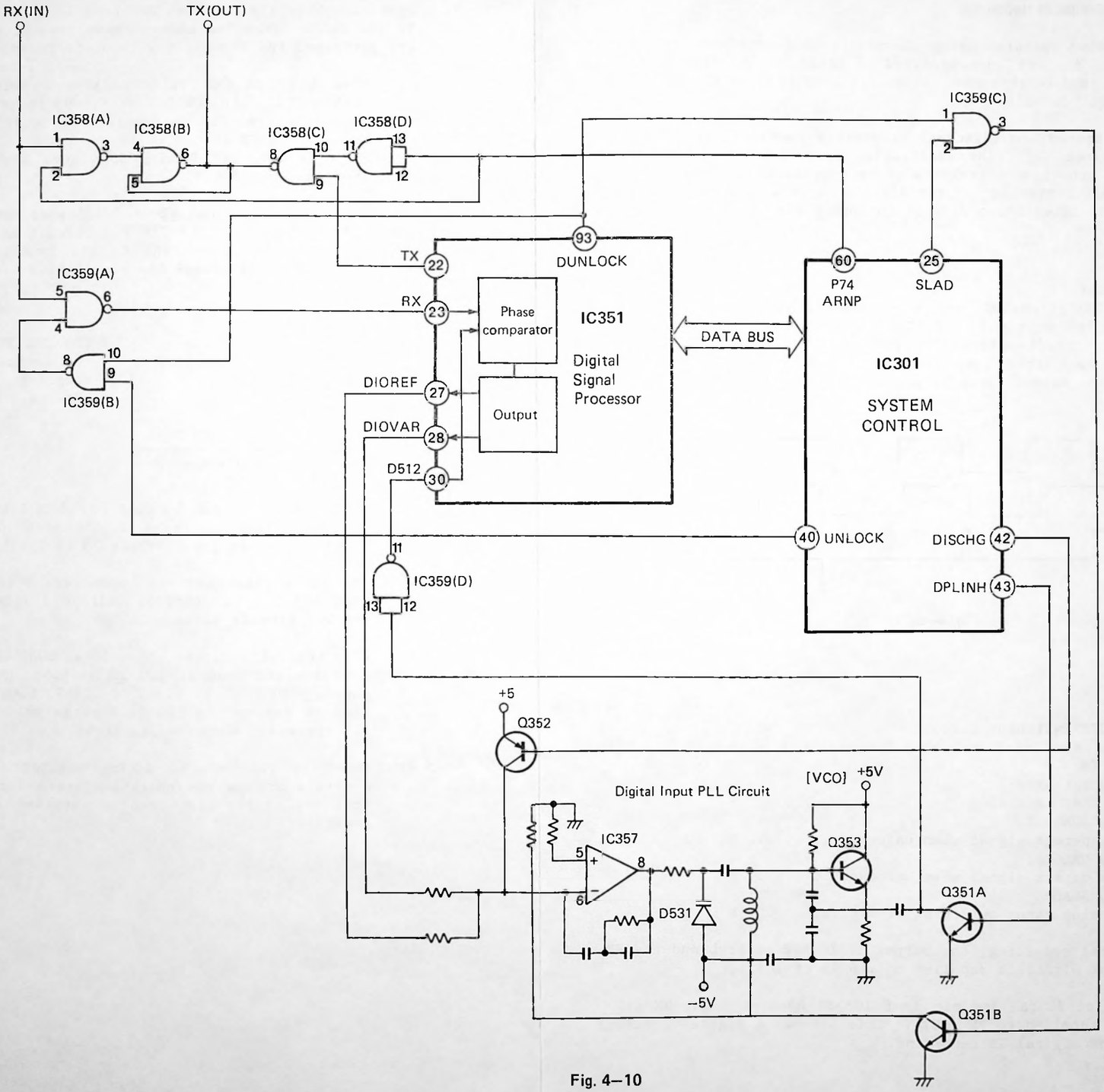


Fig. 4–10

(4. Signal Processing Circuit for SV-3700)

4-1 Overview

4-2 Main Features

4-3 Operation of the Signal Processing Block

1) Operation During Recording

2) Operation During Playback

4-4 Interface with Various Blocks

1) ADC Block

2) DAC Block

3) Digital Audio Interface Block

4) Servo Block

5) RF Block

6) Play PLL Block

7) Servo Block

8) RAM Block

9) System Control Block

10) Master Clock Oscillation Circuit Block

11) Master Clock Oscillation Circuit

12) Digital I/O Circuit

13) Circuit Operation for Digital IN Recording

4. Signal Processing Circuit for SV-3700

4-1 Overview

The digital signal processing circuit of this unit is completely contained in a single CMOS standard cell LSI chip, the MN6624. This LSI chip contains approximately 3600 gates and has a 124-pin configuration.

The processes during recording consist of adding C1 and C2 parities and then subcodes to the PCM data from the MASH A/D converter and digital audio interface, and performing 8-10 conversion.

During play, 8-10 conversion, error correction and interpolation are performed on the play RF data. PCM data is output to the D/A converter.

Therefore, the MN6624 provides all the basic functions required for R-DAT digital signal processing on a single chip. The major functions of the MN6624 are given next.

1 Recording signal generation (8-10 conversion, synchronization signal, addition of ID, ATF signal generation)

2 C1 and C2 parity generation

3 Play signal demodulation (8-10 conversion, synchronization detection, ID parity check)

4 Error correction based on C1 and C2 parities

5 Recording and playback of subcodes

6 Address control for interleave, de-interleave and error correction

7 16-bit linear data processing

8 Interpolation and previous value hold processing

9 Peak hold detection for level meter

10 Soft mute

11 Blank detection

12 IEC standard digital audio interface I/O

13 Microcomputer interface

14 Subcode post-recording

4-2 Main Features

1 Single +5 V supply operation

2 Integration of all major R-DAT signal processing functions on a single chip

3 Pack item search

4 Compatible with fs=48 kHz, 44.1 kHz and 32 kHz

5 Built-in digital audio interface I/O function

6 3 dB step digital attenuation (up/down)

7 Cue and review compatible

8 MASH A/D and D/A compatible

9 Serial copy management system compatible (SCMS)

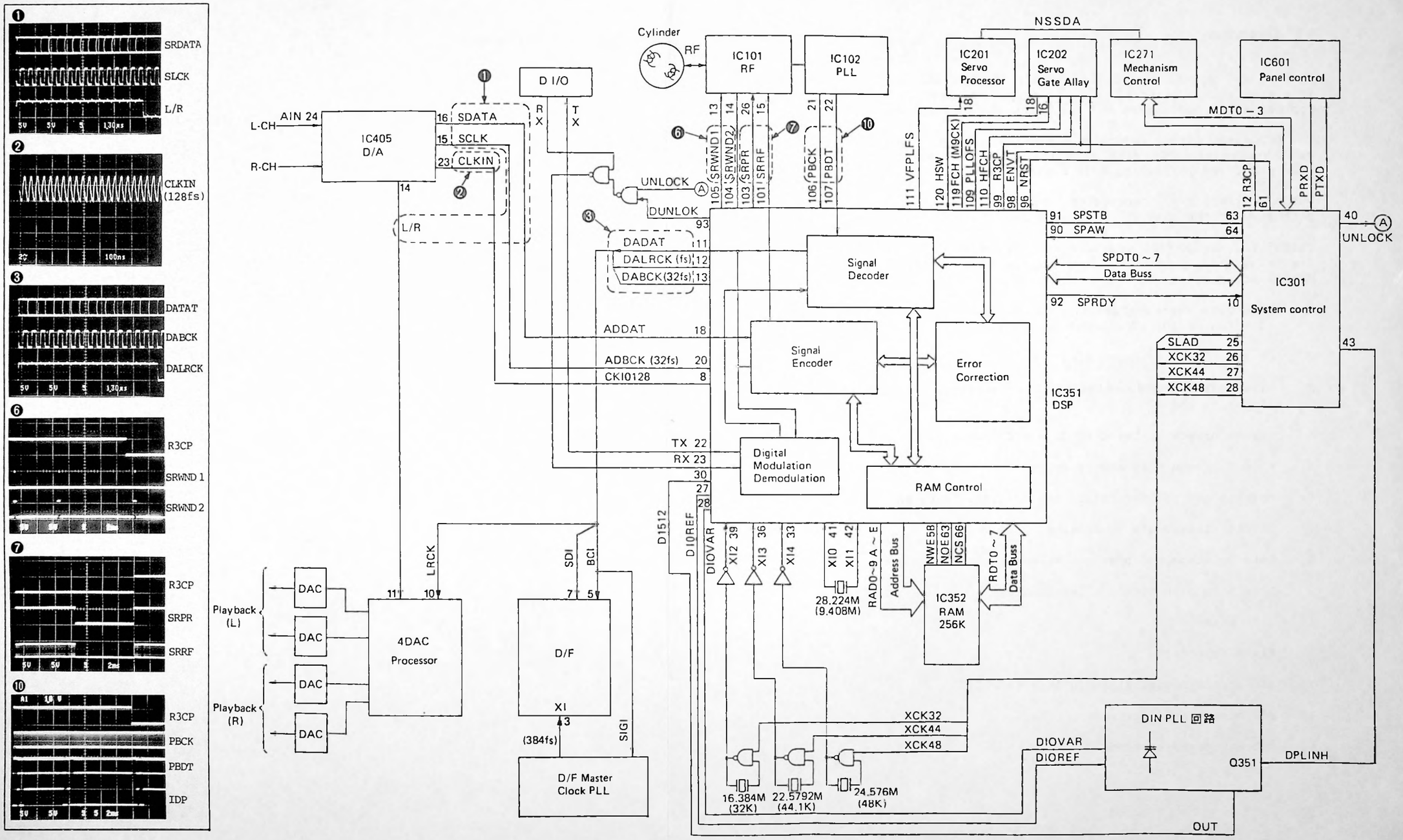


Fig. 4–1 Signal Processing Block

4-3 Operation of the Signal Processing Block

Fig. 4-1 shows the signal processing circuit and indicates the input and output signals for IC351 DSP. In addition to the single DSP IC, the signal processing circuit consists of a 256 K SRAM, 4 crystals for the master clock oscillation, and a discrete DIN PLL circuit.

1) Operation During Recording

- The analog signal is converted to 16-bit serial data by the ADC and sent to the DSP (ADDAT). The input data is written to the RAM. This data is read and the C1 and C2 parities are generated for error correction within the DSP. Then, the data and parities are again written to the RAM for the interleave.

- The subcode data generates the pack, sub ID and main ID within the DSP based on information from the system microcomputer. Like the audio data, the pack data is written to the RAM and is read for error correction to generate the C1 parity. It is then written again together with the parity.

- The data items described above are read under RAM control of the DSP. Then, the signals necessary for the DAT format produced within the DSP (ATF signal, synchronization signal, etc.) are added, 8-10 conversion is performed, and the result is output to the RF circuit as serial recording data.

- In this manner, the time compressed DAT recording signal is produced at the signal processing circuit.

2) Operation During Playback

- The data recorded on the tape is waveshaped at the RF circuit, extracted at the PLL circuit and converted to a digital signal (PBDT). Simultaneously, the playback clock (PBCK 9.408 MHz) which is synchronized with the data is generated.

- The playback data is sent to the DSP and synchronization signal detection is performed first and then 10-8 bit conversion. Then, it is separated into main data and subcode data and processed.

- The main data and pack data are written to the RAM. The data written to the RAM is read and parity based error correction is performed. It is then written again to the RAM.

- Because the main data is interleaved during recording, the DSP address control de-interleaves the data to restore it to the original audio data. This is then output to the DAC as 16-bit serial data (DADAT).

- The separated subcode data (main ID, sub ID, pack read from RAM) is sent to the system microcomputer and used for mode setting of the various blocks and FL display information.

4-4 Interface with Various Blocks

1) ADC Block

The analog signal is converted to PCM by the ΔΣ ADC and input by the DSP as serial data.

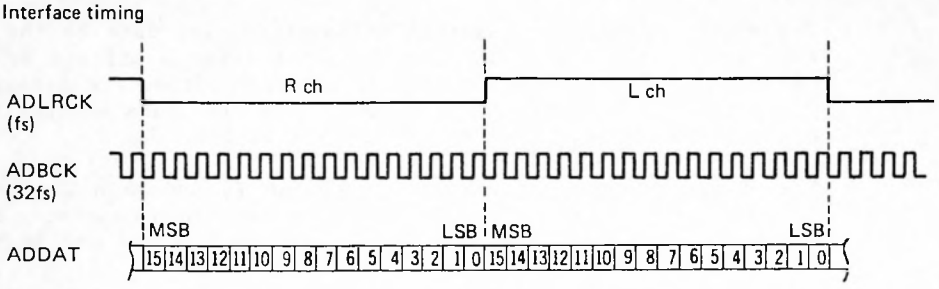


Fig. 4–2

CLKIN is the master clock for the ADC and outputs 128Fs. (Fs = 48 kHz .... 6.144 MHz)

2) DAC Block

The 16-bit serial data (DADAT) from the DSP is converted to an audio signal by the MASH DAC.

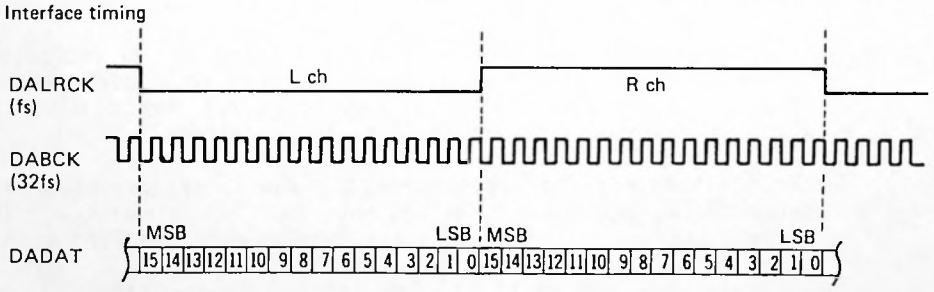


Fig. 4–3

DADAT comprises the play data during play and the source monitor data during recording.
The master clock for the DAC is the signal input by X1 to which 512 fs is applied.
Normally, for DIN (digital input), the output of the DIN PLL is switched and the signal from the crystal is used as the master clock.

48 kHz ..... 24.576 MHz
44.1 kHz .... 22.579 MHz
32 kHz ..... 16.384 MHz

3) Digital Audio Interface Block

When the input switch is set to digital, the DIN PLL circuit begins operation with DINSEL at pin (41) of system microcomputer IC301. DIOVAR and DIOREF control the DIN PLL clock frequency so that the DIN PLL output clock and digital interface input lock.

RX:	Digital interface input (Biø modulation)	IC351 Pin (23)
TX:	Digital interface output (Biø modulation) ...	IC351 Pin (22)
DI512:	Oscillation input (512 fs) of DIN PLL VCO ...	IC351 Pin (30)
DIOREF:	Reference voltage output of DIN PLL phase comparator	IC351 Pin (27)
DIOVAR:	Control voltage output of DIN PLL phase comparator	IC351 pin (28)
DUNLOK:	Out of sync indication of digital interface PLL (high when out of sync)	IC301 Pin (40)

If the DIN PLL does not lock, DUNLOK goes high (UNLOCK is high during lock detection) and the digital interface input is stopped.

4) Servo Block

Clocks and timing pulses required by the servo circuit are supplied from the DSP to the servo block. The head switch (HSW) created at the servo circuit is input and used as the signal processing timing clock.

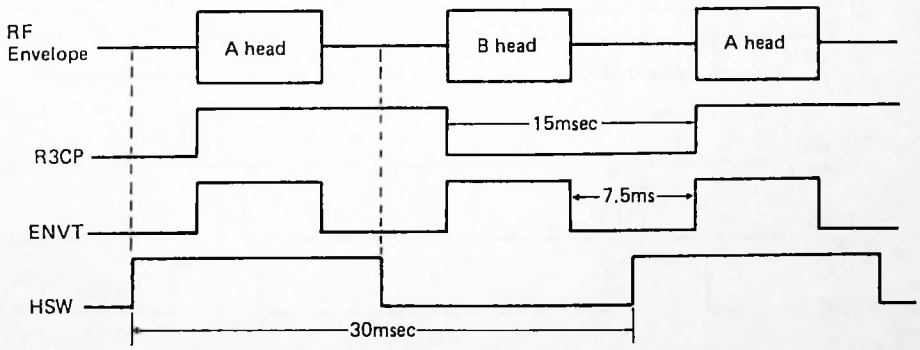


Fig. 4–4

R3CP:	Frame reference signal (33.3 Hz)	IC351 Pin (99)
ENVT:	Envelope section signal (66.6 Hz)	IC351 Pin (98)
HSW:	A/B head switching signal (33.3 Hz)	IC351 Pin (120)
M9CK:	Master clock of the servo block (9.408 MHz)	IC351 Pin (119)
NRTRST:	Rotation reset signal (initializes R3CP and ENVT)	IC351 Pin (96)

5) RF Block

The record/play switching signal (SRPR), recording signal (SRRF) when recording, and ATF window signals (SRND1, SRWND2) used for ATF level adjustment are supplied to the RF block.

(1) SRPR (record/play switching signal)

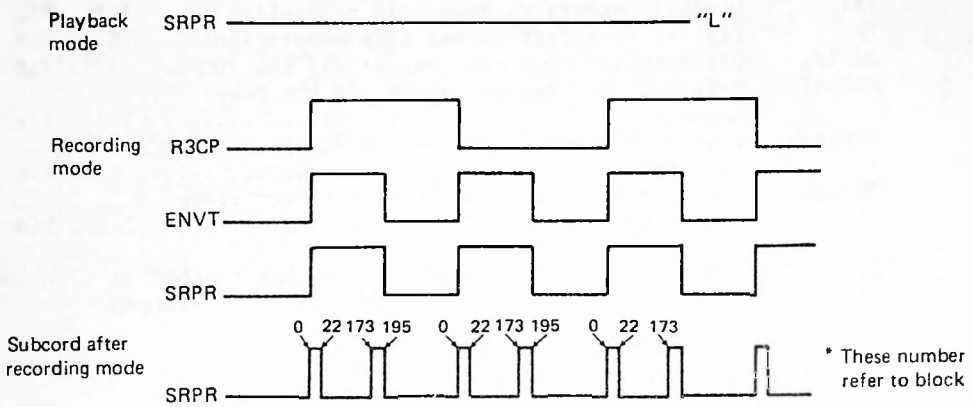
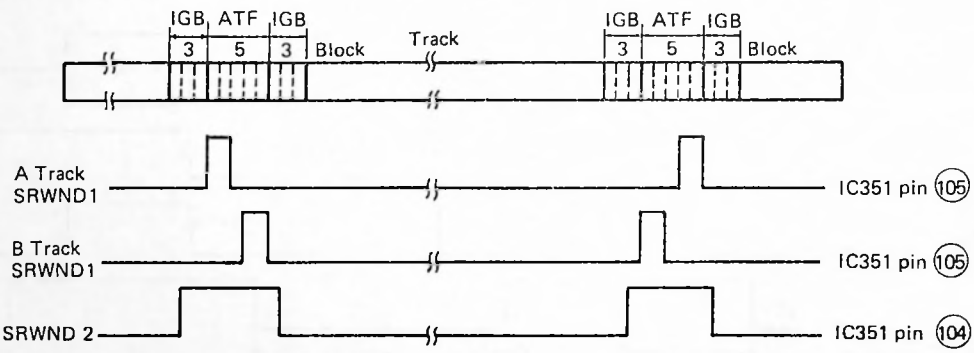


Fig. 4–5

(2) SRWND1 and SRWND2



SRWND1: PILOT interval signals for the A head and for the B head. (The positions of the PILOT signals written by the A head and by the B head differ.)

SRWND2: ATF interval signal

Fig. 4–6

6) Play PLL Block

The RF signal from the head is extracted by the PLL circuit and fed to the DSP as NRZ digital data.

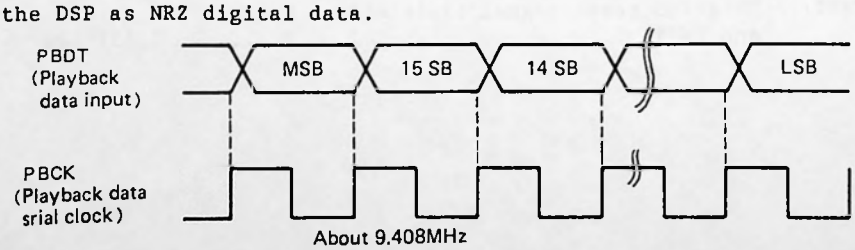


Fig. 4–7

7) Servo Block

The timing clock, master clock and PLL offset information are supplied to the servo block.

FCH (M9CK):	Master clock of the servo block (9.408 MHz)	IC351 Pin (115)
PLLOFS:	PWM signal corresponding to the deviation with respect to the target for the bit rate of input data PBDT. The tape speed in the reel mode is corrected from this data.	IC351 Pin (109)
VFPLFS:	High when the PLLOFS data is valid	IC351 Pin (111)
HFCH:	Frequency of PLLOFS serial bit clock FCH/2 (4.704 MHz)	IC351 Pin (110)

8) RAM Block

Controls the externally connected RAM (IC352) used for encoding and decoding audio data and subcode PACK data.

RDT 0-7:	8-bit data bus for the RAM	
RAD 0-9, A-E:	15-bit address control bus for the RAM	
NCS:	Standby at RAM chip select high	IC351 Pin (66)
NWE:	RAM write command	IC351 Pin (58)
NOE:	RAM read command	IC351 Pin (63)

9) System Control Block

The setting of operating modes for the various blocks and the transfer of system data are performed by the system control block.

SPDT: Bidirectional data bus. The transferred data is given below.

(1) System control to signal processing
- Operating mode (recording, play, search, post-recording, etc.)
- Main ID to be recorded (Fs, copy inhibit, etc.)
- Subcode ID to be recorded (program no. start ID, etc.)
- Subcode information for digital out (C bit, U bit information)

(2) Signal processing to system control
- Peak level meter data
- Main ID
- Sub ID
- C1 flag error information
- Subcode information for digital input

NSPSTB:	Control signal to indicate data transfer ...	IC351 Pin (91)
SPAW:	Address line signal from the system microcomputer	IC351 Pin (90)
SPRDY:	Transfer enable status to the system microcomputer	IC351 Pin (92)

10) Master Clock Oscillation Circuit Block

Four crystals are used by the DSP to produce the master clocks for the sampling frequencies.

XI0, XI1: 28.224 MHz crystal for the M9CK master clock. ..... IC351 Pin (41), (42)
XI2: 16.384 MHz crystal for the fs=32 kHz master clock. ..... IC351 Pin (29)
XI3: 22.5792 MHz crystal for the fs=44.1 kHz master clock. ..... IC351 Pin (36)
XI4: 24.576 MHz crystal for the fs=48 kHz master clock. ..... IC351 Pin (33)

The crystals at XI2-XI4 are selected by the system microcomputer to oscillate only when required. These oscillation outputs are selected according to the sampling frequency and supplied not only to the DSP but to IC501 (DAC).

11. Master Clock Oscillation Circuit

The master clock is produced at the IC351 signal processing circuit. The 28 MHz crystal connected to XI0 and XI1 at pins (41) and (42) of IC351 is for the master clock for IC351.

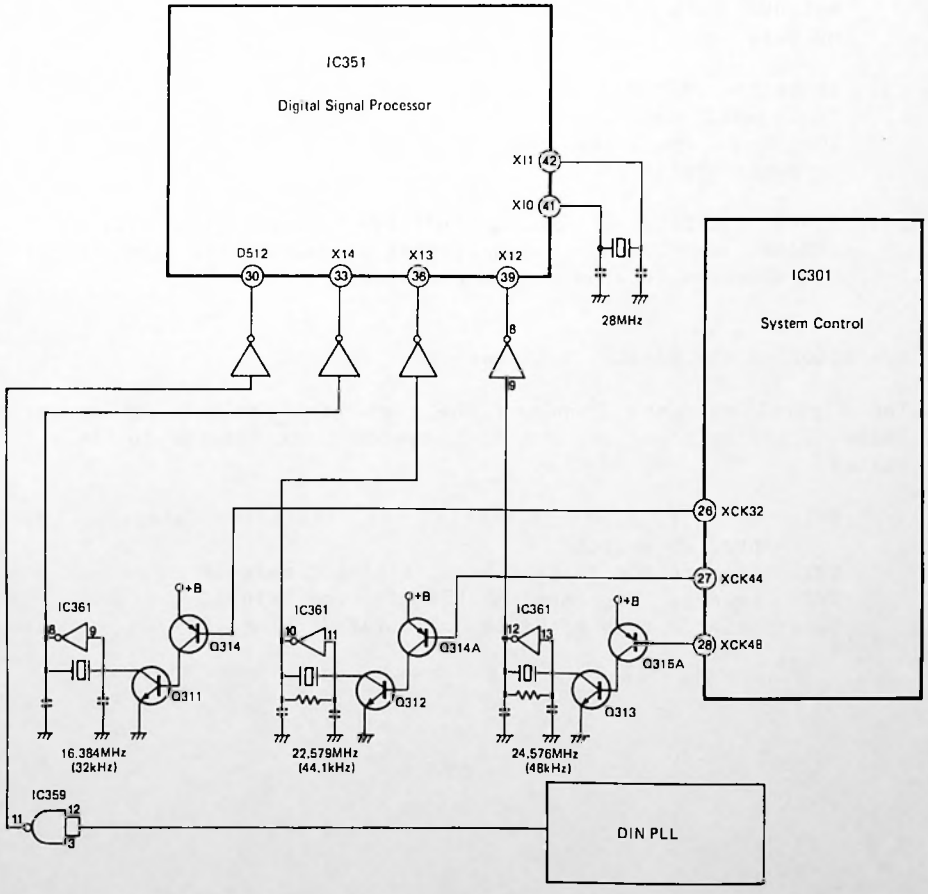
1) Analog Recording and Playback

Three crystal oscillators corresponding to the different sampling frequencies are connected and are controlled by the IC301 system microcomputer. The master clocks from these crystals are used to perform operations during analog recording and playback.

The oscillation for one of the sampling frequencies of 32 kHz, 44.1 kHz and 48 kHz in the current operation is activated and the other oscillations are stopped. The unnecessary clocks are turned off to prevent any performance degradation resulting from the mutual effects of the master clocks. This control is performed by pins (26), (27) and (28) of IC301 (goes high during operation).

2) Digital Recording

In digital recording, the output from the VCO oscillator produced by the DIN PLL circuit is used for the master clock. This is supplied to IC351. After being divided within IC351, it is also supplied to the D/A converter section as a master clock.



12. Digital I/O Circuit

The SV-3700 provides 2 sets of digital inputs and outputs for AES/EBU and IEC958 compatibility.

(1) AES/EBU:
A commercial digital audio interface I/O connector conforming to the AES (Audio Engineering Society)/EBU (European Broadcasting Union) format.
The I/O voltage is 3-10 V and the balanced I/O configuration permits long extension cords.

(2) IEC958 (SPDIF):
A coaxial I/O connector which is compatible with the IEC958 digital audio interface format.
It is a digital audio interface for consumer equipment equivalent to EIAJ TYPE II.

1) Digital I/O Circuit Configuration and Operation

(1) For the AES/EBU input, the signals for the HOT and COLD sides are combined at the balanced circuit of IC910A and supplied to the analog switch of IC909. For the output side, the digital output signal produced by the signal processing circuit is provided in 2 outputs with their phases inverted by IC910B for a balanced output.

(2) Since the IEC958 input has an input signal level of about 0.5 V, it is amplified to the TTL level by IC912A. At the output side, IC912B is connected with 3 stages in parallel to increase the current capacity.

(3) IC909 consists of analog switches which select the I/O for AES/EBU and IEC958. The switching signal is selected by setting SW4 which is located on the rear panel.

2) Operation of the Digital Switches (S902)

The digital switches found on the rear panel select the operations below. These switches set the IC301 system microcomputer to the various states.

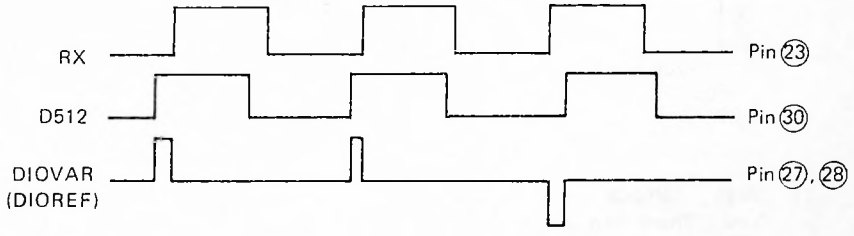
SW1: Selects blank detection or start-ID detection during program search
SW2: Selects ID6 (copy inhibit bit) for main-ID
SW3: Selects ID6 (copy inhibit bit) for main-ID
SW4: Selects type of digital I/O (AES/EBU or IEC)

13. Circuit Operation for Digital IN Recording

Digital IN recording operates using the master clock produced from the DIN PLL circuit. A clock, synchronized in phase to the digital data for the digital audio interface which is input from RX (IN), is produced at the PLL circuit.
The circuit configured from discrete components consists of a VCO and an integration circuit for the oscillation frequency control signal. The IC351 signal processor contains a phase comparison circuit and the result of the phase comparison of the digital input data and VCO output is supplied to the integration circuit to form a PLL circuit.

1) DIN PLL Circuit

When the DIGITAL/ANALOG switch on the front panel is set to DIGITAL, DPLINH at pin (43) of IC301 system control goes low and the DIN PLL circuit activates. Then the digital input data and VCO output have their phases compared, a DIN PLL circuit is formed and the master clock is produced.



2) Digital IN/OUT Switching Circuit

The NANDs at the input and output comprise a switching circuit for digital IN/OUT.

IC351 Pin (60)	P74 ARNP:	During digital recording	H
IC351 Pin (93)	DUNLOCK:	PLL unlock detect signal when unlocked	H
IC301 Pin (40)	UNLOCK:	PLL unlock detect signal when unlocked	H
IC301 Pin (25)	SLAD:	Digital/analog input switching at digital ..	H

During digital recording, the output of IC359B is high and the RX digital input signal is supplied to pin 23 of IC351.

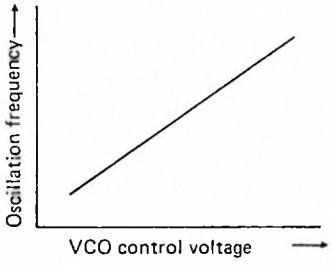
Since pin (2) of IC358A and pin (5) of IC358B both go high, RX (IN) is directly supplied to TX (OUT). This becomes a digital monitor signal during digital IN recording.

3) Operation When the PLL Does Not Lock

If the PLL unlocks for some unknown reason, the operations below are performed and the digital input is reset.

(1) When the DIN PLL unlocks, unlock detection is performed within IC351 and DUNLOCK at pin (93) is set high. This unlock detect information is transferred to IC301 through the data bus and UNLOCK at pin (40) is set high.
As a result, pin (8) of IC359B goes low and the RX digital input is turned off.

(2) Next, DISCHG at pin (42) of IC301 goes momentarily high which turns on Q352 in the DIN PLL circuit and temporarily lowers the VCO control voltage to its lowest level. (Discharge operation: Minimizes the oscillation frequency)



* The DIN PLL has a wide range of control to handle the sampling frequencies of 32 kHz, 44.1 kHz and 48 kHz.

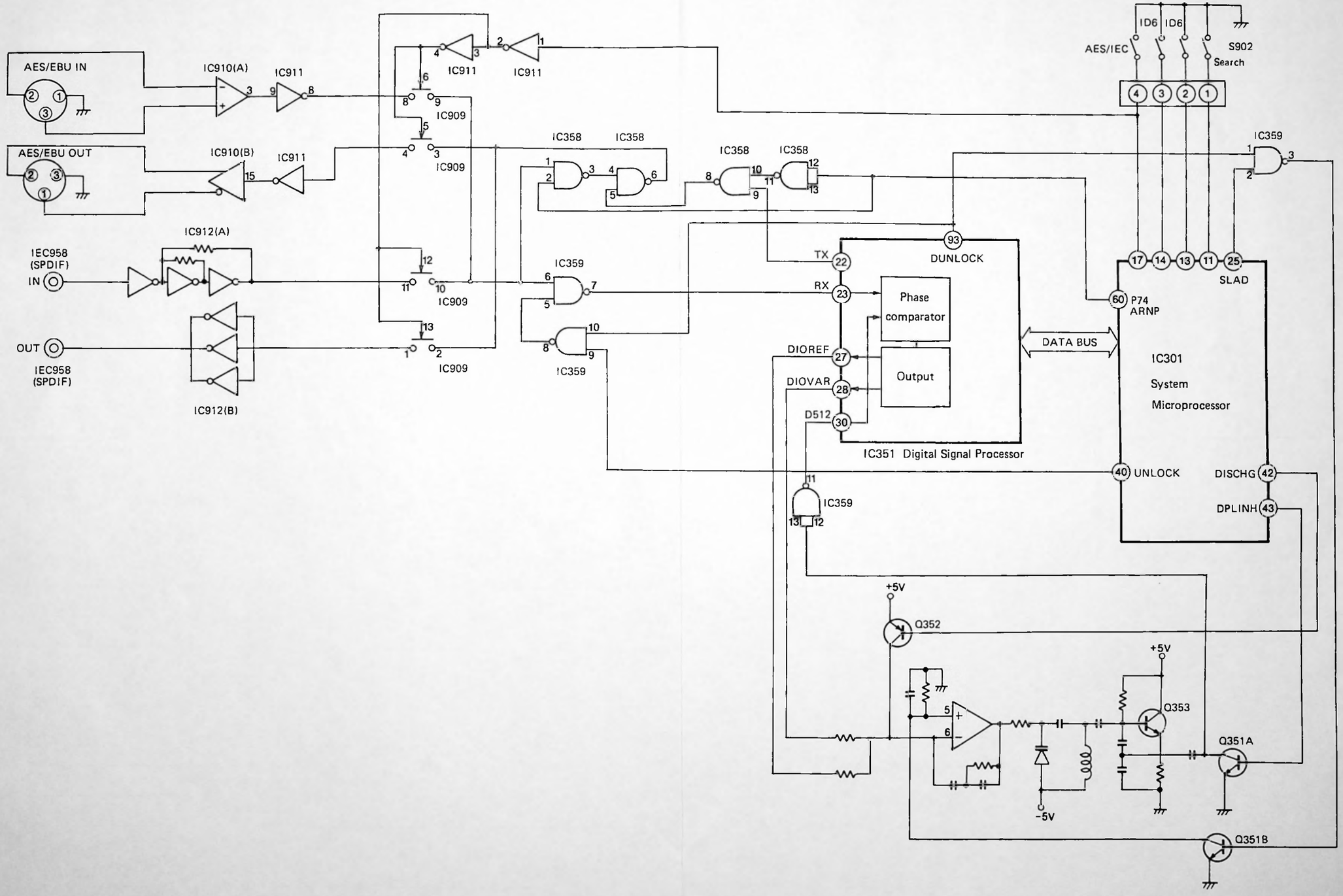
(3) Next, UNLOCK at pin (40) goes low when DISCHG at pin (42) resets to low. Then pin (8) of IC359B goes high and the digital input signal is input by pin (23) of IC351.

(4) The VCO's phase and the input data start the phase comparison and the VCO control voltage gradually increases until the PLL finally locks.

(5) When the PLL achieves phase lock, DUNLOCK at pin (93) of IC351 goes low and SLAD at pin (25) of IC301 goes high for digital input. The high at pin 3 of IC359C turns on Q351B. This is used to narrow the PLL lock range which stabilizes the DIN PLL operation when the PLL locks.

(6) When the PLL unlocks during digital IN recording, the 3 crystals are in the operating state for backup purposes so that the master clock can be supplied immediately from the crystal.

Digital IN/OUT Circuit Operation



— MEMO —

5. Servo Circuit

5. Servo Circuit

5-1 Overview

The servo circuit consists of a digital servo configuration which uses a microcomputer. Fig. 5-1 shows the schematic diagram of the servo control. In the servo circuit, the capstan and cylinder are controlled so that they rotate at the specified speeds. The servo system consists of the cylinder servo and capstan servo. Each has its own speed control and phase control which are switched according to the following mode.

	Cylinder	Capstan
Recording	Speed control + phase control	Speed control
Playback	Speed control + phase control	Speed control + ATF control
FF/REW	Speed control	Speed control

Table 5–1

For the cylinder, the speed control uses the FG signal and the phase control uses the PG signal.
The capstan uses 2 FG signal systems for speed and phase control. During FF and REW, the reel servo controls the tape speed so that the sum of the periods of the FG signals for the left and right reels is constant.

5-2 Servo Circuit Configuration

Fig. 5-2 shows the block diagram of the servo circuit. As shown in the figure, the servo circuit consists of 3 servo control ICs and 2 driver ICs (IC203, 202, 201). The major functions of each IC (IC204, 205) are described in the following.

1 Linear Servo IC (IC203)
- ° Waveshaping for capstan FG signal
- ° Waveshaping for cylinder FG and PG signals
- ° Waveshaping for reel motor FG signal
- ° ATF control voltage generation

2 Servo Gate Array IC (IC202)
- ° Generation of ATF sampling pulses, SP1, SP2 and SPE
- ° Head switching signal (HSW) generation
- ° Capstan FG signal synthesis
- ° Switching for the input port supply signal to the servo processor

3 Servo Processor (IC 201)
This IC with built-in ADC, DAC and D/F is a 16-bit microcomputer developed for VTR applications. Although its basic operation is the same as that of a VTR servo circuit, it performs digital servo operations with the addition of DAT specific signal processing.
- ° Capstan speed control signal generation and output
- ° Cylinder speed control signal and phase control signal generation
- ° Reel servo control signal generation

4 Capstan and Cylinder Drives (IC204, IC205)
Each IC comprises a circuit which drives a 3-phase motor. IC204 uses a switching power supply which supplies a voltage corresponding to the rotational speed. A fixed voltage is used for the cylinder drive.

These circuits enable the capstan and cylinder to be rotated at the specified speeds during the recording, playback, FF and REW modes.

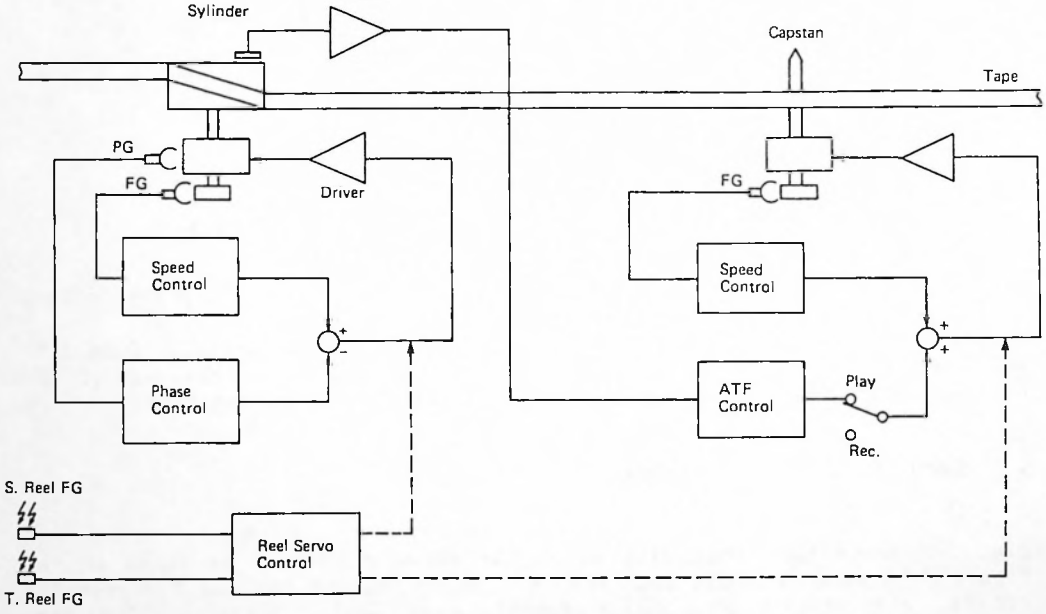


Fig. 5—1 Servo Circuit Block

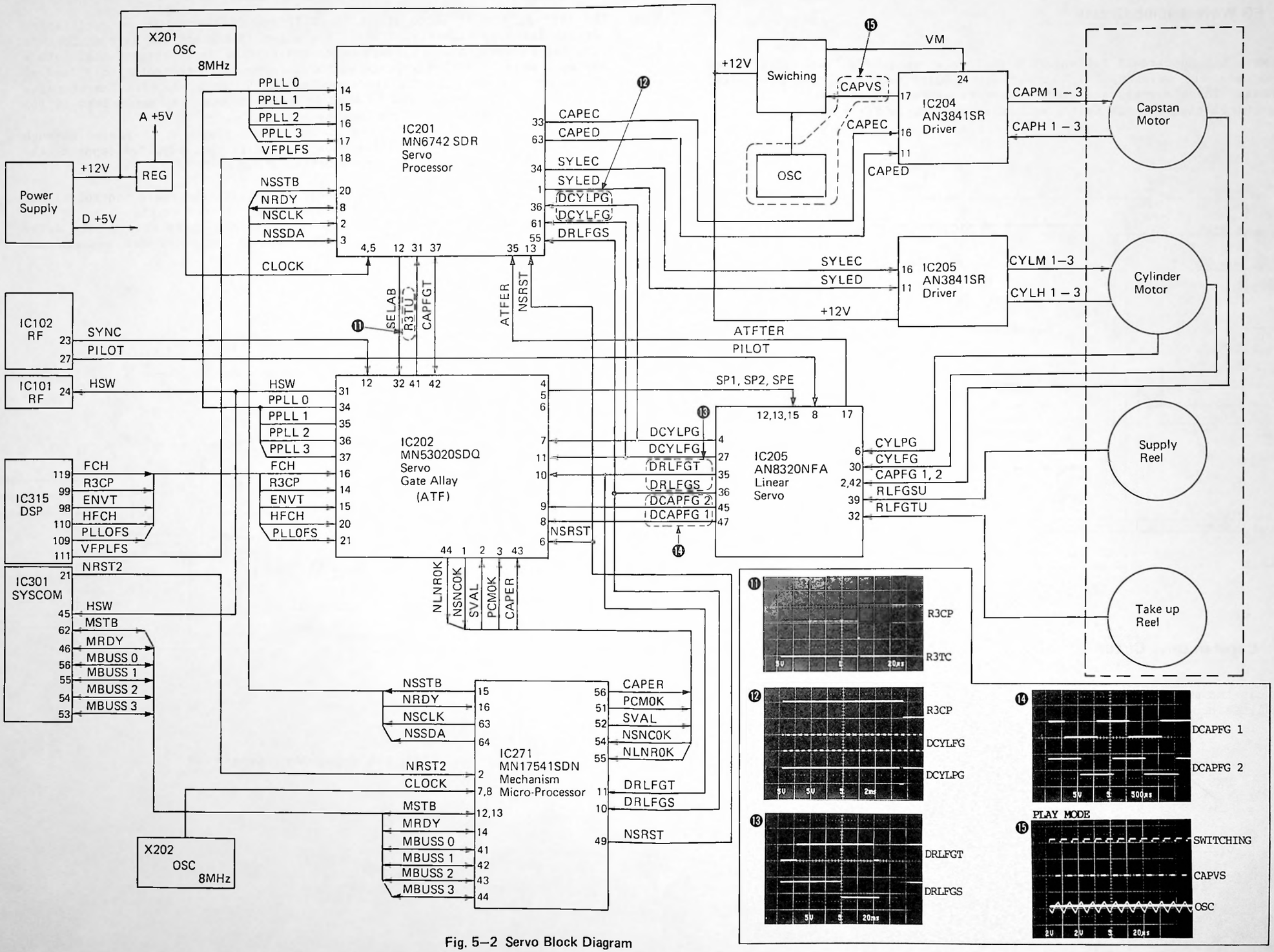


Fig. 5–2 Servo Block Diagram

5-3 FG Waveshaping Circuit

The waveshaping circuit for the FG signal is shown in Fig. 5-3. The FG and PG signals are waveshaped in linear servo IC205 and converted to digital signals. These signals are used to execute servo control.
The reel FG signal input by the mechanism control is for counter control.

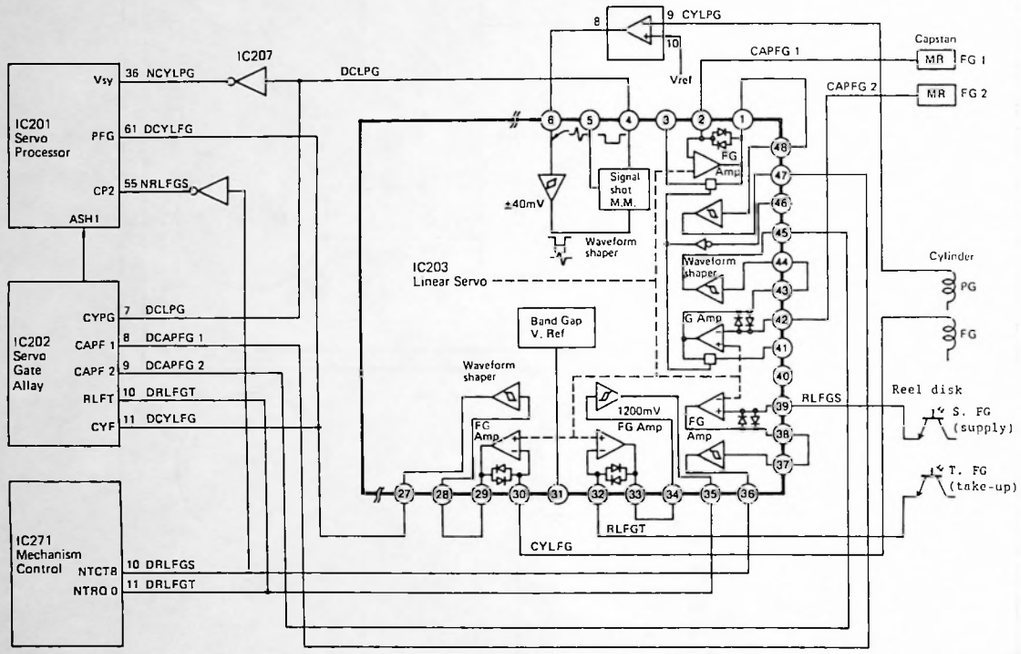


Fig. 5–3 FG Waveshaping Circuit

5-4 Capstan Drive Circuit

The capstan motor is a 3-phase motor. The voltage applied to the drive IC, IC204, is produced and output from the switching power supply.

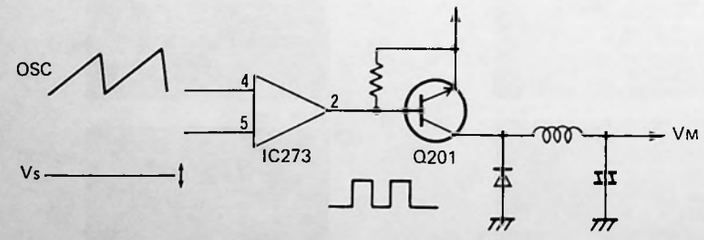


Fig. 5–4 Switching Power Supply

The left op amp of IC206 and R275, R277 and C273 comprise an oscillation circuit for approximately 80 kHz. The right op amp and the surrounding RCs comprise an integration circuit which changes the oscillating signal into a sawtooth wave. Vs is a voltage which corresponds to the rotational load of the motor. These voltages are compared and VM is produced. Therefore, a high VM when the motor load is high or a low VM when the motor load is low is applied to the drive IC to improve efficiency.
Since the load is extremely low during normal play, VM is passed through D203 which regulates the voltage when low and is then supplied (approx. 4.4 V). The switching power supply operates during FF/REW.

CAPEC supplied from the servo processor (IC201) is the speed control signal and CAPED is the rotational direction command. (Refer to Fig. 5-5.)
Like the capstan motor, the cylinder motor is a 3-phase motor. The drive circuit is the same as that for the capstan but does not contain the switching power supply.

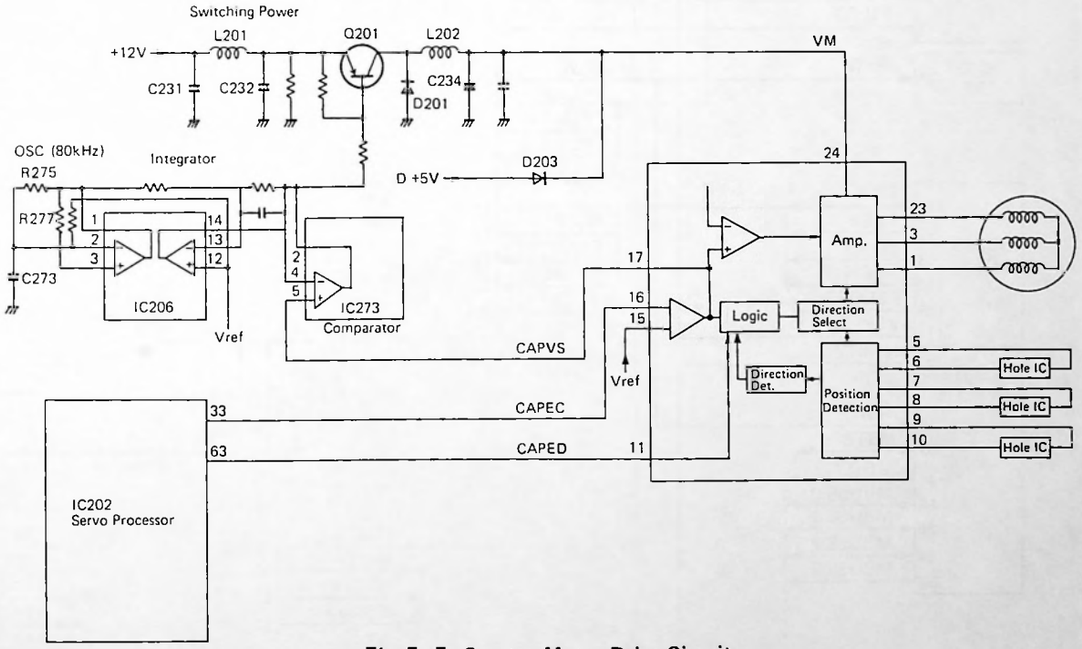


Fig. 5–5 Capstan Motor Drive Circuit

5-5 ATF Signal Generation Circuit

The ATF signal generation circuit is shown in Fig. 5-7. The pilot signal for the adjacent track detected by the RF circuit is sampled and held with SP1 and SP2, and its voltage difference is supplied to the servo processor as ATFTER (during play).
SP1, SP2 and SPE are generated in the servo gate array using the ATFSYNC signal and supplied to the linear servo.

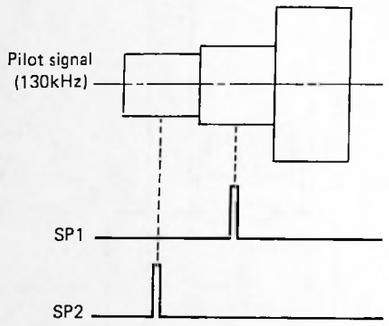


Fig. 5–6

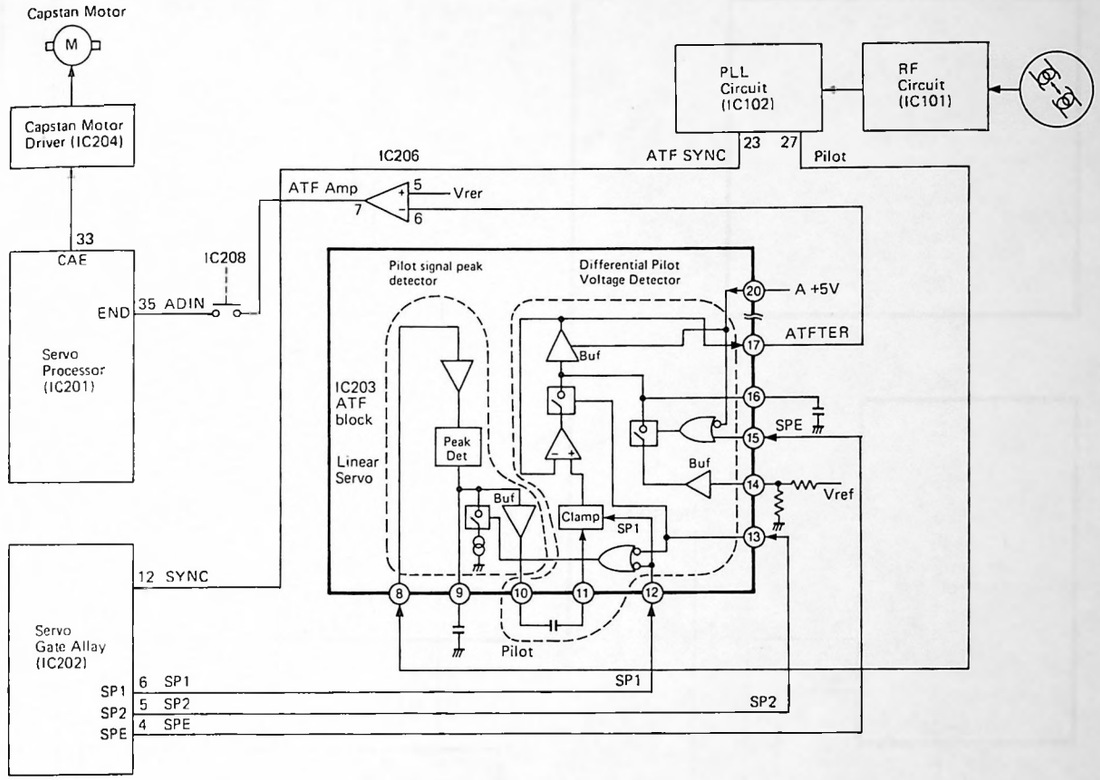


Fig. 5–7 Signal Generation Circuit

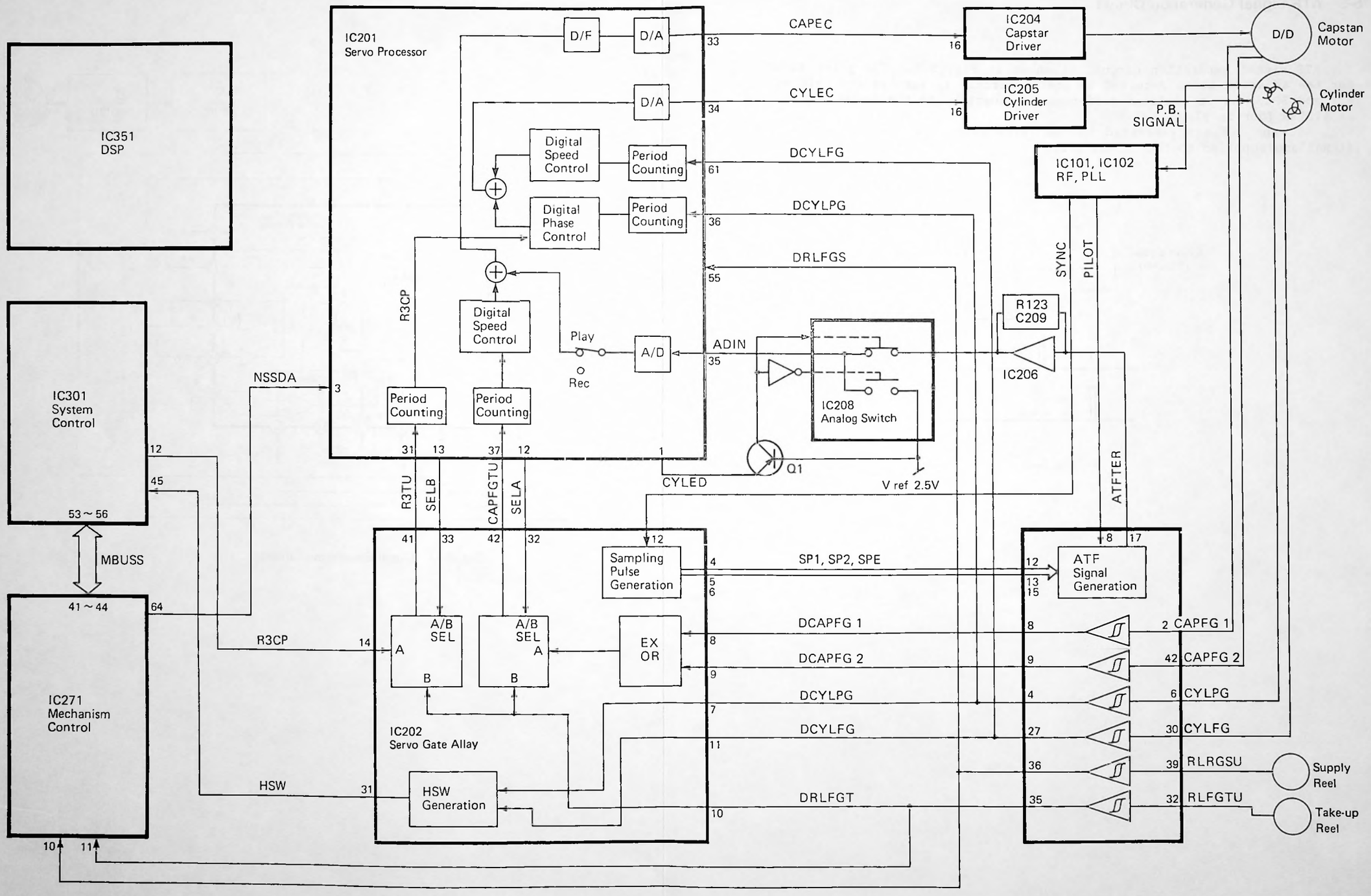


Fig. 5–8 Block Diagram of REC/PLAY Mode (Servo Circuit)

5-6 Servo Circuit Operation During Recording

Fig. 5-8 shows the block diagram of the servo operation during recording and playback. This block diagram is used to describe the servo operation during recording.

1) When the REC button is pressed, this information is received by the panel control which transfers it to the system control. Then, the system control transfers the operation mode command (MBUSS) to the mechanism control. Based on the information, the mechanism control sends various motor rotation commands (NSSDA) to the servo processor and sets the servo mode.

2) The capstan motor is activated and the FG signals (FG1, FG2) is fed to the servo circuit. This signal is used by the servo circuit to control the capstan speed. Since the cylinder is also rotating, FG and PG are fed to the servo circuit and control the rotation speed.

3) The servo system during recording is set by the servo processor (IC201) in the following manner.
   - Capstan motor: Speed control
   - Cylinder motor: Speed control + phase control

4) The capstan FG is synthesized at EXOR within the servo gate array (IC202) and fed to the servo processor (IC201) (CAPFGTU). The period of the FG signal is counted by the counter and the speed error is processed as a digital signal.

5) The digital speed error data is converted to an analog voltage at the DAC within the servo processor. As CAPEC, it is fed to the capstan driver (IC204) for capstan speed control.

6) Similarly, the rotation error can be detected by counting the periods of the cylinder FG and PG. The cylinder FG for the speed error and the cylinder PG for the phase error are digitally processed and added. The added data is converted to analog at the DAC and becomes the rotational speed command (CYLEC).

5-7 Operation During Playback

The block diagram in Fig. 5-8 is used for the description. As in recording, the servo mode is set in the order of panel control → system control → mechanism control → servo processor. The servo mode during playback is set in the following manner.
- Capstan motor: Speed control + ATF
- Cylinder motor: Speed control + phase control

1) ATF Control
   The ATF control voltage produced by the linear servo (IC203) is output as ATFTER. This voltage is first amplified by the op amp of IC206. (This reduces the quantization error when loading to ADIN of the servo processor.) The amplified ATFTER signal first passes the analog switch of IC208 and is then input by the servo processor as ADIN. This is to input the reference voltage Vref (2.5 V) which is necessary for the servo processor to calculate the ATF control voltage.

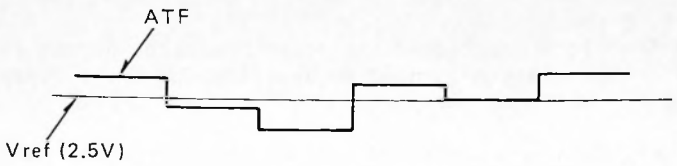


Fig. 5–9

To detect the ATF error voltage, Vref is first input beforehand and stored. Next, the amplified ATFTER voltage is input, the voltages are compared and the error voltage is detected.
The loading of the reference voltage Vref is performed while the cylinder is stopped (when cassette is replaced, etc.). When the cylinder rotational direction command CYLEP is the STOP command, Q1 turns on and the reference voltage is loaded.

* The ATF signal is converted from analog to digital in the servo processor (8-bit A/D converter). During this time, the signal is first amplified by IC206 to reduce the error since quantization error is generated if the ATF signal is small. Since the capstan motor speed suddenly changes if the ATF signal suddenly increases, the waveform is smoothed by the integration circuit.

2) Capstan Control
The ATF voltage input by the servo processor is converted to digital data at the ADC and added to the FG-based speed control data. This data (CAPEC) controls the rotational speed of the capstan.

3) Cylinder Control
The cylinder is controlled in exactly the same manner as in recording.

5-8 Operation During FF and REW Modes

It is necessary for the DAT to read subcode data (A-Time, PNO, etc.) also during FF and REW. For this reason, the rotational speed of the cylinder is changed at the same time the tape speed is changed and control is performed to keep the relative speed constant.

Therefore, during FF and REW, the mode is switched to the reel servo mode which uses the reel FG signal. In the servo circuit, the speed of the capstan motor is varied so that the sum of the periods of the FG signals for the take-up and supply reels becomes constant.

The speed is increased while varying it in x25 steps for a maximum of x250 during FF and x225 during REW. (Although the tape speed increases to x400 when the FF or REW button is pressed twice, the subcode is not read at this speed.)

Fig. 5-11 shows the block diagram of the servo operation in the FF and REW modes. This block diagram is used for the description.

1 The reel mode of the servo circuit is set by serial data NSSDA from the system control through the mechanism control. The servo processor (IC201) is set only to the capstan speed control and cylinder speed control mode. (At the same time, the maximum speed is transferred.)

2 When the reel mode is set, the capstan speed is first forcibly raised so that the tape speed is x12.5. R3TU is fed to the servo processor and take-up reel FG signal RLFGT is selected only in this x12.5 mode.

3 The sum of the periods of take-up reel FG (DRLFGTU) and supply reel FG (DRLFGSU) is calculated at the reel FG sum setting block of the servo processor. The period sums for x25, x37.5, x50, x62.5, x75, until x250 are calculated and set based on the sum of the reel periods at x12.5. (Once the period sum is set at x12.5, this mode is omitted as long as the tape is not removed.)

4 Next, the tape speed is raised to x25. The take-up reel FG is switched to CAPFGTU. Similarly, the reel servo output is fed to the capstan driver so that the sum of the periods of both reel FGs is attained.

5 When the sum of the reel periods reaches a constant x25, speed lock is detected. The speed lock detection is performed within the servo processor. When speed lock is detected, control is performed so that the next speed of x50 is attained. This operation is repeated until the final speed is reached.

6 So that the subcode is read with greater accuracy during FF/REW (reel servo mode), the PLL offset information detected by the signal processing IC (IC315) is supplied to the servo circuit and the tape speed is fine adjusted within the speed locked range at the various speeds. The amount of deviation from the reference is detected by the play data block in the signal processing IC and the amount of error is output as PLLOFS.

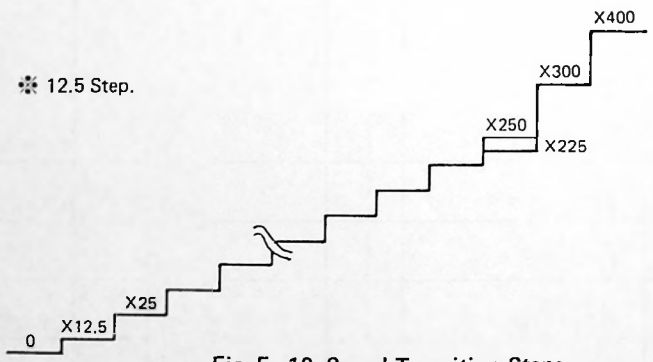


Fig. 5—10 Speed Transition Steps

<Tape Near End Detection>

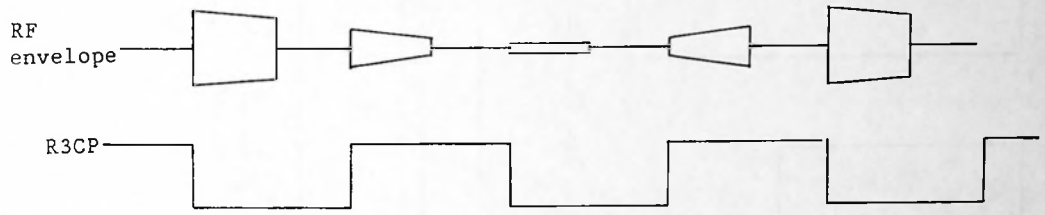
Since there is the danger of the tape breaking when the end is reached at high speeds, the near end is detected when the radius of the wound tape on the supply reel reaches 9.5 mm. This is performed by detecting the period of FG for the supply reel.

When the near end is detected, the speed is decreased to x100 and the end is set after approximately 10 seconds of tape travel.

5-9 Shuttle Search Operation

During shuttle search, the speed command is transferred from the system control to the mechanism control to the servo processor for speeds of x1/2, x1, x3, x5, x9 and x15.
The rotational speed of the cylinder during this operation is the same as during play at 2000 rpm. However, since the tape speed varies, it is necessary to devise a method to read the data. Therefore, the servo circuit activates the ATF operation only at the entrance of a track.

(1) Operation at 1/2 Speed



Since the tape speed is slow, the A and B heads are inclined and trace the same track. Therefore, the RF envelope is output erratically (due to inverted azimuth). To best read the data, the ATF control is activated each time only at the entrance of the B head. (Signal SVAL at pin (52) of IC271 mechanism microcomputer controls the ATF operation.)

(2) Other Speed Modes

Similar to the 1/2 speed above, this time the ATF control is performed only at the entrance of the A and B heads to read as much data as possible since the tape speed is fast.

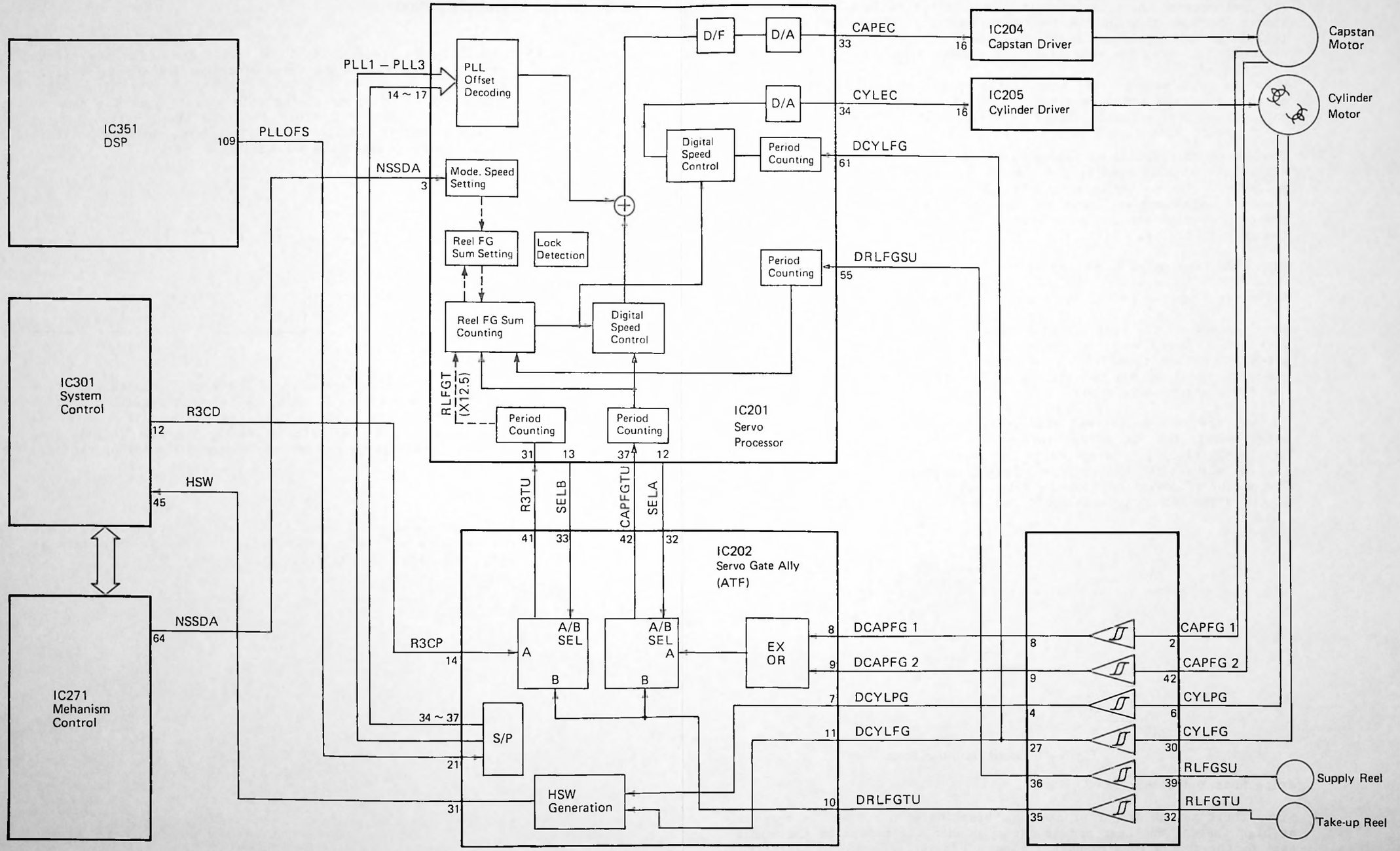


Fig. 5–11 Block Diagram for FF/REW Mode (Servo Circuit)

6. System Control Circuit

6-1 Overview of the System Control Circuit

6-2 System Control Block Diagram

6-3 Signal Flow

1) Signal Processing Circuit and System Control Circuit

2) Panel Control Circuit and System Control Circuit

3) Mechanism Control Circuit and System Control Circuit

6. System Control Circuit

6-1 Overview of the System Control Circuit

1) Reset Control
   * When the system controller exits the Reset state after power on, it releases the Signal Processor, Panel Controller, Servo Processor, and audio circuit from the Reset state, in this order.

2) Clock Control
   * Generates and cancels (32, 44.1, 48) x 512 kHz clocks depending on the recording mode and FS reconstruction playback.

3) Audio Control
   * Provides muting On/Off control.
   * Activates/deactivates the emphasis and de-emphasis circuits.
   * During recording, selects the Din PLL clock for digital input or the crystal-controlled clock for analog input.
   * Inserts or removes a low-pass filter depending on the shuttle playback speed.
   * Selects the crystal frequency according to the FS.

4) Panel Control
   * Receives key codes from the momentary, lock, remote control and shuttle keys, decodes them, and sets the operation mode according to the received key code.
   * Provides FL display data (level meter, counter, ID) and LED on/blink control.

5) Signal Processing Control
   * Selects signal processing mode.
   * Sets main and sub ID data to be recorded, and detects them during playback.
   * Provides soft mute for muting.

6) Din PLL Control
   * Activates/deactivates the Din PLL.
   * Provides control for servo unlock, and a discharge command.

7) Mechanism Control
   * Sets Mechanism Controller mode.
   * Sets tape speed.

8) Protection
   * Unloads the tape if a lockup occurs during mode transition.
   * Unloads the tape if the mechanism is left in the Pause mode for 2 hours.
   * Unloads the tape if the cylinder gathers condensation.
   * Closes the tray when it is pushed by hand.

9) Other Processes
   * Detects the presence of envelope.
   * Computes remaining tape time.
   * Computes error rate for each head.
   * Stores cue positions and searches for them at 400-times speed during Search.

6-2 System Control Block Diagram

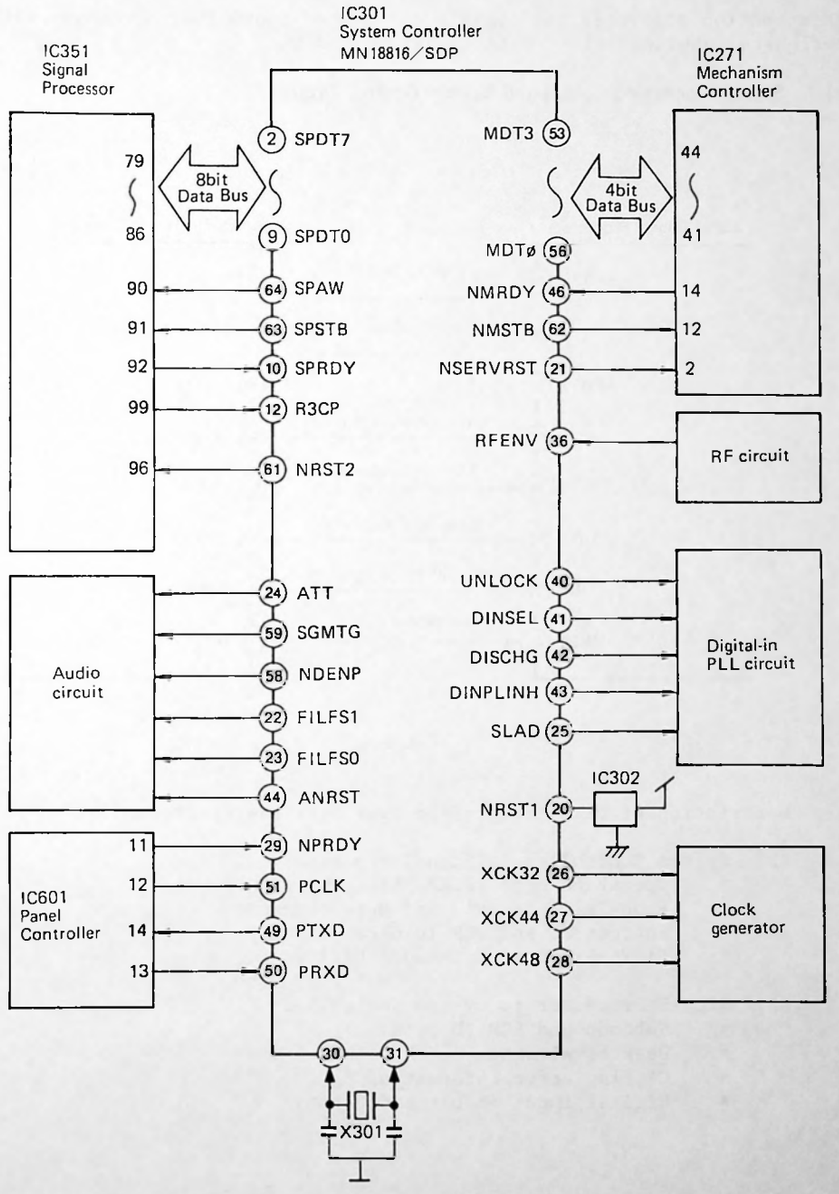


Fig. 6–1

6-3 Signal Flow

This section describes the signals the System Controller exchanges with its peripheral devices, along with signal processing.

1) Signal Processing Circuit and System Control Circuit

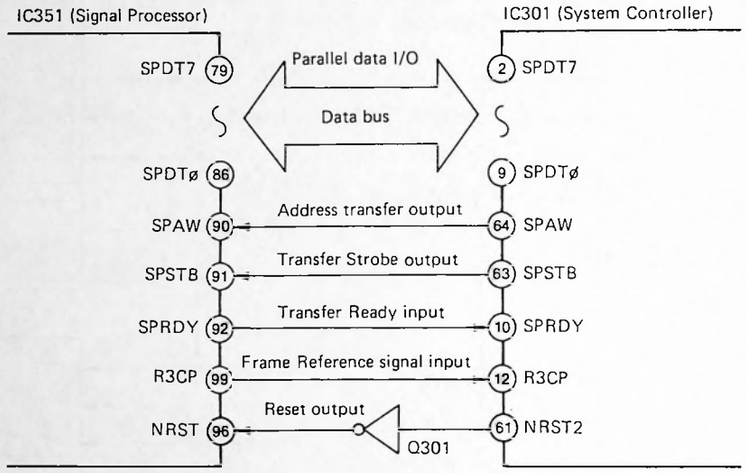


Fig. 6–2

Description of Data Transferred over Data Bus (SPDTϕ-SPDT7)

(1) System Controller to Signal Processor
- * Operation mode (PLAY, REC, FF, SEARCH, etc.)
- * Fade-In, Fade-Out, and Mute commands
- * Subcode ID and PCM ID data
- * Digital out (c bit and u bit)

(2) Signal Processor to System Controller
- * Subcode and PCM ID data
- * Peak level data
- * C1 flag error information
- * Digital input (c bit and u bit)

(1) SPAW (address write signal), SPSTB (transfer strobe signal) and SPRDY (transfer ready signal) are 8-bit parallel data transfer signals which use SPDT0 to SPDT7.

Transfer Timing Chart

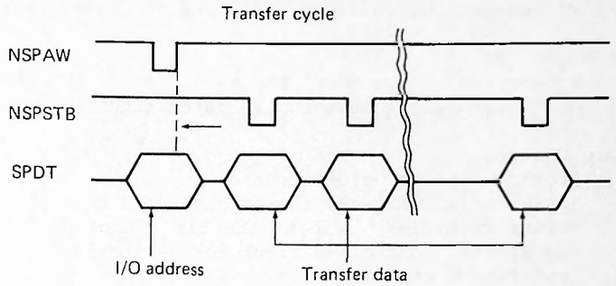


Fig. 6–3

(2) R3CP is a frame reference input of 33.3 Hz.
(3) NRST2, a reset pulse output used to reset the signal processing IC (IC351), is inverted by Q301 and input by pin 96 of IC351.

2) Panel Control Circuit and System Control Circuit

Serial data transfers are performed on the lines for PTXD (transmit data) and PRXD (receive data) based on NPRDY (transfer ready signal) and PCLK (transfer clock signal). (Refer to the panel control circuit.)

<Serial Data Contents>
(1) System Control to Panel Control
- ° FL display data
- ° LED on and flashing data

(2) Panel Control to System Control
- ° Mode transfer is performed from the code reception and key determination of a non-lock key, lock key, shuttle key, or remote controller key.

3) Mechanism Control Circuit and System Control Circuit

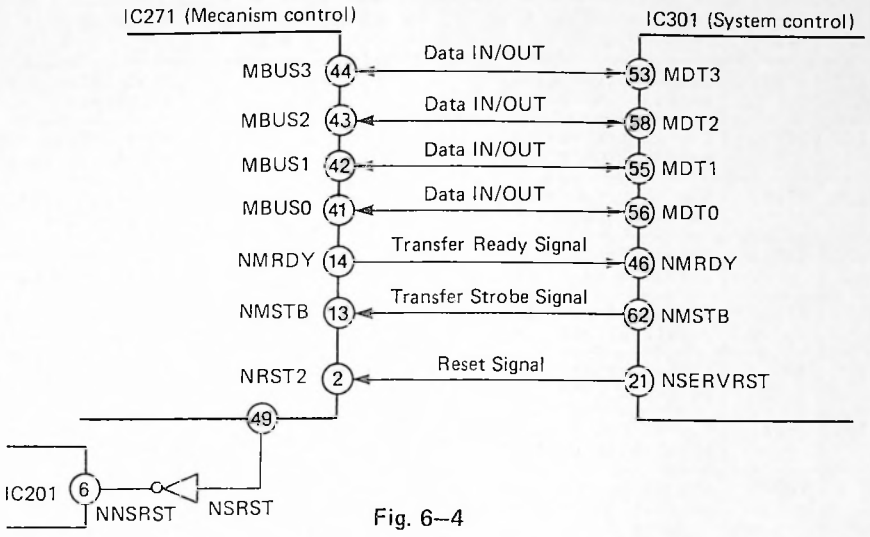


Fig. 6–4

Data Transferred on the Data Bus (MDT0-MDT3)

(1) System Control to Mechanism Control
Mode command, speed command, final speed command, track pitch signal, counter reset signal and SPEMASK signal.

(2) Mechanism Control to System Control
Current mode information, current speed information, tape begin-end information, mechanism lock information, tray information, accidental erasure information, cassette detect information, reel counter information and error information.

(1) Data transfer is performed using MDT0-MDT3 based on MSTB (strobe information) and MRDY (ready signal).

Transfer Timing Chart

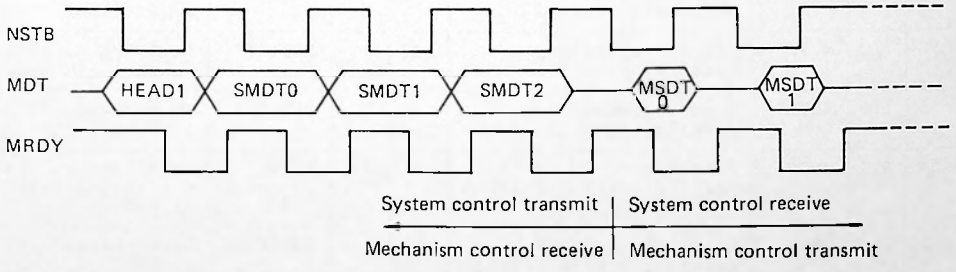


Fig. 6–5

(2) NSERVRST (reset pulse signal), a reset signal which is input by pin 2 of mechanism control IC271, resets the mechanism control. The reset pulse output from pin 49 of IC271 is inverted by the inverter of IC207, input by pin 6 of servo processor IC201 and resets the servo IC.

IC301 System Microcomputer Pin Description

Pin	I/O	Signal Name	Function	Pin	I/O	Signal Name	Function
2	I/O	SPDT7	Signal processing parallel data I/O (MSB)	45	I	HSW	Head switch input 1: A head
3	I/O	SPDT6	Signal processing parallel data I/O (MSB)	36	I	RFENV	RF envelope information input 1: Envelope present
4	I/O	SPDT5	Signal processing parallel data I/O (MSB)	11	I	ENVT	Envelope section 1: Envelope
5	I/O	SPDT4	Signal processing parallel data I/O (MSB)	12	I	R3CP	Frame reference signal Period: 30 ms
6	I/O	SPDT3	Signal processing parallel data I/O (MSB)	58	O	NDEMP	De-emphasis control signal 0: ON
7	I/O	SPDT2	Signal processing parallel data I/O (MSB)	59	O	SGMTG	Analog output muting output 1: Mute
8	I/O	SPDT1	Signal processing parallel data I/O (MSB)	39	O		
9	I/O	SPDT0	Signal processing parallel data I/O (LSB)	24	O	ATT	Cue/rev high cut 0: ON
63	O	SPSTB	Signal processing transfer strobe output	40	O	UNLOCK	D-IN PLL unlock output 0: Detecting
64	O	SPAW	Output which indicates address transfer to signal processing	41	O	DINSEL	D-IN frequency 0: 32 k, 44.1k, 48 k
10	I	SPRDY	Signal processing transfer ready input 1: Ready	42	O	DISCHG	D-IN PLL discharge command 1: Act
49	O	PTXD	Serial data output to panel control	43	O	DINPLINH	1: Disabled
50	I	PRXD	Serial data input from panel control	22	O	FILFS1	Clock frequency select 11: 48 kHz 10: 44.1 kHz 01: 32 kHz
51	O	PCLK	Transfer clock output to panel control	23	O	FILFS0	
29	I	NPRDY	Panel control transfer ready input 0: Ready	25	O	SLAD	Input select output 1: DIGITAL IN
53	I/O	MDT3	Parallel data I/O with mechanism control	26	O	XCK32	32 kHz oscillation control 1: Oscillation
54	I/O	MDT2	Signal processing parallel data I/O (MSB)	27	O	XCK44	44.1 kHz oscillation control 1: Oscillation
55	I/O	MDT1	Signal processing parallel data I/O (MSB)	28	O	XCK48	48 kHz oscillation control 1: Oscillation
56	I/O	MDT0	Signal processing parallel data I/O (LSB)	61	O	RST2	Panel control, signal processing reset output 1: RST
62	O	MSTB	Mechanism control transfer strobe output	21	O	NSERVRST	Servo reset output 0: RST
46	I	NMRDY	Mechanism control transfer ready input 0: Ready	44	O	ANRST	Analog reset output 1: RST

Table 6–1

7. Panel Control Circuit

7. Panel Control Circuit

7-1 Panel Control Circuit Block Diagram

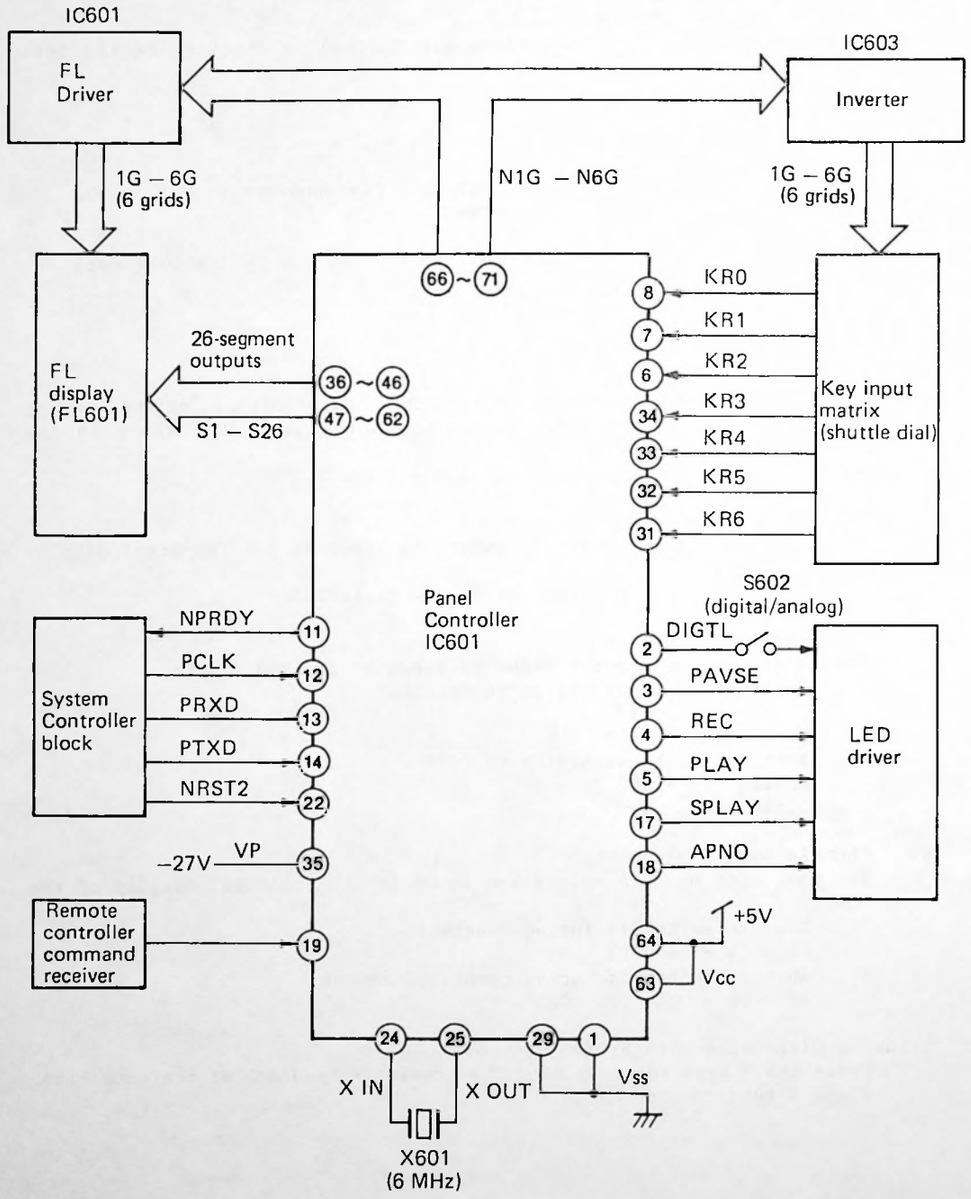


Fig. 7–1 Panel Controller-Block Diagram

7-2 Overview of the Panel Control Circuit

The SV-DA10 employs a microprocessor (IC601) dedicated to panel control. Data is serially transferred to and from the System Controller, so there are only a few connections between the two processors.

IC601 Controller Functions

- Key scan input
  Scans the key matrix to test lock switches (including shuttle dial) and momentary switches, and transfers key codes to the System Controller.

- Remote control command decoding
  Decodes remote control commands and transfers decoded instructions to the System Controller.

- Data transfer to System Controller
  Transfers 4-byte code repeatedly, in the sequence of momentary key code, lock switch code, and shuttle dial code.

- Data reception from System Controller
  Receives FL display data (time code, PNO, mode information, etc.), LED on (blink) data, and Peak level data from the System Controller.

- FL display and LED driving
  Drives the FL display and LEDs according to display data received from the System Controller.

- Level meter driving
  (1) Level display: Creates level meter driving data based on level data received from the System Controller and drives the FL level meter.
  (2) Peak hold: Resets peak level data at approx. 2 second interval.

7-3 Data Transfer with the Panel Control Circuit

Data transfer with the panel control circuit is performed in serial using PTXD and PRXD.

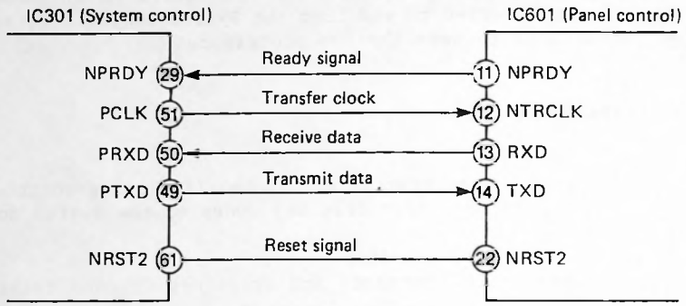


Fig. 7–2

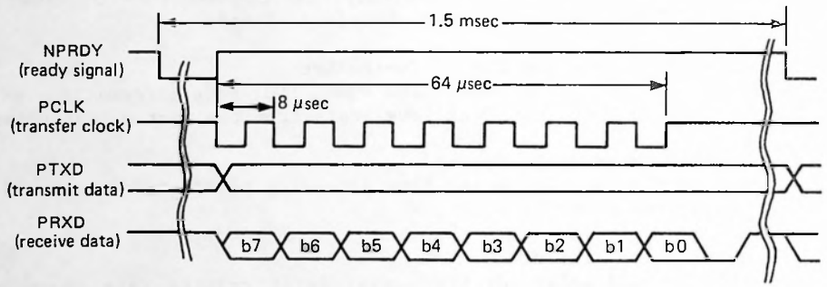


Fig. 7–3

Transfer Data Contents

System control ← Panel control

Transmit data	Non-lock key code	Lock switch code	Shuttle switch code	Remote control code	

System control → Panel control

Receive data	Time code	PNO	Mode display	Level meter information

Table 7–1

The data above is transferred by sending and receiving 8-bit serial data for 15 times during 1.5 ms.

7-4 Panel Control Unit Troubleshooting

For the panel control unit diagnostics,

(1) FL and LED illumination
(2) Various key switch inputs
(3) Transfer with the system control are checked by shorting of the test jumpers.

FL and LED Diagnostic

TP602 is shorted → All indicators turn on. Disconnected output signal lines can be checked.

Remote Controller, Key Switch, Lock Switch and Shuttle Switch Diagnostic

TP601 is shorted

1. Remote Controller Diagnostic
   By pressing a remote controller key, the "hours" display of the counter shows "8" and the code corresponding to the switch is shown in the "minutes" display.
   * Code table for the key switches → Table 7-2

2. Key Switch Diagnostic
   The code corresponding to the switch is shown in the "minutes" display of the counter.
   * Code table for the key switches → Table 7-2

3. Lock Switch Diagnostic
   The corresponding numeric value is shown on the PNO display.
   ° Setting the input select to "analog":
     Timer rec → 41
     Timer play → 42
   ° Setting the timer switch to "off":
     Analog → 40
     Digital → 48

4. Shuttle Switch Diagnostic
   The following numeric values are shown in the "seconds" display of the counter.
   ° Shuttle switch is turned clockwise:
     00 → 04 → 06 → 02 → 03
   ° Shuttle switch is turned counterclockwise:
     00 → 08 → 0C → 0E → 0A

Transfer Diagnostic with System Control
Press the 3 keys (counter "mode" + "reset" + "pause") at the same time. A and B turn on.

Code Table for All Key Switches (TP601 shorted)

Key Name	"Minutes" Display of Counter		Note
	Panel Key	Remote Controller Key	
open/close	00	01	Display for the remote controller key is 8+XX.
rew/rev	25	02	
stop	04	00	
play	05	0A	
ff/cue	24	03	
rec	13	08	
pause	14	06	
auto rec mute	12	82	
Skip FWORD	15	4A	
Skip REVERSE	16	49	
music scan	01	46	
1 *		10	Switches with * are only found on the remote controller
2 *		11	
3 *		12	
4 *		13	
5 *		14	
6 *		15	
7 *		16	
8 *		17	
9 *		18	
0 *		19	
memory *		A7	
recall *		81	
end search	35	E9	
repeat *		47	
start–ID	33	D0	
skip–ID	32	D1	
0EE (end mark)	31	D2	
ID–write	06	D3	
ID–erase	36	D4	
renumber	26	42	
skip play cancel	02	EA	
auto PNO	21	D8	
fade in	22	28	
fade out	23	29	
counter mode	20	55	
counter reset	30	54	

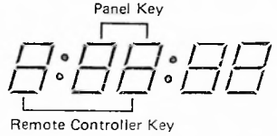


Fig. 7–4

FL Display Tube Grid

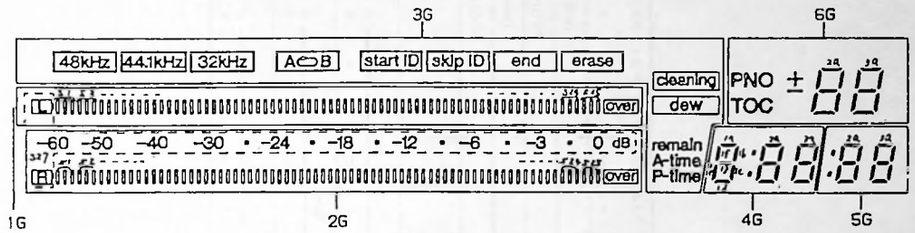


Table 7–2

ANODE CONNECTION

	1G	2G	3G	4G	5G	6G
S1	||| |||	48KHz	-	-	-
S2	||| |||	44.1KHz	-	-	-
S3	||| |||	32KHz	-	-	-
S4	||| |||	A	1a	-	-
S5	||| |||	⊂	1b	-	-
S6	||| |||	B	1f	-	-
S7	||| |||	start ID	1g	-	PNO
S8	||| |||	skip ID	1c	-	TOC
S9	||| |||	end	1e	-	+
S10	||| |||	erase	1d	-	–
S11	||| |||	-	col,1	col,2	-
S12	||| |||	-	2a	2a	2a
S13	||| |||	cleaning	2b	2b	2b
S14	||| |||	dew	2f	2f	2f
S15	||| |||	-	2g	2g	2g
S16	||| |||	remaln	2c	2c	2c
S17	||| |||	A-time	2e	2e	2e
S18	||| |||	P-time	2d	2d	2d
S19	||| |||	-	-	-	-
S20	||| |||	-	3a	3a	3a
S21	||| |||	-	3b	3b	3b
S22	||| |||	-	3f	3f	3f
S23	||| |||	-	3g	3g	3g
S24	||| |||	-	3c	3c	3c
S25	||| |||	-	3e	3e	3e
S26	over	over	-	3d	3d	3d
S27	L	R -60~0 dB	-	-	-	-

Table 7–3

Port / Grid	P51	P50	P17	P16	P15	P14	P13	P12	P11	P10	P07	P06	P05	P04	P03	P02	P01	P00	P47	P46	P45	P44	P43	P42	P41	P40
	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q	r	s	t	u	v	w	x	y	z
P65 / 1G	⇐ L-ch level meter ⇒																									over
	LOW																									HIGH
P64 / 2G	⇐ R-ch level meter ⇒																									over
	LOW																									HIGH
P53 / 3G	48kHz	44.1kHz	32kHz	A	repeat	B	start ID	skip ID	end	ERASE	PAUSE		clean-ing	dew		remain	A-time	P-time					Δ1			
P62 / 4G				⇐ Hours Δ1 ⇒							:	⇐ Minutes H ⇒								⇐ Minutes L ⇒						
				a	b	f	g	c	e	d		a	b	f	g	c	e	d		a	b	f	g	c	e	d
P61 / 8G											:	⇐ Seconds H ⇒								⇐ Seconds L ⇒						
												a	b	f	g	c	e	d		a	b	f	g	c	e	d
P60 / 6G							PNO	TOC	+	−		⇐ PNO H ⇒								⇐ PNO L ⇒						
												a	b	f	g	c	e	d		a	b	f	g	c	e	d

Table 7–4

8. Mechanism Control Circuit

8. Mechanism Control Circuit

8-1 Overview of the Mechanism Control Circuit

The Mechanism Controller (IC271) provides all mechanism control funcitons according to System Controller commands. Receiving mechanism control information, it controls the mode motor (DC), tray motor (DC), and the capstan (DD) and cylinder (DD) motors via the Servo Processor.

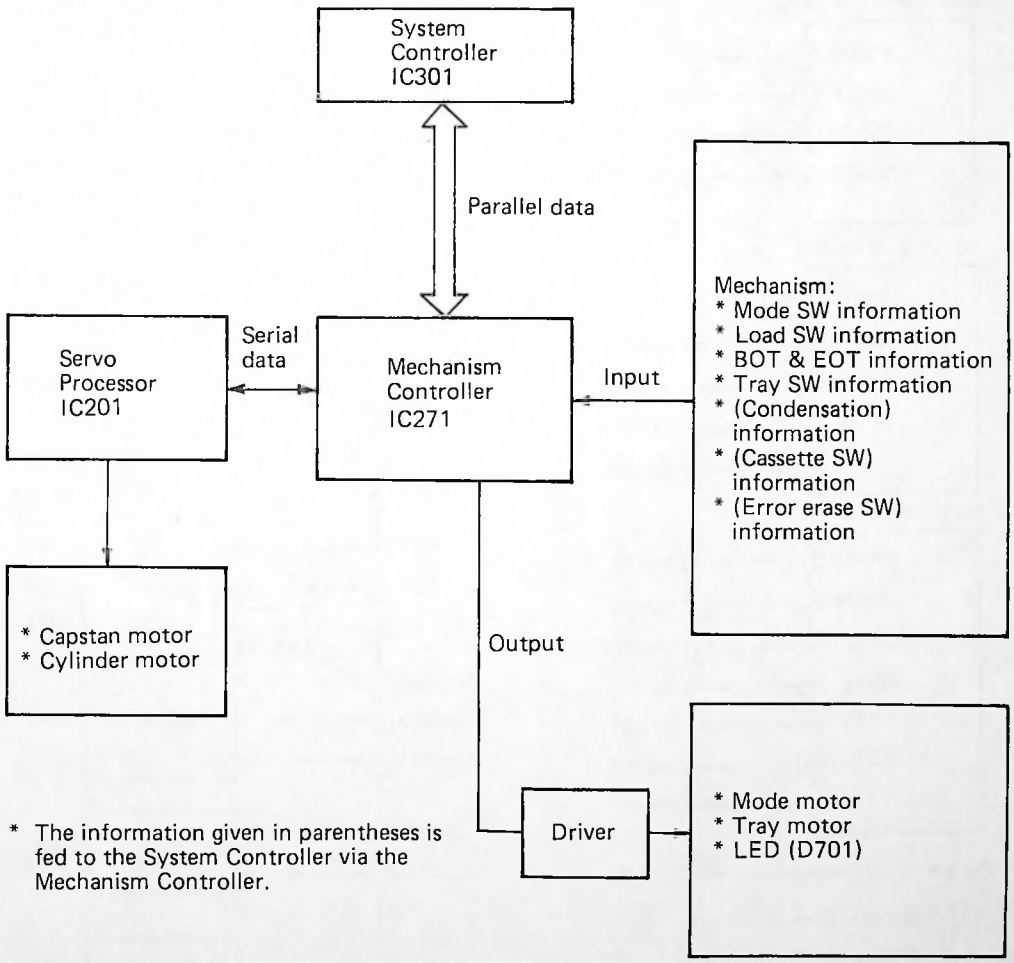


Fig. 8–1

8-2 Mechanism Control Circuit Block Diagram

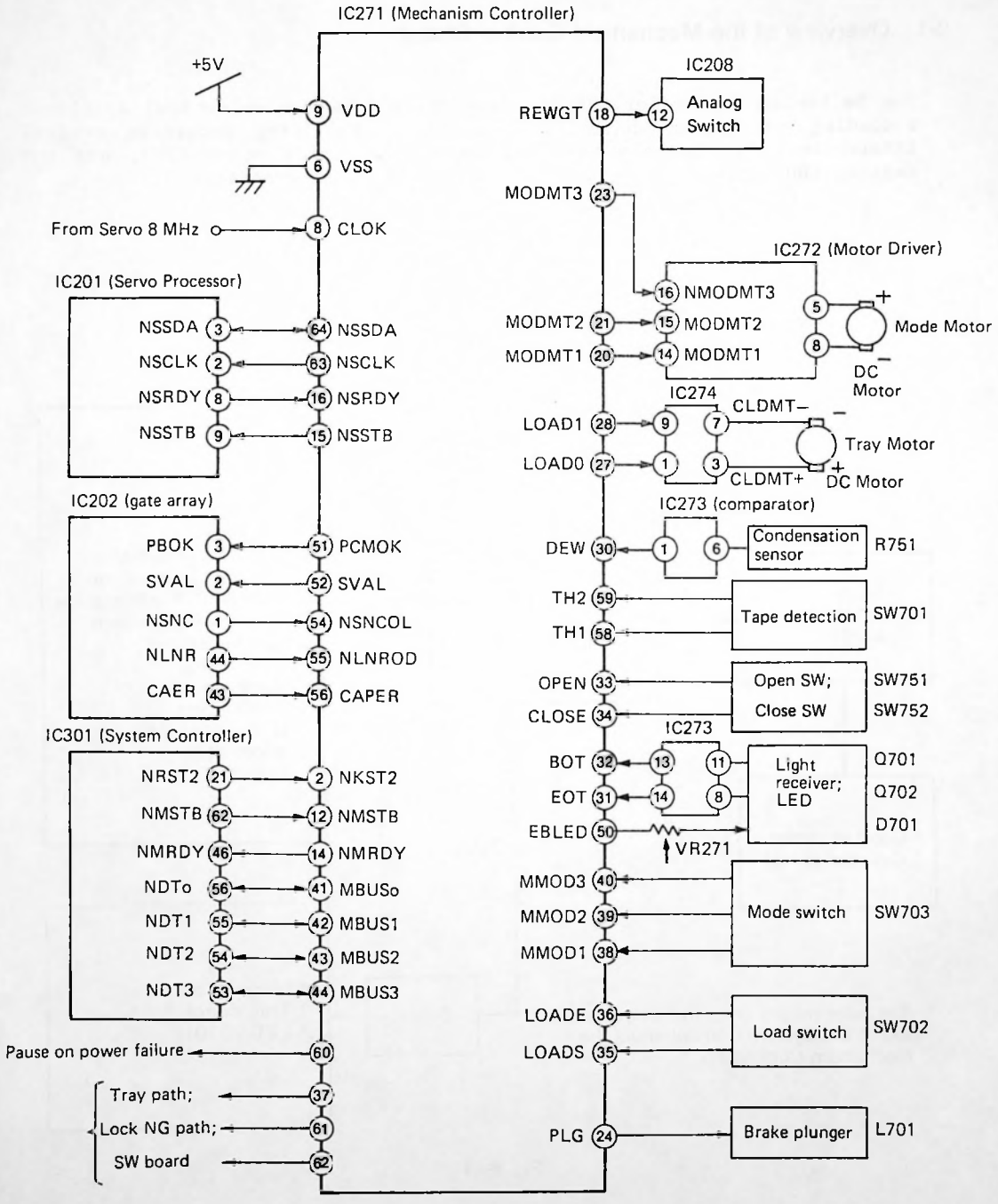


Fig 8–2

Pin Description of Mechanism Control IC271 **Table 8–1**

Pin	Pin Name	Name	Purpose
1			
2	NRST2	Reset signal	Inputs reset signal from system control
3			
4			
5			
6	VSS	Ground terminal	Connects to ground
7			
8	CLOCK	Oscillation terminal	8 MHz from servo
9	VDD	Power supply terminal	Connects to +5 V
10	DRLFGS	Supply reel FG signal	
11	DRLFGT	Take-up reel FG signal	
12	NMSTB	Strobe signal	For data transfer with system control (ready for sending)
13			
14	NMRDY	Ready signal	For data transfer with system control (ready for receiving)
15	NSSTB	Strobe signal	For data transfer with servo processor (ready for sending)
16	NSRDY	Ready signal	For data transfer with servo processor (ready for receiving)
17			
18	REWGT	REW gain select	Output
19			
20	MODMT1	Mode motor 1	Mode motor drive signal outputs (forward, reverse, brake, stop)
21	MODMT2	Mode motor 2	
22	MODMT3	Mode motor 3	
23			

Pin	Pin Name	Name	Purpose
24	PLG	Plunger signal	Brake plunger signal output, low when operating
25			
26			
27	LOAD0	Tray motor control	Tray motor drive output
28	LOAD1	Tray motor control	
29			
30	DEW	Dew detect signal	Dew sensor input signal, high when dew detected
31	EOT	EOT detect signal	End of tape sensor input signal, low when end of tape detected
32	BOT	BOT detect signal	Beginning of tape sensor input signal, low when beginning of tape detected
33	OPEN	Open switch detect	Low when open
34	CLOSE	Close switch detect	Low when closed
35	LOADE	Load switch detect	Load state detect input
36	LOADS'	Load switch detect	
37	(TORAY PASS)	For diagnostic use	Grounding permits operation without the tray
38	MMOD1	Mode switch detect	Mode state detect input
39	MMOD2	Mode switch detect	
40	MMOD3	Mode switch detect	
41	MBUS ϕ	Data bus	4-bit parallel data I/O with the system control
42	MBUS1		
43	MBUS2		
44	MBUS3		

Pin	Pin Name	Name	Purpose
45	FIL	Filter selector	Capstan FG amplifier, f characteristic selection
46			
47			
48			
49	NSRST	Reset signal	Reset signal output for servo processor
50	EBLED	LED on signal	Intermittent drive output, controls Q274
51	PCMOK	PCMOK	PCM play state monitor, low when PCM play OK
52	SVAL	SVAL signal	One/both ATF switching terminal, high for one ATF (left side)
53			
54	NSNCOK		SYNC detect state monitor, low when SYNC state OK
55	NLNROK		Play linearity monitor, low when in and out are equal OK
56	CAPER	Capstan rotational direction command	Input from the servo, counter increment or decrement, high when forward rotation
57			
58	TH1	Tape hole detect signal	Cassette detect input, high when no tape and low when tape present
59	TH2	Tape hole detect signal	Accidental erasure detect input, high when record enabled and low when record disabled
60	NPMUT	Power off pause	Loosens the tension in the mechanism when the power is turned off (pause)
61	SW2	Lock NG path	For diagnostic use, operates even during error state
62	SW1	Switch board	For diagnostic use, uses dedicated tool (switch board)

Pin	Pin Name	Name	Purpose
63	NSCLK	Serial clock	Serial transfer clock with servo processor
64	NSSDA	Serial data	Serial data I/O with servo processor

8-3 Operational Description of the Mode Switches

A 3-contact rotary switch is attached to the mode cam and performs the important function of detecting the mechanism mode. The 3-bit information, input by pins (38), (39) and (40) of IC271 as MM0D1, MM0D2 and MM0D3, informs the mechanism control of the mechanism mode.

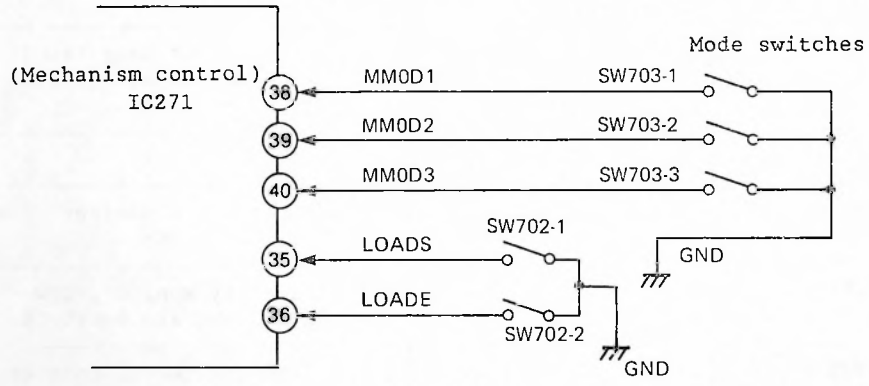


Fig. 8–3

The mode positions comprise 6 modes. The states of SW703-1, SW703-2 and SW703-3, determined by the angle of the mode cam (mode switches), are shown below.

		Mode Switch (SW703)			IC271		
Mode Name	Cam Angle	1	2	3	(38)	(39)	(40)
Load	10°	ON	ON	OFF	L	L	H
Load End	50°	ON	OFF	OFF	L	H	H
FF/REW	130°	ON	OFF	ON	L	H	L
Pause	170°	OFF	OFF	ON	H	H	L
Play	250°	OFF	ON	ON	H	L	L
Review	310°	OFF	ON	OFF	H	L	H

Table 8–2

8-4 Operational Description of the Mode Motor Drive

The mode motor drive switches the operation of the mechanism.
Driver IC272 has 3 input pins and 2 output pins, and controls the 4 modes of brake, stop, forward rotation and reverse rotation.

The mode at power on is set to the brake mode since the mechanism may otherwise malfunction as the mode motor rotates when the power is turned on.

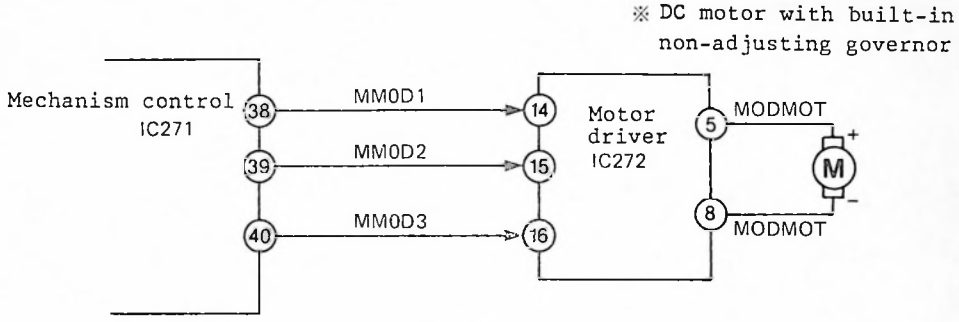


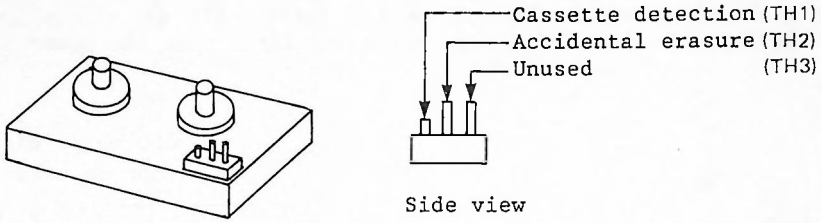
Fig. 8–4

	IC271			IC272			Motor	
	㊳	㊴	㊵	⑭	⑮	⑯	⑤	⑧
Brake	H	H	L	L	H	L	H	H
Stop	L	L	L	L	L	L	-	-
Forward Rotation	L	L	H	H	L	H	H	L
Reverse Rotation	L	H	L	L	H	L	L	H

Table 8–3

8-5 Operational Description of the Cassette Tape Information Detection

The cassette tape information detection is performed by switches which detect holes on the cassette. The information is input by pins (58) and (59) of mechanism control IC271.



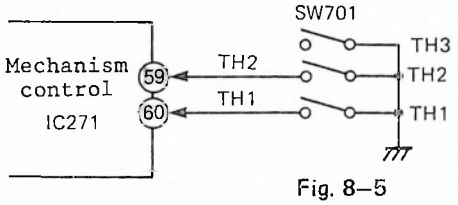


Fig. 8–5

	SW701	IC271	
TH1 cassette detection	ON	(60) L	Tape present
	OFF	(60) H	No tape
TH2 accidental erasure	ON	(59) L	Record disabled
	OFF	(59) H	Record enabled

Table 8–4

8-6 Operational Description of the Brake Plunger

During mode transition from FF/REW to the stop operation, current is supplied to the plunger and the take-up and supply brake levers are held. FF/REW is performed in the brake off state, the plunger is released simultaneously with the stop command and the brake is applied to the S/T reel.

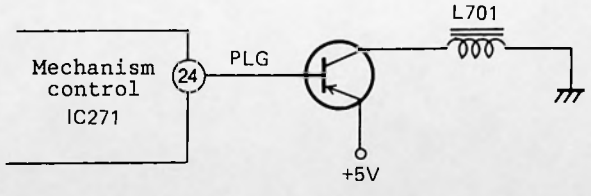


Fig. 8–6

When pin (24) of IC271 is low, the plunger is actuated.
When pin (24) of IC271 is high during stop, the plunger is released.

8-7 Operational Description of the Load Switches

The 2-contact rotary switch (SW702) attached to the load cam detects the load state of the mechanism which is input by pins (35) and (36) of mechanism control IC271 as LOADS and LOADE.

	SW702		IC271		Remark
Loading position	1	2	(35) LOADS	(36) LOADE	
Load (loading completed position)	ON	ON	L	L	LOADS and LOADE both high during loading
Tape slack	OFF	ON	H	L	
Unload (unloading completed position)	OFF	ON	H	L	
Normal operation	ON	ON	L	L	

Table 8–5

* Normal operation: Play, review, FF/REW, pause, stop

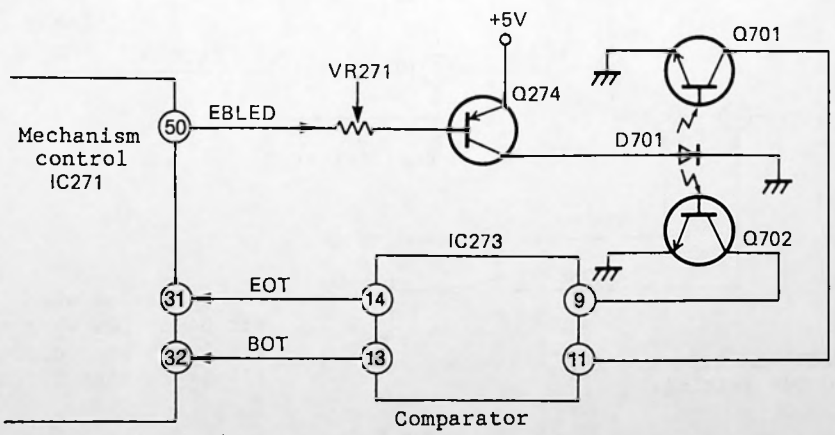
8-8 Operational Description of Beginning and End of Tape Detection

A lighthouse LED (D701) is used at the center of the mechanism and emits light in both directions. Two light sensors (beginning and end) detect the transmitted light for the leader and magnetic portions of the tape.

The LED is driven intermittently by the EBLED signal which is output from pin (50) of mechanism control IC271. The mechanism control reads the signal for the BOT and EOT using the timing of the LED lighting. The information is then sent to the system control.

BOT = Beginning Of Tape
EOT = End Of Tape

VR271 is a variable resistor used to adjust the LED light intensity. (It is necessary to check the light intensity when D701, Q701 and Q702 are replaced.) Check that the tape is stopped at the leader portion of the DAT tape.



Pin (32) is low at the beginning.
Pin (31) is low at the end.

Fig. 8–7

8-9 Operational Description of Condensation Detection

A dew sensor is attached to the left front side of the tray and its resistance rises when the humidity increases. This change passes comparator IC273, is input by pin (30) of mechanism control IC271, and sent to the system control as information. Since this unit does not contain a heater, "dew" is displayed until pin (30) of IC271 goes low as a result of the unit's heat. At this time, the mechanism is in the unload state, the cylinder rotation is stopped and the mechanism's keys do not accept any inputs.

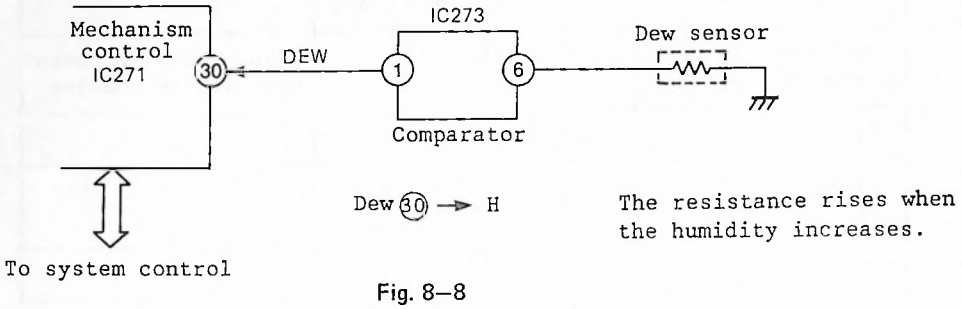


Fig. 8–8

8-10 Operational Description of Tray State Detection and Tray Motor

The open switch (SW751) and close switch (SW752) detect the tray state from the tray cam for the cassette tray.

As the OPEN/CLOSE button is pressed, a command signal is sent from the panel control to the system control and then to the mechanism control. The tray motor drive signals LOAD0 from pin (27) and LOAD1 from pin (28) of IC271 are input by pins (1) and (9) of IC274 and its outputs are fed to both terminals of the tray motor as CLDMT+ and CLDMT-.

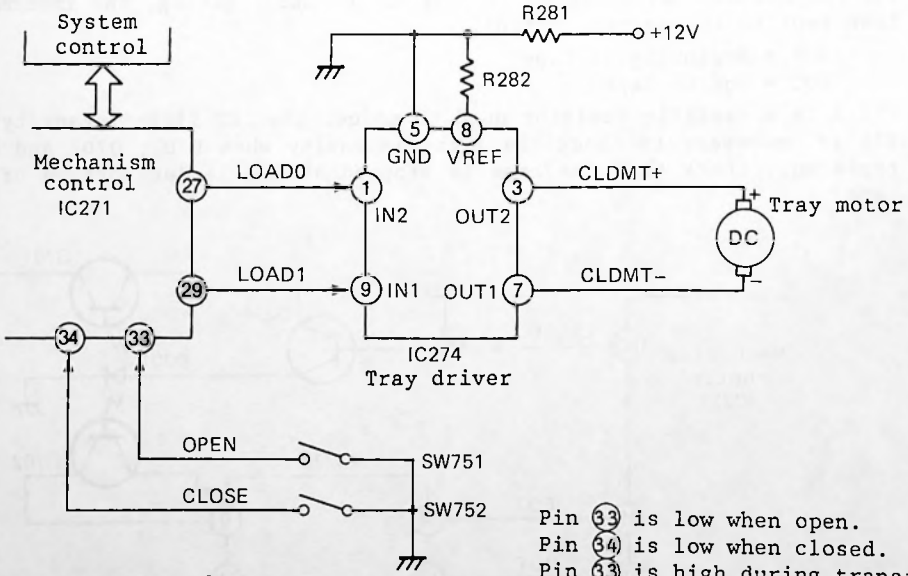


Fig. 8–9

8-11 Data Transfer Between the Mechanism Control and Servo Processor

The transfer of signals between the mechanism control and servo processor exchanges information used to perform mechanism drive.

The data transfers consist of NSSTB (ready for sending), NSRDY (ready for receiving), NSCLK (transfer clock) and NSSDA (serial data). The data consists of 16 serial bits.

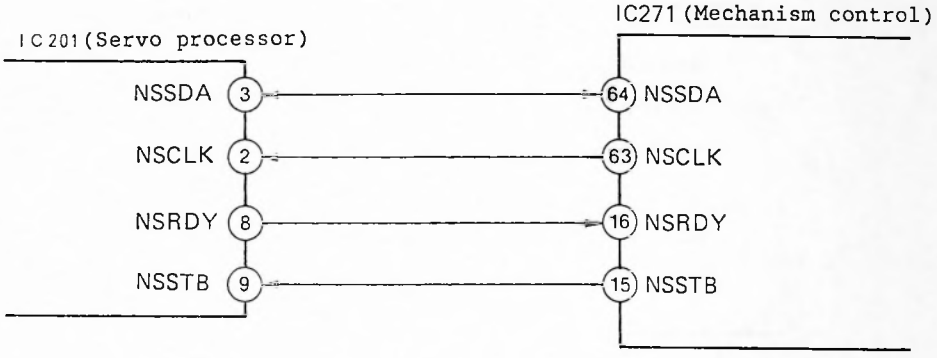


Fig. 8–10

Serial Data Contents

Data consisting of 16 bits is exchanged between the mechanism control and servo processor. The major contents are given below.

No.	Mechanism Control to Servo	No.	Servo to Mechanism Control
1	-	1	-
2	-	2	-
3	Track pitch, 1 and 1.5	3	Speed command from the servo
4	ATF ON, OFF (PLAY - ON)	4	
5	Capstan torque setting High, low	5	
6		6	
7	-	7	
8	Cylinder, start, stop - 0	8	
9	Rapid brake (for capstan)	9	Checking of rapid brake
10	-	10	-
11	Capstan rotational direction Forward - 1	11	-
12	Reel servo, capstan servo	12	Whether the speed is OK in reel mode
13	Speed command	13	-
14		14	Whether the cylinder rotational speed is OK
15		15	Whether the capstan rotational speed is OK
16		16	End of tape proximity speed

Table 8–6

8-12 Data Transfer Between the Mechanism Control and System Control

The transfer of data signals between the mechanism control and system control is performed in 4 parallel bits using pins 41 to 44 (MBUSφ to MBUS3) of IC271.

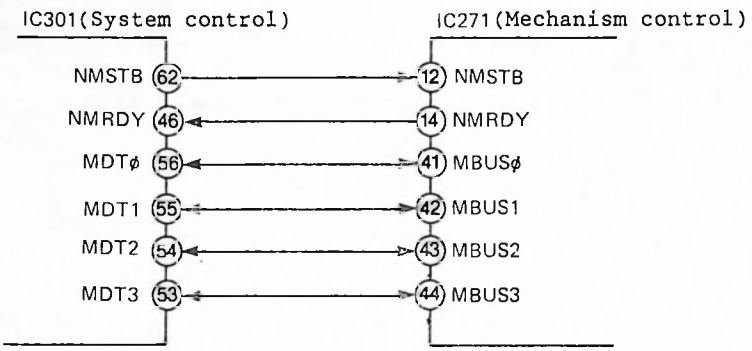


Fig. 8–11

Parallel Data Contents

Mechanism Control to System Control	System Control to Mechanism Control
Current mode information Current speed information Tape begin-end information Dew information Mechanism lock information Tray information Accidental erasure information Cassette detect information Reel counter information Error information	Mode command Speed command Final speed command Track pitch signal Counter reset signal SPE MASK signal.

Table 8–7

8-13 Error Rate and Error Code Display Function

The error rates for the A and B heads, and the various error codes are shown on the FL display when certain buttons are pressed while servicing the SV-DA10.

* This is very useful when checking the unit during servicing.

<Display Method>

Simultaneously press the [Counter Mode] key, [Counter Reset] key and [Pause] key.

(1) The error rates for the A and B heads are displayed. (FL A and B illuminate)
Successively pressing the [Counter Mode] key performs the error displays in (2) to (5).

(2) Displays the error rate for the A head (FL [A] illuminates).

(3) Unused

(4) Displays the error code for the system control and mechanism control.
* The error codes are described separately.

Press the [Counter Reset] key to return to the normal mode.

* The display changes to the A-time (absolute time) mode.

8-14 About the Error Rate

The number appearing on the display in the error rate display mode represents the number of blocks that could not be read during approximately one second.

Actually, 39 frames are played, and the number of C1 flags generated during that time are counted and displayed.

39 frames/33.3 Hz = 1.17 second
Total number of blocks = 9984 (128 blocks x 2 channels x 39 frames)

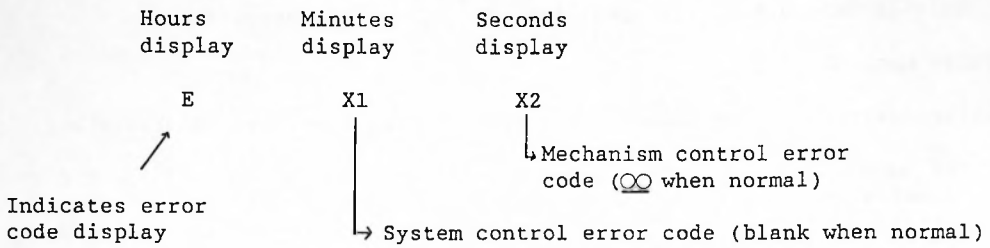
Troubleshooting can be performed from the value of the error rate that is displayed when the sound skips or when click noises are heard during the playback of a music tape.

Error Rate	Cause
0-1000	It can be assumed there is no problem with the mechanism, head and tape. Check the amplifier circuit.
1000-5000	Head cleaning is necessary. Check the envelope.
5000-9984	Dirty or disconnected head. Check the envelope.

* The error rate reaches approximately 5000 when one head becomes disconnected.
* The maximum value for the error rate display mode for A head is 4992. If there is a problem at either drive A or B, it can be determined in this mode.
* When the error rate exceeds 1000, the cleaning lamp on the display turns on.

8-15 Description of the Error Code Table

Error codes are shown on the FL display tube according to the method described previously.



Error Code (X1) (X2)	System Control Error Code		Mechanism Control Error Code	
	Process	Description	Process	Description
1	Temporary operation	R3CP clock error	Unload	Mechanism mode transfer lock
2	Temporary operation	HSW clock error	Unload	Tape loading lock
3	Transfer omitted	Mechanism control transfer error	Unload	Capstan, unlock
4	Unload	Still protective operation (normal operation)	Unload	Cylinder unlock
5	Unload	Tape cut	Unload	Reel, unlock
6	Unload	SP1 transfer error	Unload	Reel period sum measurement disable
7			Unload	In cassette rew time over
8			Unload	Slack take-up time over
9			Unload	Tape jamming (supply side)
A			Unload	Tape jamming (take-up side)
-			Unload	Rotation gear

Table 8–8

Process During Error Generation

- Temporary operation:
  Operation is temporarily continued with the system control internal clock.
- Transfer omitted:
  Transfer process is terminated.
- Unload:
  Tape is placed in the unload mode.

Mechanism mode transfer lock:
  Mode switch does not switch, mode motor does not rotate.
Tape loading lock:
  Load switch does not switch, capstan motor does not rotate.
Capstan unlock:
  Capstan speed does not lock.
Cylinder unlock:
  Cylinder speed does not lock.
Reel unlock:
  Reel FG speed does not match (during FF/REW operation).
Reel period sum measurement disable:
  Speed cannot be measured at x12.5 speed (during FF/REW operation).
In cassette rew time over:
  Rew time exceeds the standard time.
Slack take-up time over:
  Slack take-up exceeds the standard time.
Tape jamming (supply side):
  Supply-side reel locks.
Tape jamming (take-up side):
  Take-up-side reel locks.

– MEMO –

9. Mechanism

9-1 Features and Overview of the Mechanism

9-2 Mechanism Parts Layout

9-3 Name and Description of Each Part

9-4 Name and Function of Each Gear

9-5 Operational Description of the Mechanism

9-6 Mechanism Operation of Each Part

1) Operation of the S Brake and T Brake
2) Operation of the P Idler Gear and F Idler Gear
3) Operation of the Load Gear Train
4) Operation of the Tension Regulator
5) Operation of the Supply Reel Back Tension
6) Operation of the Pinch Roller

9-7 Detection of Mechanism Operation

9. Mechanism

9-1 Features and Overview of the Mechanism

The DAT employs a newly-developed mechanism measuring 93.5 (H) x 80 (W) x 29.5 (D) mm and weighing 180 grams.
The mechanism employs a cylinder with a diameter of 30 mm, M loading with a 90° wrapping angle, dual-head helical scan, and amorphous MIG heads (MIG: metal-in gap; base material is ferrite with amorphous gap portion).

The tape driving mechanism uses three motors (cylinder (DD) motor, capstan (DD) motor, and mode (DC) motor). The capstan motor also loads the tape loading and drives the reel.
The mechanism uses no belt; all driving is accomplished through gear arrays.
The mechanism has the following six basic modes:

1. Load
2. Load End
3. FF/REW
4. Pause
5. Play
6. Review

A brake plunger is used in the mechanism. In the FF/REW mode, the brake is activated by the plunger to enter the pause mode. In Stop mode, the plunger is de-energized to release the brake.

For BOT and EOT detection, a beacon LED is used in the center of the mechanism to emit light on both sides, which is picked up by the BOT and EOT sensors in the leading and trailing portion of the tape.

Cassette detection is accomplished by a contact switch. The switch only detects the presence of a cassette and its erasure prevention tab. The SV-DA10 uses no switch to detect cassette tape material and thickness as employed in the preceding model.

The mechanism uses two rotary switches, mode and load switches, which detect the mode and tape-loading state, respectively.

The mode switch is driven by the mode motor via a mode cam to identify the Forward, Reverse, Brake, and Stop modes.

The load switch is driven by the capstan motor via a load cam.

FG signals are detected as follows:

(1) Cylinder FG: Detected by an integration coil for total gap circum-ference (40 pulses per rotation).
(2) Capstan FG: Detected by an MR device (290 pulses per rotation).
MR device: Magnetic register which varies its resistance with the magnetic field strength.
(3) Reel FG: Detected optically (64 pulses per rotation).

9-2 Mechanism Parts Layout

1) Top View

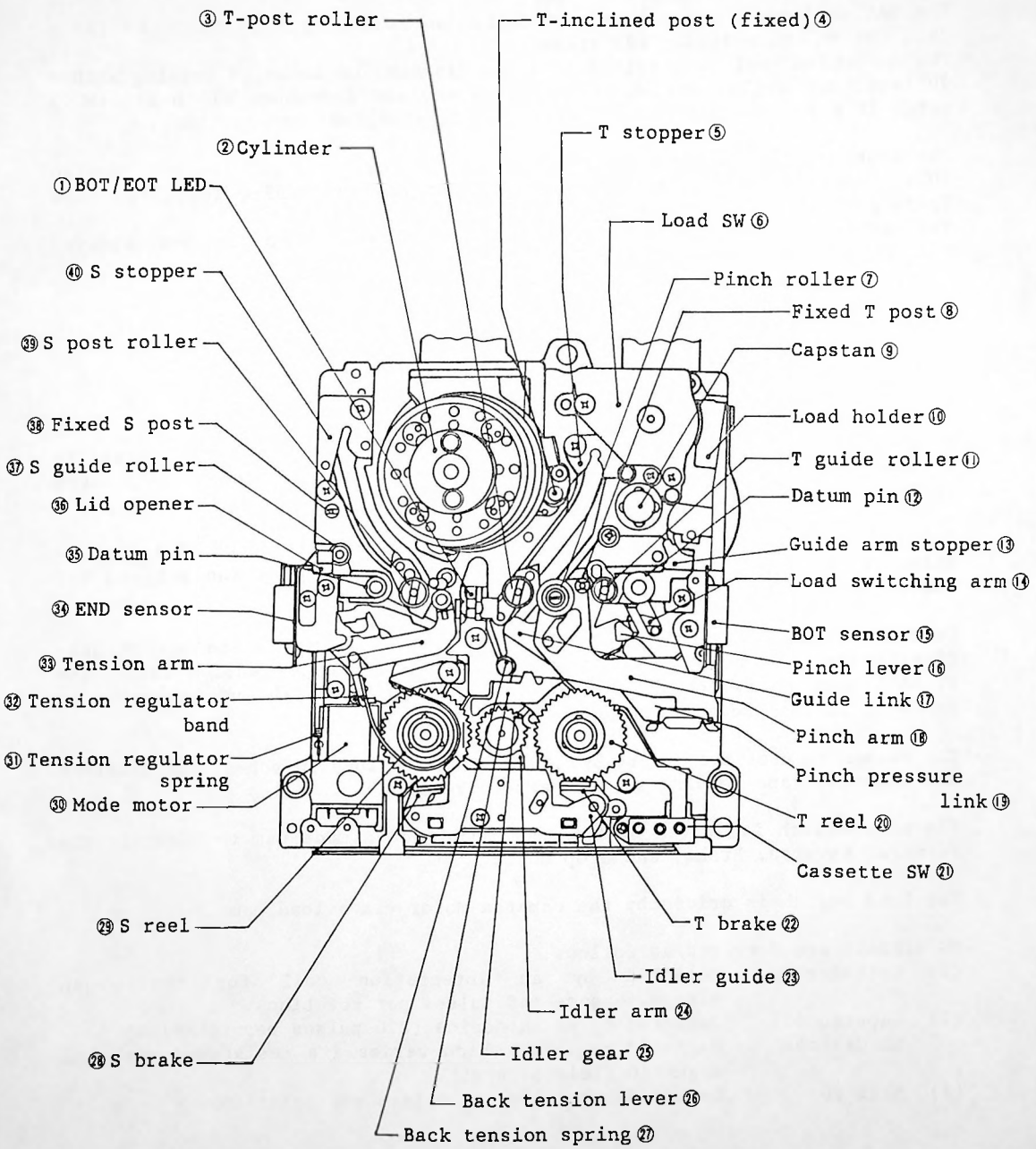


Fig. 9–1

2) Side and Bottom Views

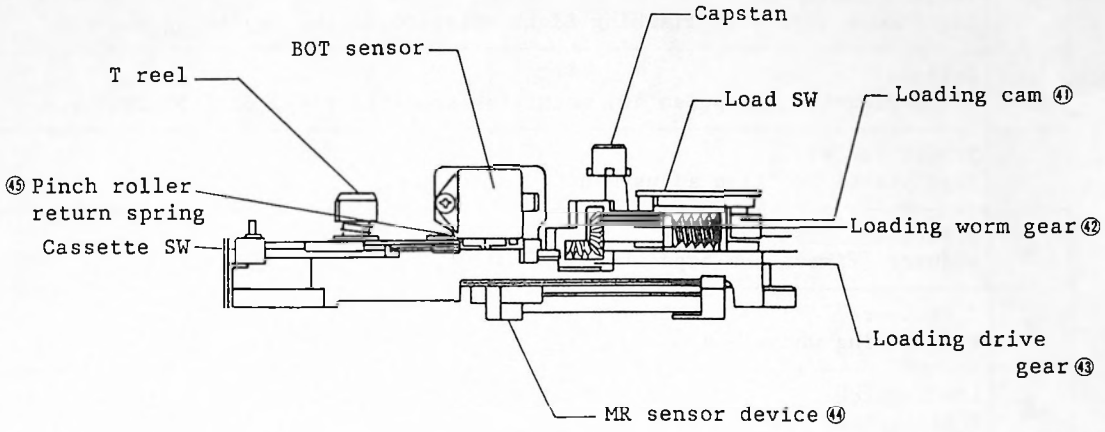


Fig. 9–2

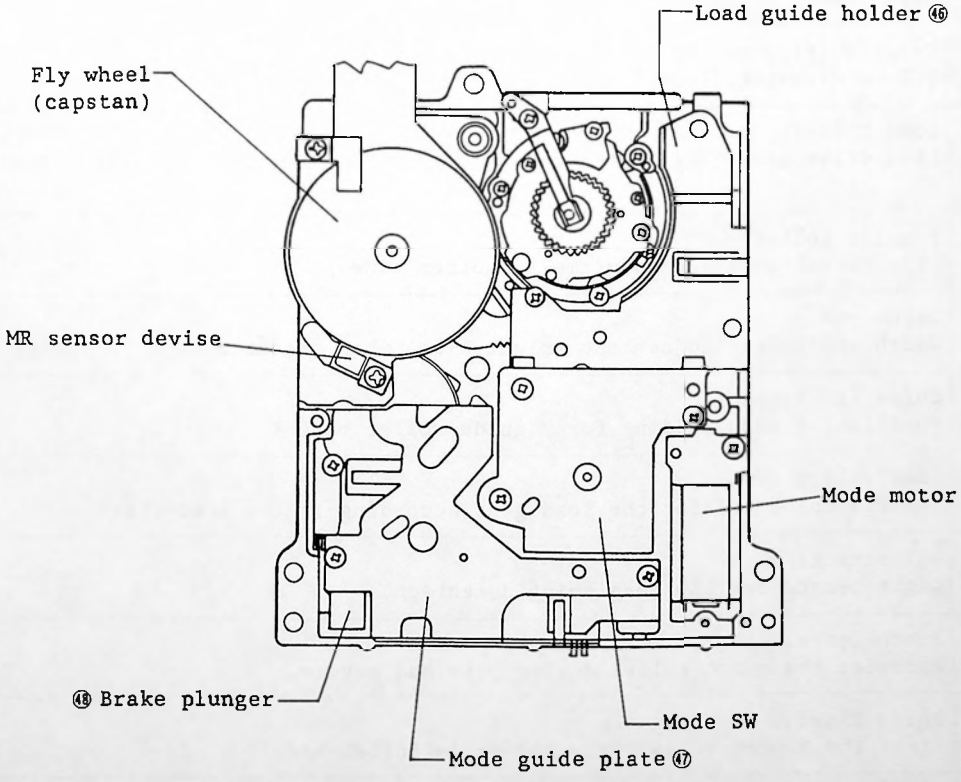


Fig. 9–3

9-3 Name and Description of Each Part

①	BOT/EOT LED: Lighthouse type with flashing light emission at the beginning and end
②	Cylinder: 30 mm diameter, FG pulse 40, maintains specific speed of 1000-3000 rpm
③	T post roller: Tape travel position adjustment (top side)
④	T inclined post: Adjusts (fixed) the tape wrap angle (90°) onto the cylinder
⑤	T stopper: Positioning when loading for the T post roller base
⑥	Load switch: 2-bit rotary switch, load position detection
⑦	Pinch roller: Actuated during play and review
⑧	Fixed T post: Tape travel adjustment
⑨	Capstan (flywheel N): 1.5 mm diameter, FG pulse 290
⑩	Load holder: Load drive gear, built-in worm gear, contact or break down with M gear A
⑪	T guide roller: Tape travel position adjustment (bottom side)
⑫	Datum pin: Width and height adjustment (right side) when cassette tape is loaded
⑬	Guide arm stopper: Positioning when loading for T guide roller base K
⑭	Load select lever: Selects on or off for the load gear according to the load state
⑮	BOT sensor: Light sensor for LED (beginning detection)
⑯	Pinch lever: Actuates the pinch roller during play and review
⑰	Guide link: Links the T post roller base and guide roller base
⑱	Pinch arm: Consists of pinch roller and T fixed post, applies pressure to capstan

⑲	Pin pressure link: Connected with pinch arm and pin pressure spring
⑳	T reel: Take-up reel, FG pulse 64
㉑	Cassette switch: Detection of cassette information (accidental erasure, cassette detection)
㉒	T brake: Brake actuated by brake shoe pressure against the reel gear
㉓	Idler guide: Idler arm, S and T brake pressure cover
㉔	Idler arm: Moves to the left and right according to the mode, transfer of counter gear to the S and T reels
㉕	Idler gear: Transfer to the S reel or T reel according to the mode
㉖	BT lever: Applies back tension to the T reel during review
㉗	BT spring: Applies pressure for back tension lever
㉘	S brake: Brake actuated by brake shoe pressure against the S reel gear
㉙	S reel: Supply reel, FG pulse 64
㉚	Mode motor: 6.5 V, DC motor, mode switching with forward rotation and reverse rotation
㉛	Tension regulator spring: Source of back tension force of tension regulator
㉜	Tension regulator band: Attached to tension regulator and applies back tension to the S reel
㉜	Tension arm: Detects the state of the tape and applies back tension during play and review
㉝	End sensor: Light sensor for LED (end detection)
㉞	Datum pin: Width and height adjustment (left side) when cassette tape is loaded
㊱	Lid opener: Opens the cassette lid when tape is loaded

㊲	S guide roller: Tape travel position adjustment (bottom side)
㊳	Fixed S post: Tape travel adjustment (bottom side)
㊴	S post roller: Tape travel position adjustment (top side)
㊵	S stopper: Positioning when loading for the S post roller base
㊶	Load cam: Moves the load lever from transfer of load worm
㊷	Load worm: Performs transfer with the load drive gear and load cam
㊸	Load drive gear: Transfer of M gear A and load worm, on or off according to mode
㊹	MR sensor device: Detects the change in magnetic intensity (290 pulses) of the flywheel's side
㊺	Pinch roller return spring: Attached to the pinch arm and returns the pinch roller
㊻	Load guide holder: Load arm, load lever pressure cover
㊼	Mode guide plate: Pressure cover for various gears, plunger hold
㊽	Brake plunger: 5 V, 200 mA, turns the brake on or off according to the mode

* MR (magnetoresistor) device: Device which performs FG detection, its resistance changes according the change in magnetic intensity

9-4 Name and Function of Each Gear

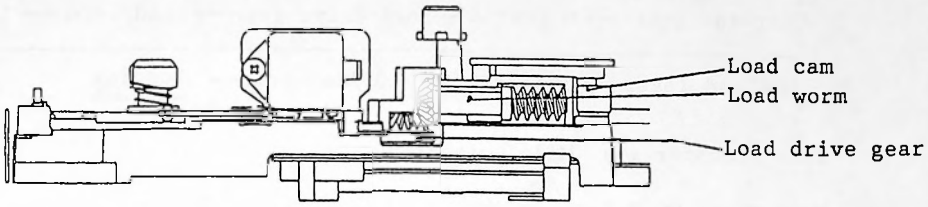


Fig. 9–4

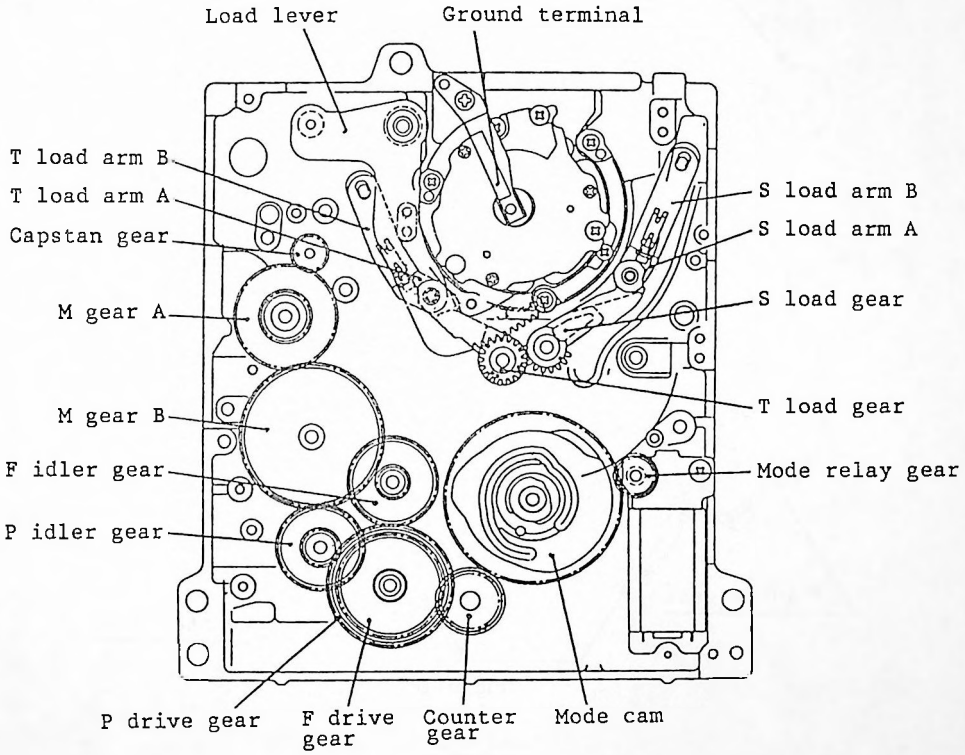
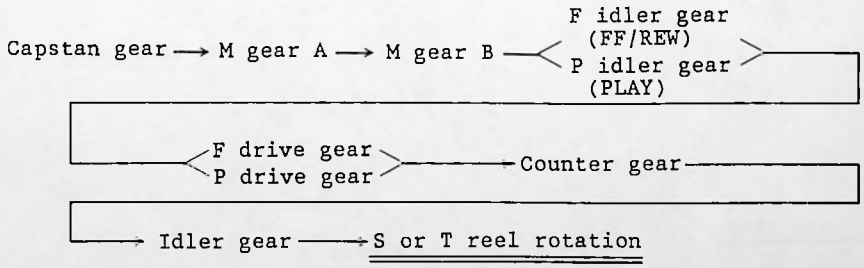


Fig. 9–5

Gear Transfer (1) Reel Drive



Gear Transfer (2) Loading

○ Capstan gear → M gear A → Load drive gear → Load worm → Load cam → Load lever → T load gear → S load gear → Loading

Gear Transfer (3) Mode Switching

Mode motor worm gear → Mode relay gear → Mode cam

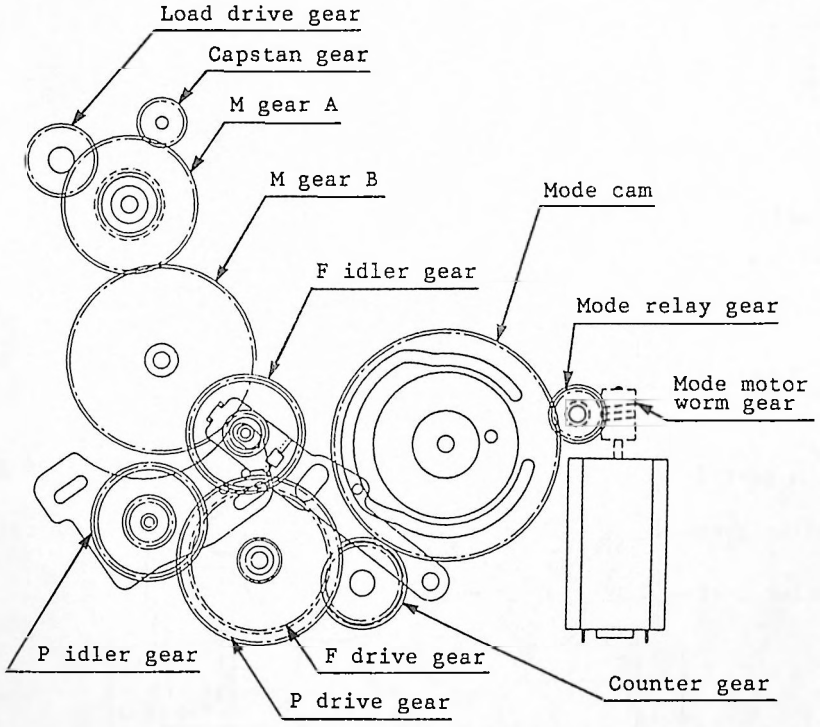


Fig. 9–6

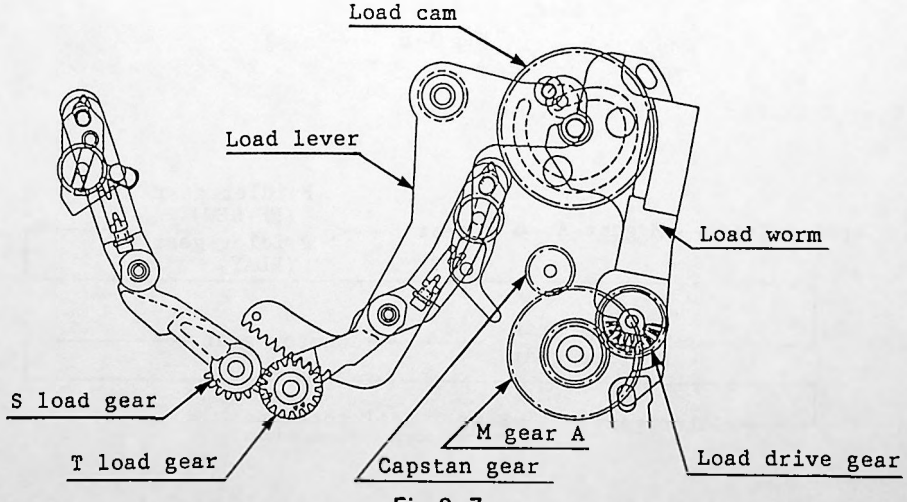


Fig. 9–7

9-5 Operational Description of the Mechanism

The 6 modes given below represent the basic modes of the mechanism.

1. Load
2. Load end
3. FF/REW
4. Pause
5. Play
6. Review

All mechanism operations can be controlled by the switching of these 6 modes.

Mode switching is driven by the capstan motor and mode motor. Both motors are precisely interrelated to perform mode transition.

The mode position is detected by the rotary contact mode switch. This switch is attached to the mode cam and has 6 positions (modes), where various operations are performed, in the rotation (10° to 310°) of the mode cam.
Load 10°, load end 50°, FF/REW 130°, pause 170°, play 250°, review 310°

* The load position is detected by the rotary contact load switch attached to the load cam.

The rotation of the mode cam switches the operation of the parts below with the grooves provided on the front and rear surfaces of the cam.

1. Supply reel brake
2. Take-up reel brake
3. P idler and F idler
4. Load drive gear
5. Tension regulator
6. Take-up real back tension
7. Pinch roller pressure

Operation of Mode Cam

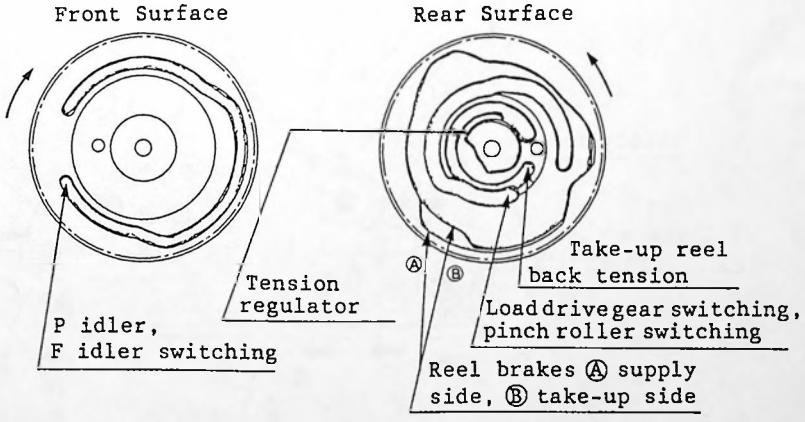


Fig. 9–8

* The arrows show the start positions.
* The brake cam is divided into two parts: upper and lower.

9-6 Mechanism Operation of Each Part

1) Operation of the S Brake and T Brake

There are 3 patterns of operation:
(1) S brake off, T brake on
(2) S brake off, T brake off
(3) S brake on, T brake on

Their respective operating states are:
(1) Load, unload, slack take up
(2) Play, review, FF/REW, end of tape rewind
(3) Stop, pause
In the operation from FF/REW to stop, the brake plunger which maintains the off state of the S and T brakes is released simultaneously with the stop operation and the brakes are rapidly applied.

The outer shape of the mode cam switches the S and T brakes on and off. The S brake is off and the T brake is on at the portion where the cam shape is divided into 2 levels, upper and lower. Otherwise, the S and T brakes are both switched simultaneously on or off.

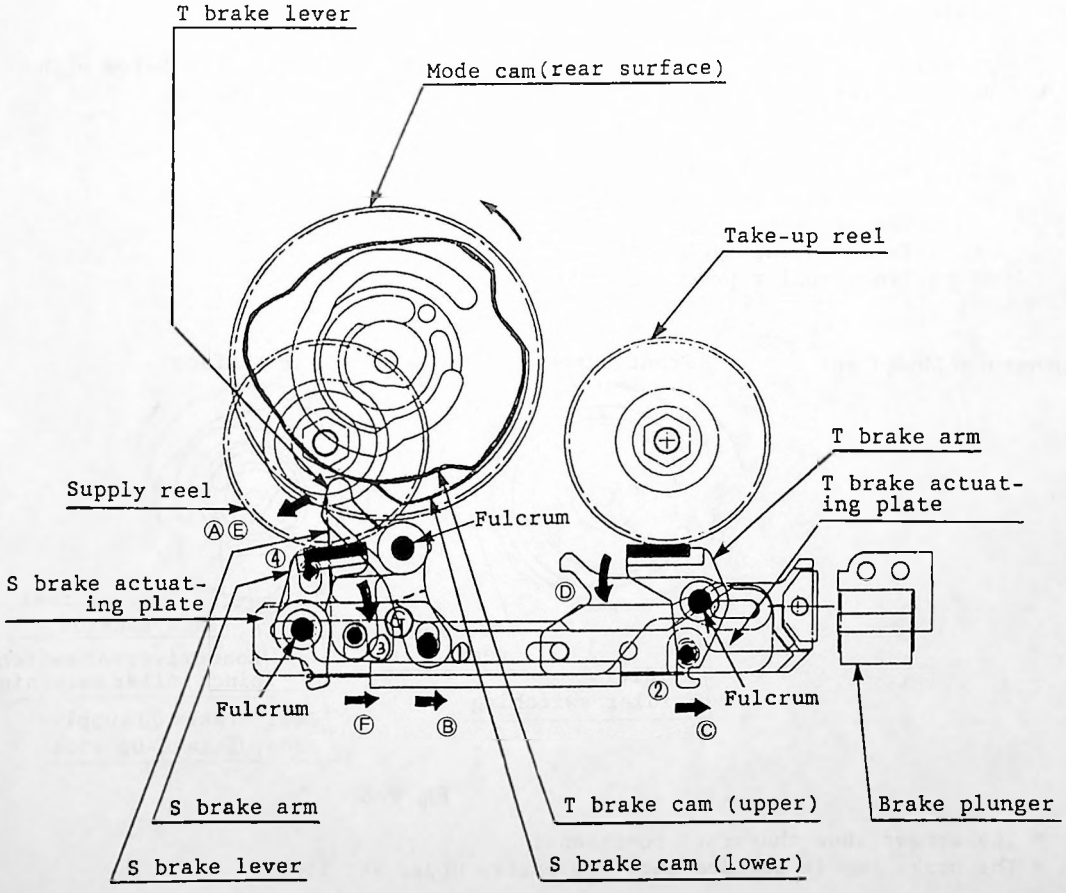


Fig. 9–9

Operation of the T Brake (brake on to off)

Rotation of the mode cam → T brake lever ↙ Ⓐ direction → Pin ① → Ⓑ direction → T brake actuating plate, pin ② → Ⓒ direction → T brake arm ↙ Ⓓ direction

Operation of the S Brake (brake on to off)

Rotation of the mode cam → S brake lever ↙ Ⓔ direction → Pin ③ → Ⓕ direction → S brake actuating plate, pin ④ → S brake arm ↘ Ⓖ direction

Supply Reel, Take-up Reel and Brake Operation

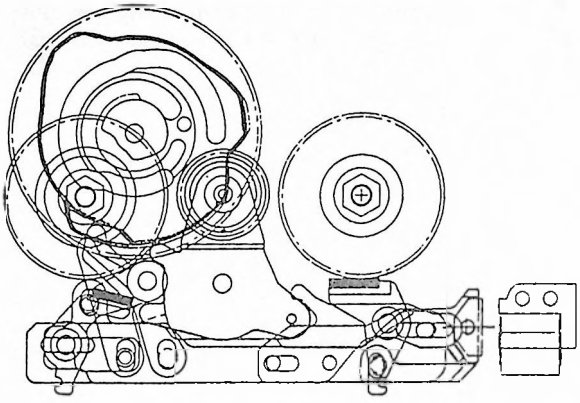


Fig. 9–10

S brake off, T brake on
* Load
* Unload
* Slack take up

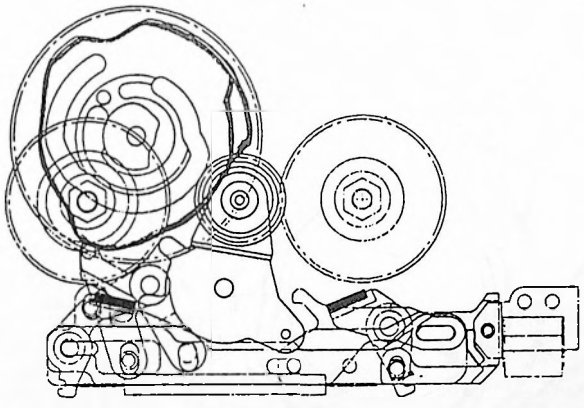


Fig. 9–11

S brake off, T brake off
* Play
* Review
* FF/REW
* End of tape rewind

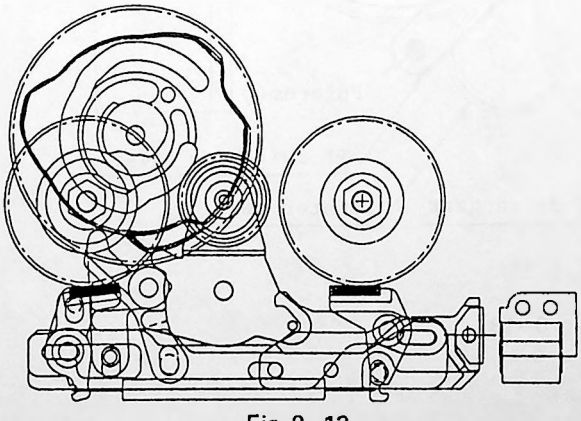


Fig. 9–12

S brake on, T brake on
* Stop
* Pause

2) Operation of the P Idler Gear and F Idler Gear

The F idler gear is used in FF/REW and pause. The P idler gear is used in the other modes (play, review, load, unload).

When the P idler and F idler switch during mode transition, the capstan motor rotates slightly in the forward and reverse directions and the timing operation is performed during switching so that the gear teeth engage smoothly.

Switching Operation of the P Idler Gear to F Idler Gear

Mode relay gear → mode cam ↗ Ⓐ direction → pin ① centering on PF switching lever fulcrum ②, ↙ Ⓑ direction → PF idler arm, pin ③ ↙ Ⓒ direction → F idler engages with M gear B.

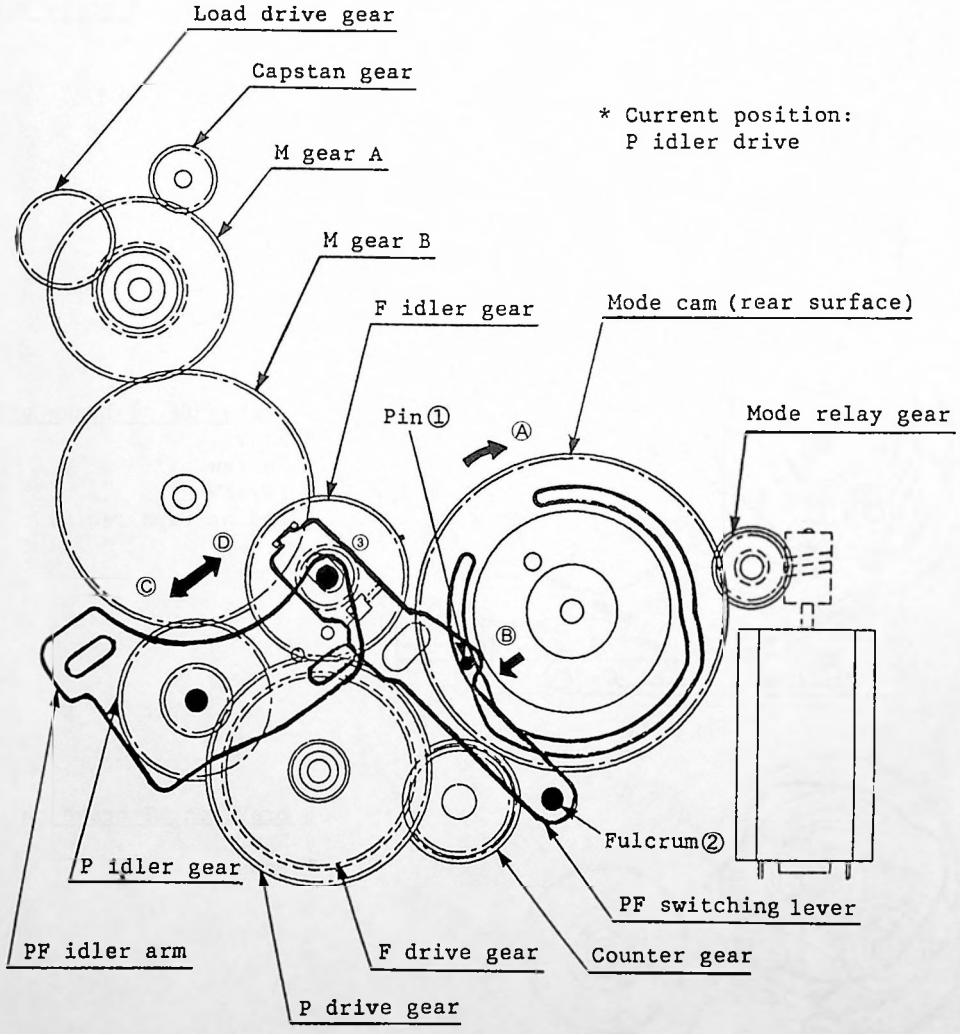


Fig. 9–13

3) Operation of the Load Gear Train

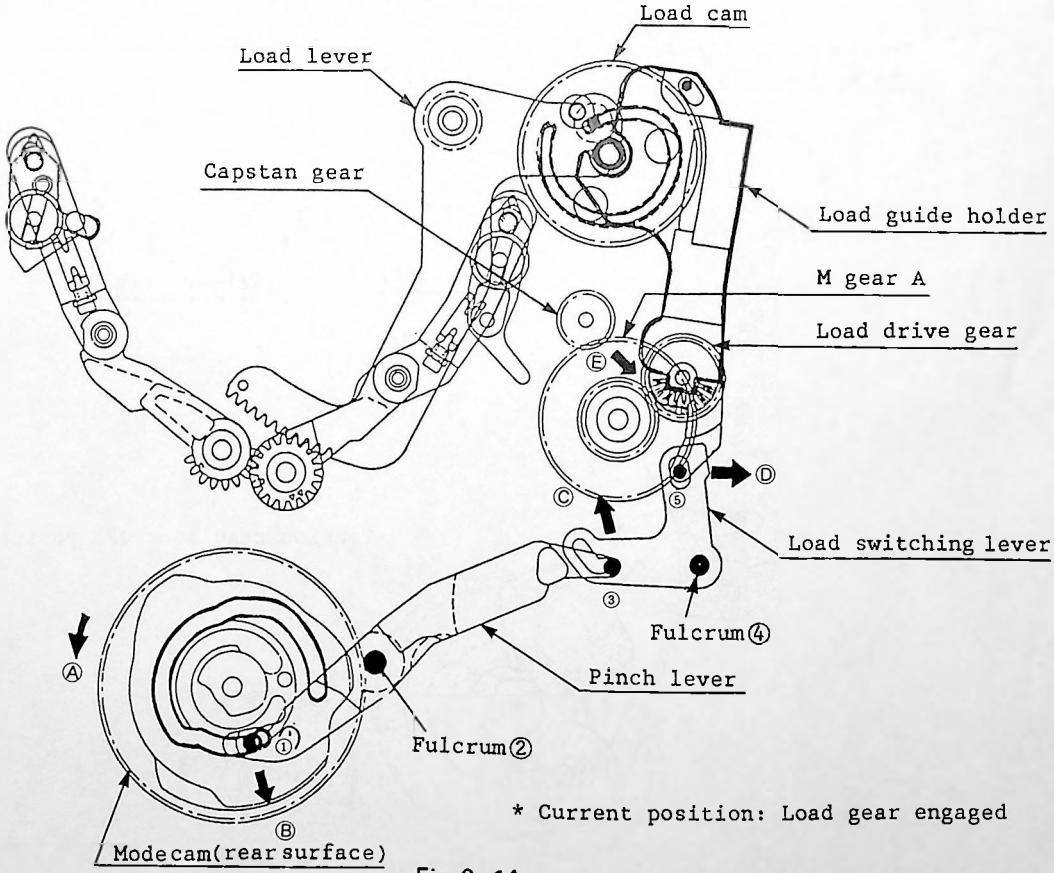
The pin of the pinch lever enters the mode cam's groove and the rotation of the mode cam rotates the pinch lever. The movement of the load switching lever moves the load guide holder.
The load drive gear installed in the load guide holder also moves to engage or disengage the gear transfer with the M gear A.
There are 2 patterns of operation.

(1) Load drive gear is engaged with the M gear A
Capstan motor rotates the load drive gear to perform loading and unloading.

(2) Load drive gear does not engage with the M gear A
This operation is always performed except when loading.

Engage Load Drive Gear to Disengage Load Drive Gear

Mode cam ↙ Ⓐ direction → pinch lever, pin ① ↓ Ⓑ direction
→ pinch lever pin ③ centering on fulcrum ② ↖ Ⓒ direction
→ centering on load switching lever fulcrum ④ → Ⓓ direction
→ load drive gear, pin ⑤ ⇨ Ⓓ direction → ↘ Ⓔ point M gear A and load drive gear disengage



* Current position: Load gear engaged

Fig. 9–14

4) Operation of the Tension Regulator

The mode cam rotates the tension regulator lever and tension arm, and the tension regulator band applies back tension to the supply reel. The tension regulator is on during play and review.

Operation of the Tension Regulator from On to Off

Mode cam ↘ Ⓐ direction → ↙ Ⓑ portion of cam moves the tension regulator lever → tension regulator lever centering on fulcrum ① ↗ Ⓒ direction tension regulator band loosens → tension arm ↘ Ⓓ direction → tension regulator off

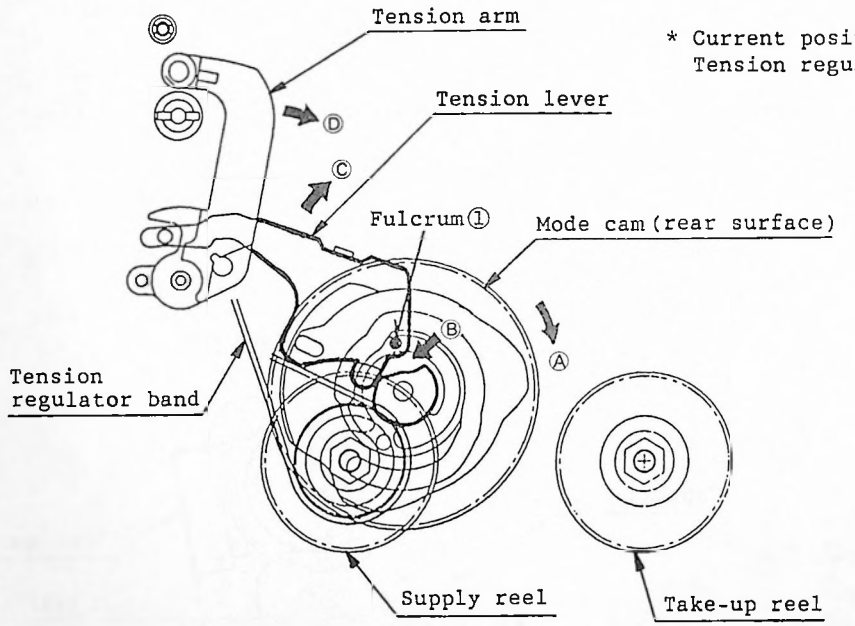


Fig. 9–15

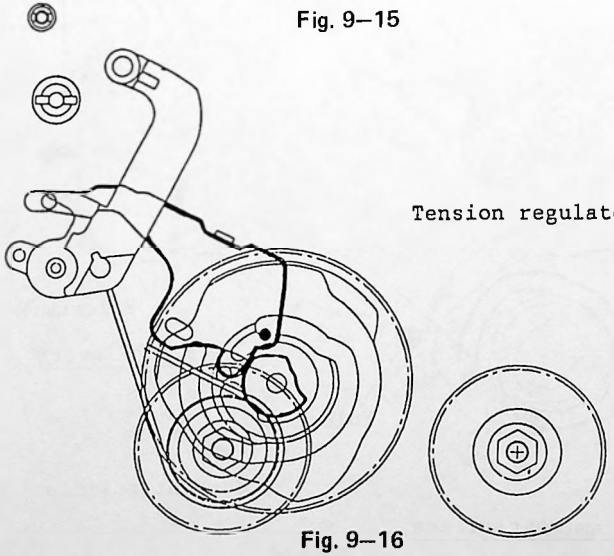


Fig. 9–16

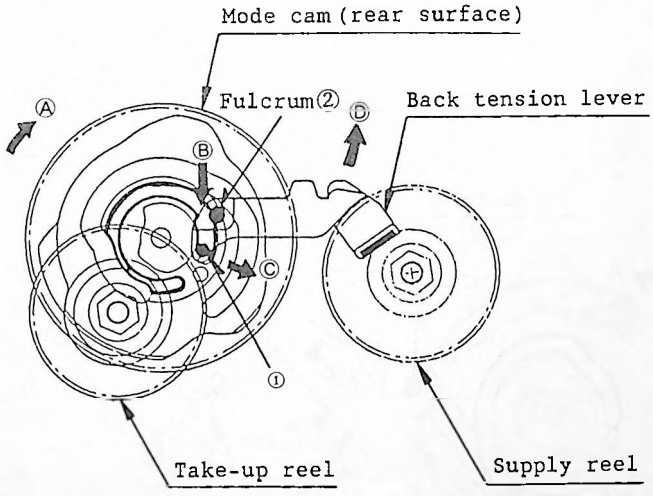
5) Operation of the Supply Reel Back Tension

The rotation of the mode cam moves the back tension lever which entered the cam groove and applies back tension to the supply reel.

This operation is performed only during review.

Operation of the T Reel Back Tension from On to Off

Mode cam ↗ Ⓐ direction → ↓ Ⓑ portion of cam shape → back tension lever pin ① ↘ Ⓒ direction → back tension lever centering on fulcrum ② ↗ Ⓓ direction → back tension off



* Current position: Back tension ON

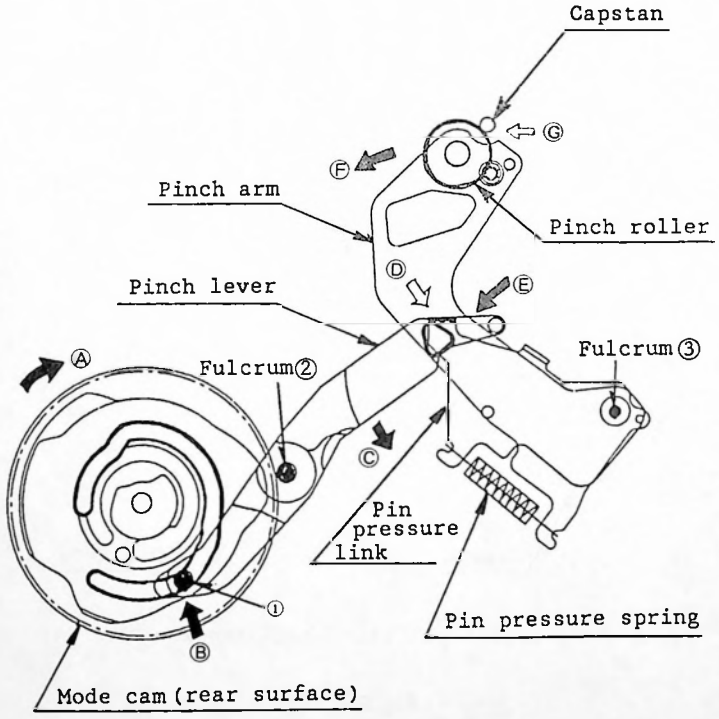
Fig. 9–17

6) Operation of the Pinch Roller

In the operation where the pinch roller applies pressure to the capstan when the posts are in the load state, the rotation of the mode cam moves the pinch lever and presses the pin pressure link. This pulls the pin pressure spring, the pinch arm moves and the pinch roller applies pressure.

Operation of the Pinch Roller from On to Off

Mode cam ↗Ⓐ direction → pinch lever, pin ① ↖Ⓑ direction → pinch lever centering on fulcrum ② ↘Ⓒ direction → △ and pin pressure link → separates (↓Ⓓ portion) → pin pressure link ↙Ⓔ direction → pinch arm centering on fulcrum ③ ↙Ⓕ direction → capstan and pinch roller separate ← Ⓖ portion



* Current position: Pinch roller ON

Fig. 9–18

Operating State of the Basic Modes (6 patterns)
Once the operations of the major parts (described in 1 to 6) described above are understood, the operating positions of the basic modes will be described since the basic modes described next represent the combinations of these operations.

9-7 Detection of Mechanism Operation

The operating state of the mechanism is detected by two switches:
2-contact rotary load switch
3-contact rotary mode switch

Mechanism information is fed to the mechanism control from the high and low states of the 2 bits (load switch) and 3 bits (mode switch). The mechanism control interprets the state of the mechanism and supplies the appropriate commands to the mode motor and capstan motor to properly control the mechanism.

Mechanism Mode Tables

The operating positions of the load switch, mode switch and major parts are shown for each mode in Table 9-1.

The operating states for each mode transition are shown with respect to time in Table 9-2. From this table, one can clearly see the switching of the various parts during one rotation (10° to 310°) of the mode cam.

Mechanism Modes

Mode	Gear	Brake S	Brake T	Tension Regulator	T reel BT	Pinch Roller	Load Gear
Cassette insertion	P idler	ON	ON	OFF	OFF	OFF	ON
Slack take up	P idler	OFF	ON	OFF	OFF	OFF	ON
End of tape rewind	F idler	OFF	OFF	OFF	OFF	OFF	OFF
Tape load	P idler	OFF	ON	OFF	OFF	OFF	ON
Pause (stop)	F idler	ON	ON	OFF	OFF	OFF	OFF
Play	P idler	OFF	OFF	ON	OFF	ON	OFF
Review	P idler	OFF	OFF	ON	ON	ON	OFF
FF/REW	F idler	OFF	OFF	OFF	OFF	OFF	OFF
FF/REW (pause)	F idler	OFF (Plunger on)	OFF (Plunger on)	OFF	OFF	OFF	OFF
Unload	P idler	ON	ON	OFF	OFF	OFF	ON
Unload	P idler	OFF	ON	OFF	OFF	OFF	ON

Table 9–1

Mode Tables

The operation of each part is shown based on the rotation (10° to 310°) of the mode cam. (from left to right)

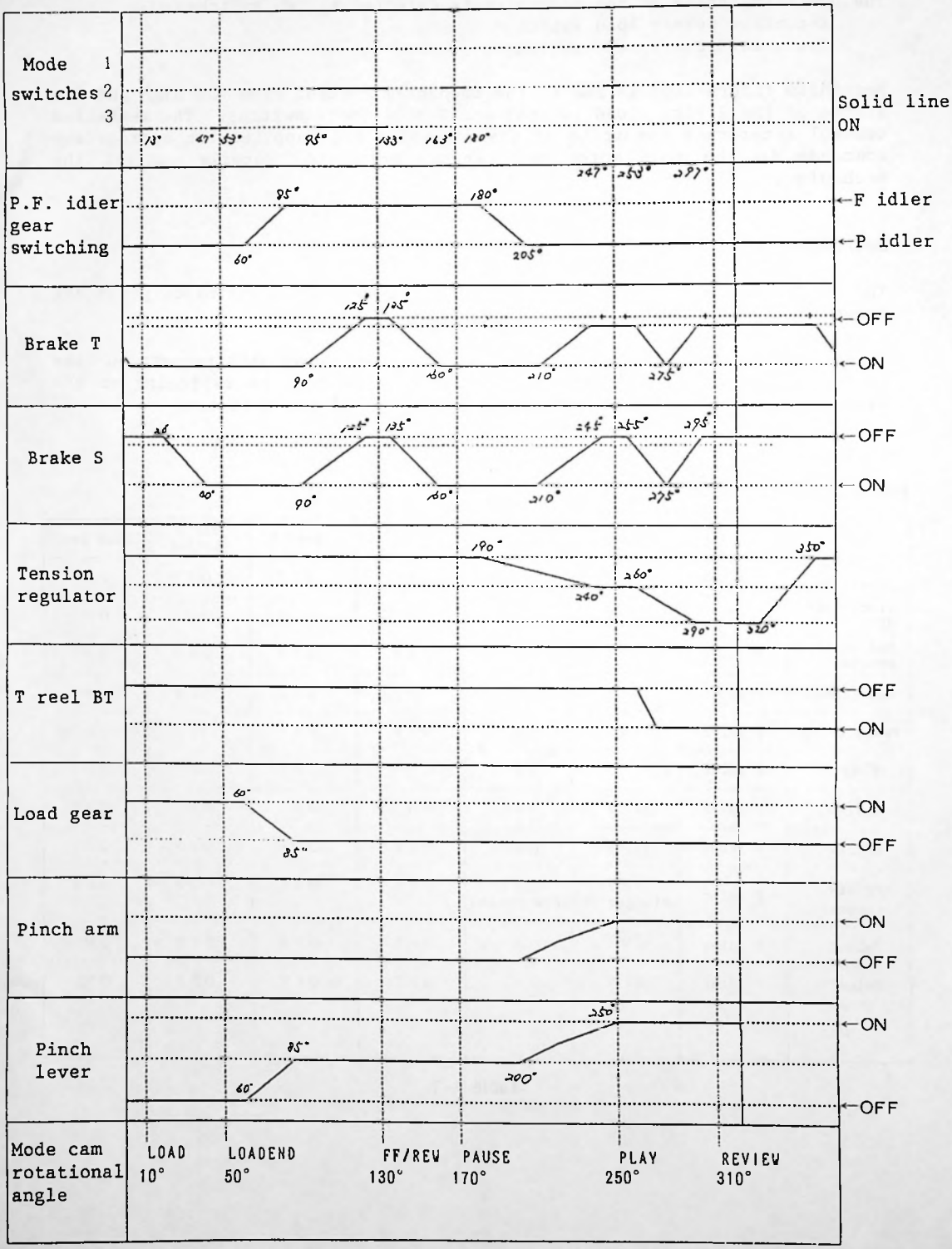
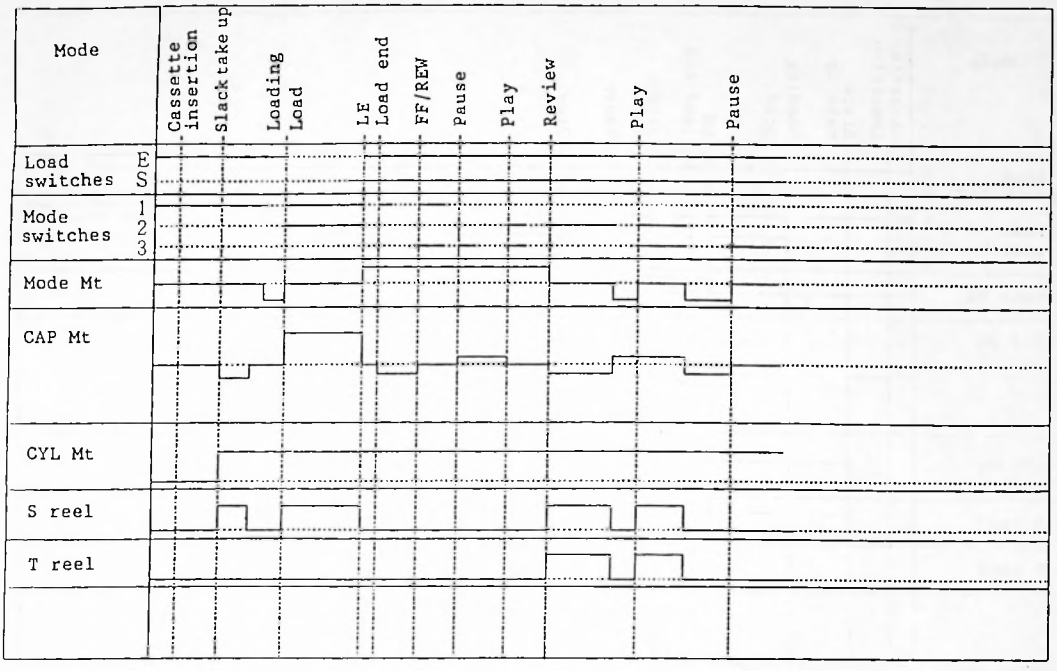
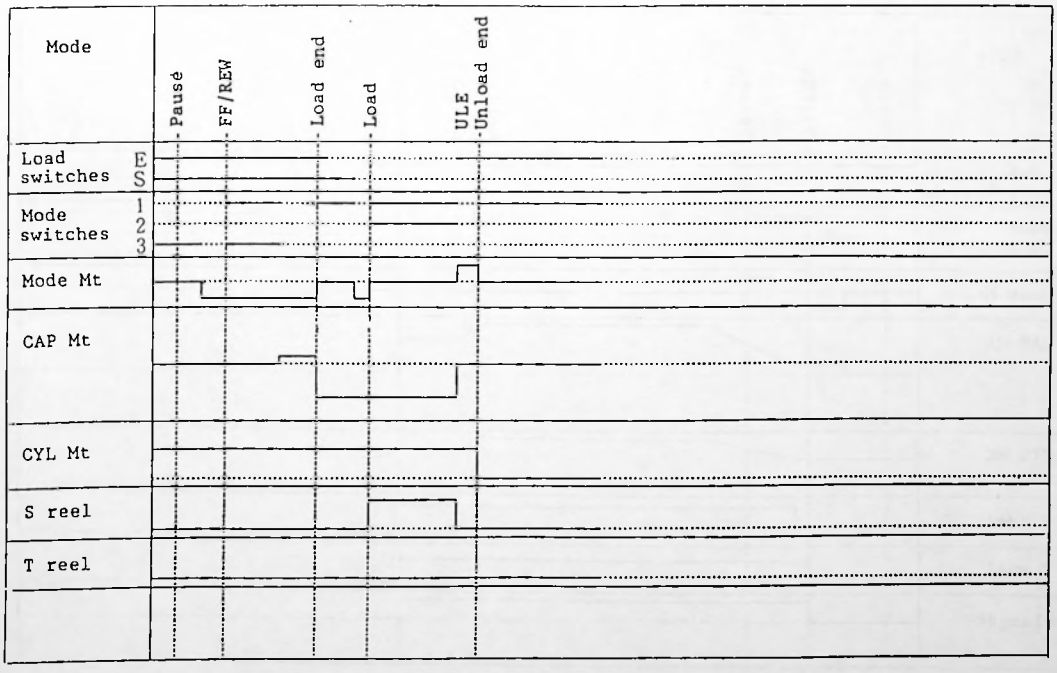


Table 9–2

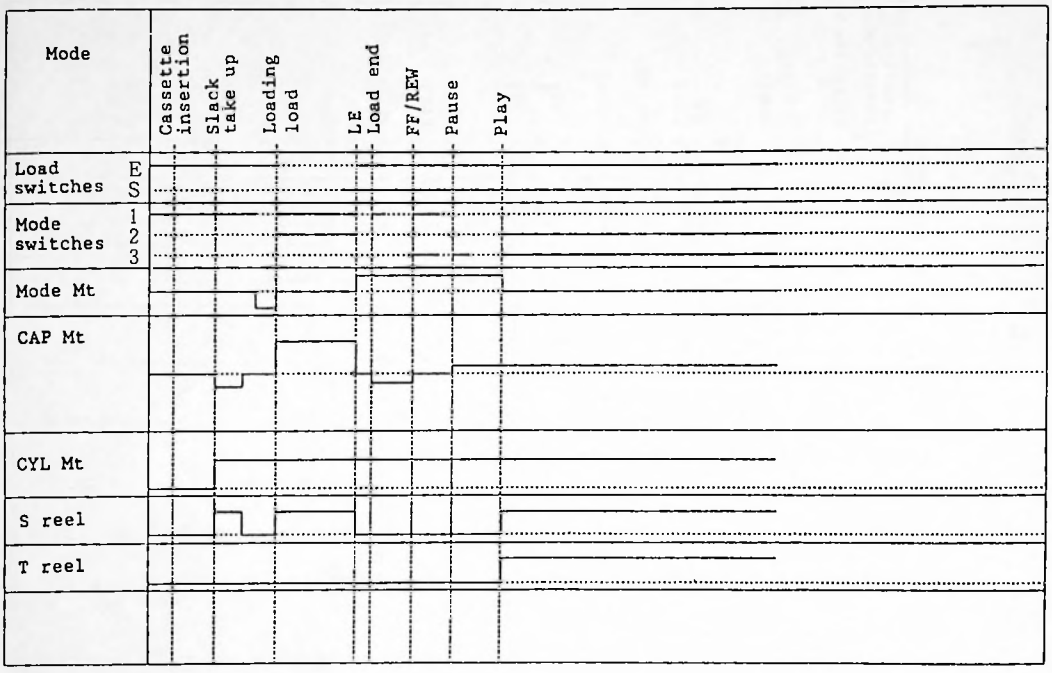
Cassette Insertion to Pause



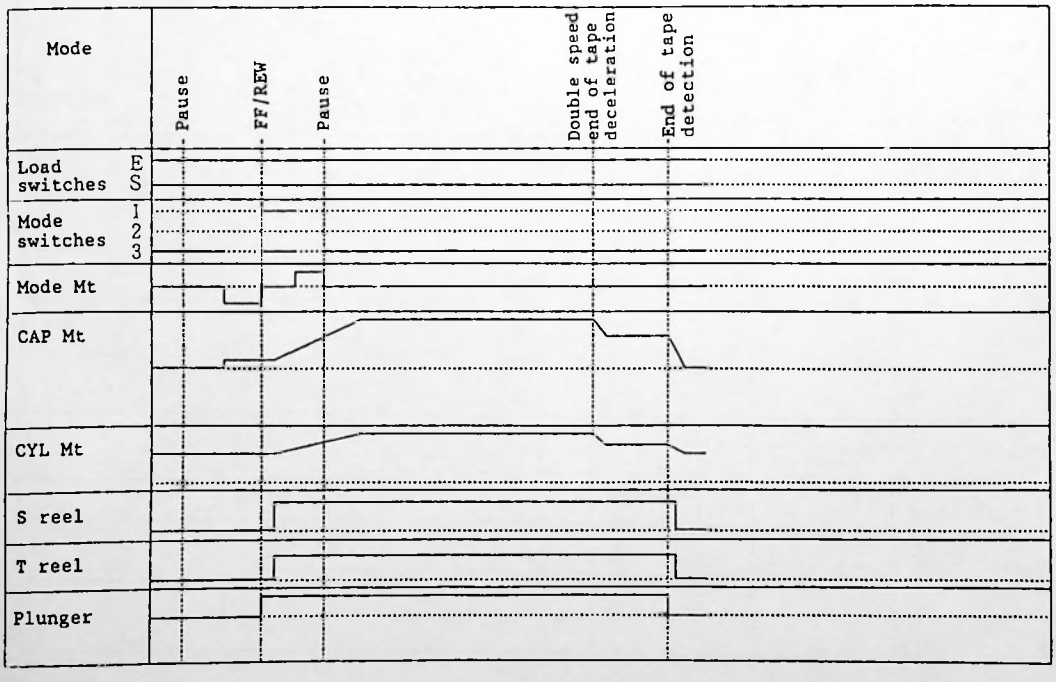
Pause to Unload



Cassette Insertion to Play



Pause to FF to End of Tape Stop



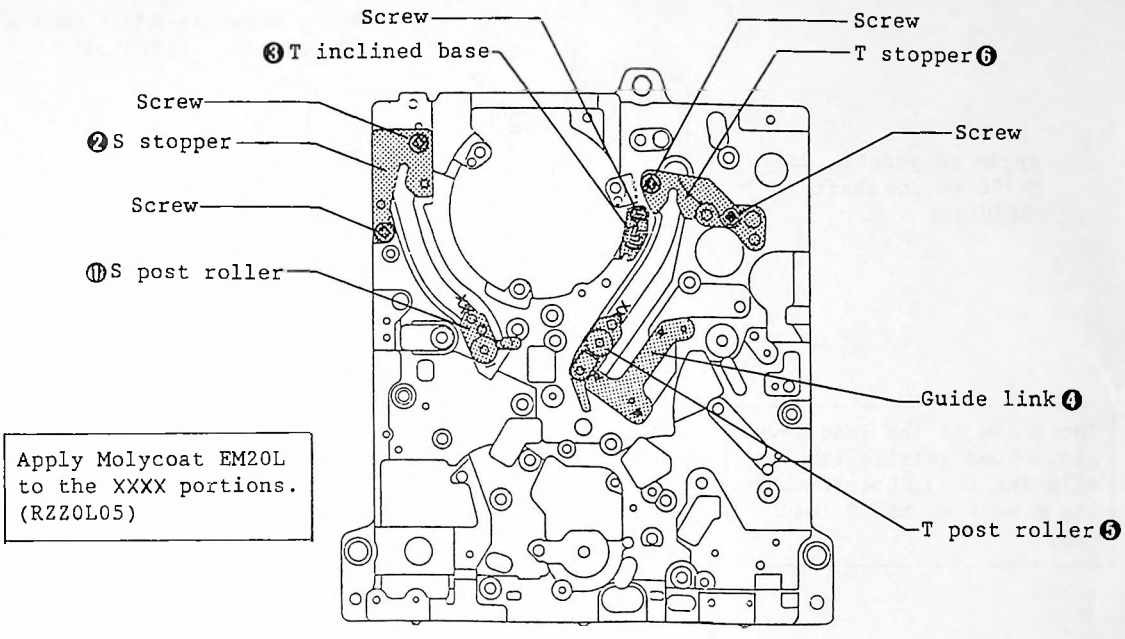
10. Mechanism Disassembly and Assembly

Disassemble in the sequence of: X, W, V, ... 3, 2, 1.

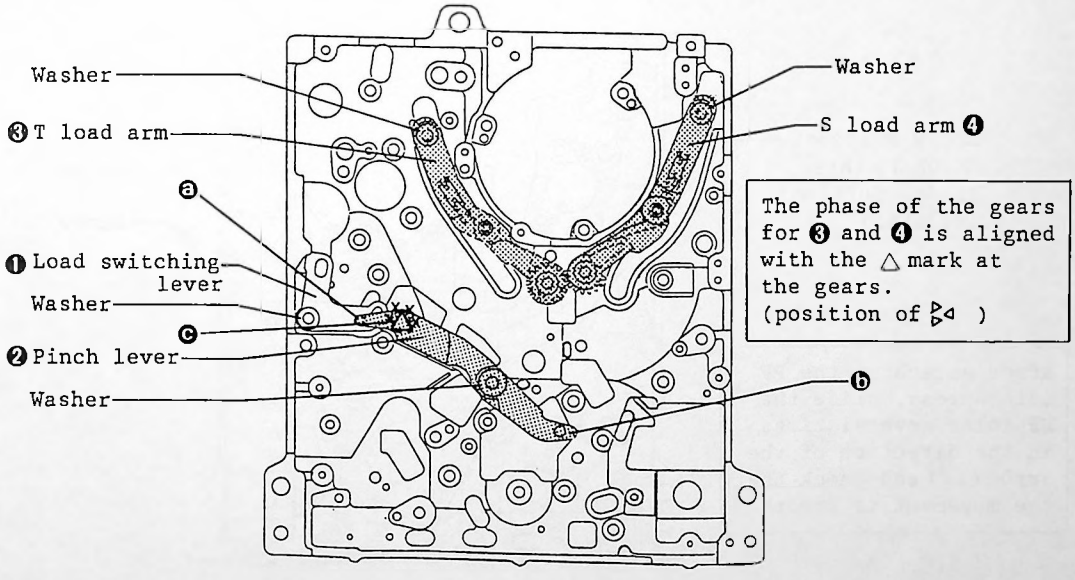
Assemble in the sequence of: A, B, C, ... 1, 2, 3.

10. Mechanism Disassembly and Assembly

[A] Assembly of the Post Roller



[B] Assembly of the Load Arm and Pinch Lever

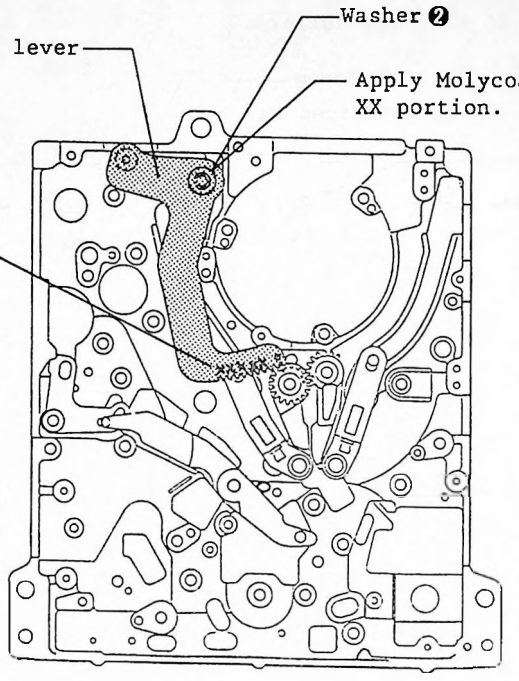


Be sure that "ⓐ" is inside the hole of the load switching lever.

Be sure that "ⓑ" is above the chassis.

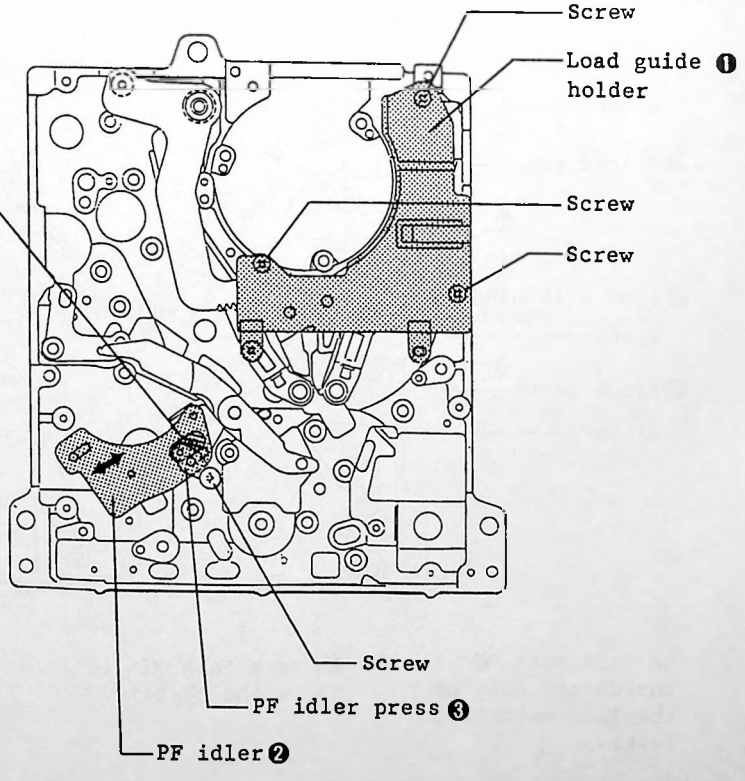
ⓒ Apply Molycoat EM20L to the XXXX portion at the △ on the rear surface of the pinch lever. (RZZ0L05)

[C] Assembly of the Load Lever



The phase of the load lever and T load gear is set by aligning the ○ hole with the ● mark on the T load gear.

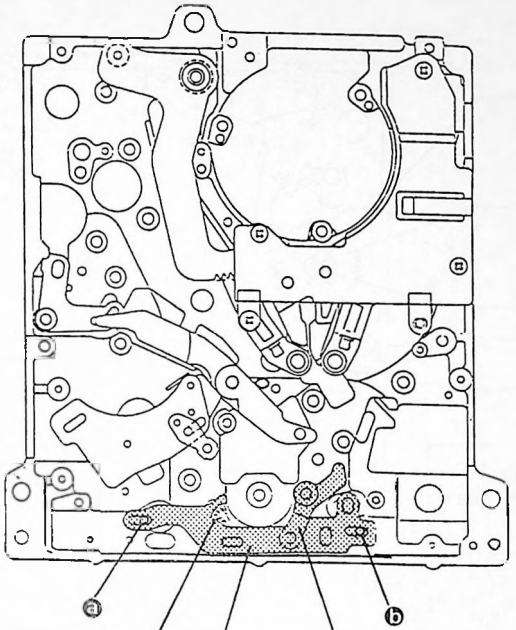
[D] Assembly of the PF Idler and Load Guide Holder



After attaching the PF idler press, slide the PF idler several times in the direction of the arrow (↔) and check that the movement is smooth.

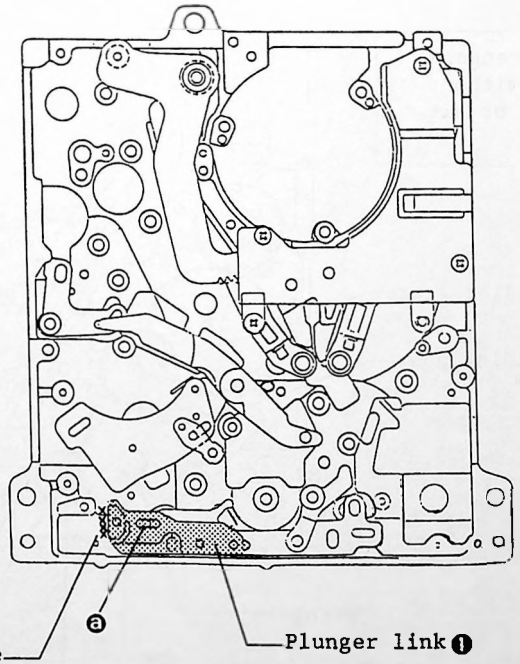
[E] Assembly of the S Brake Actuating Plate

When assembling the S brake actuating plate, be sure "ⓐ" and "ⓑ" are in the holes.

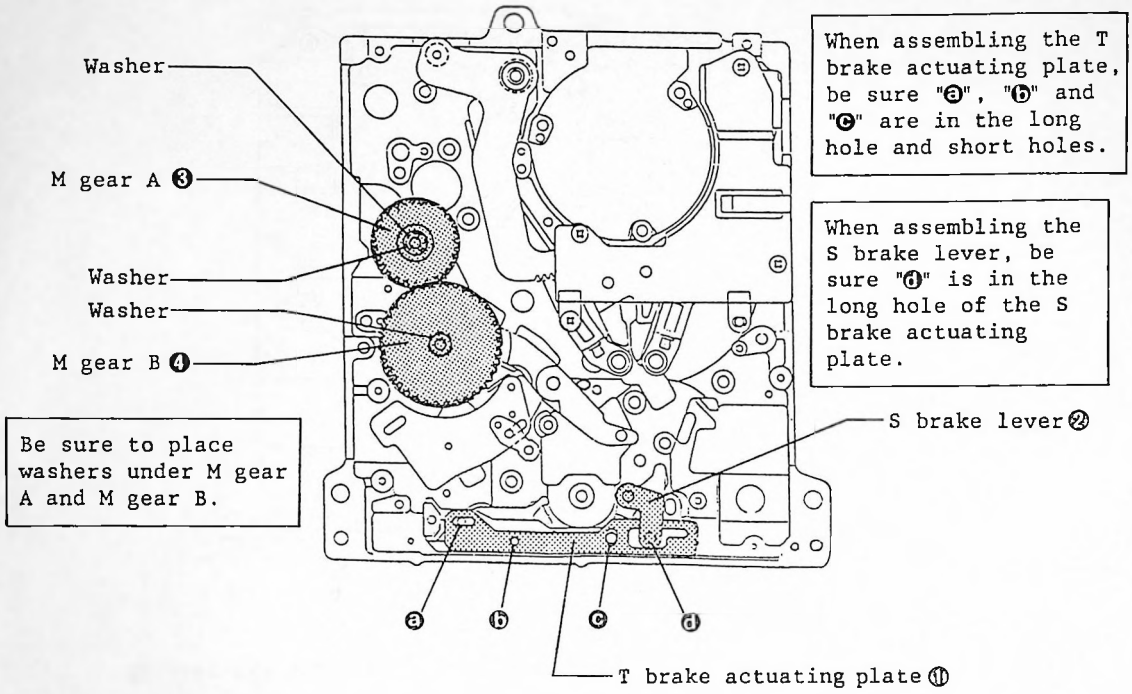


[F] Assembly of the Plunger Link

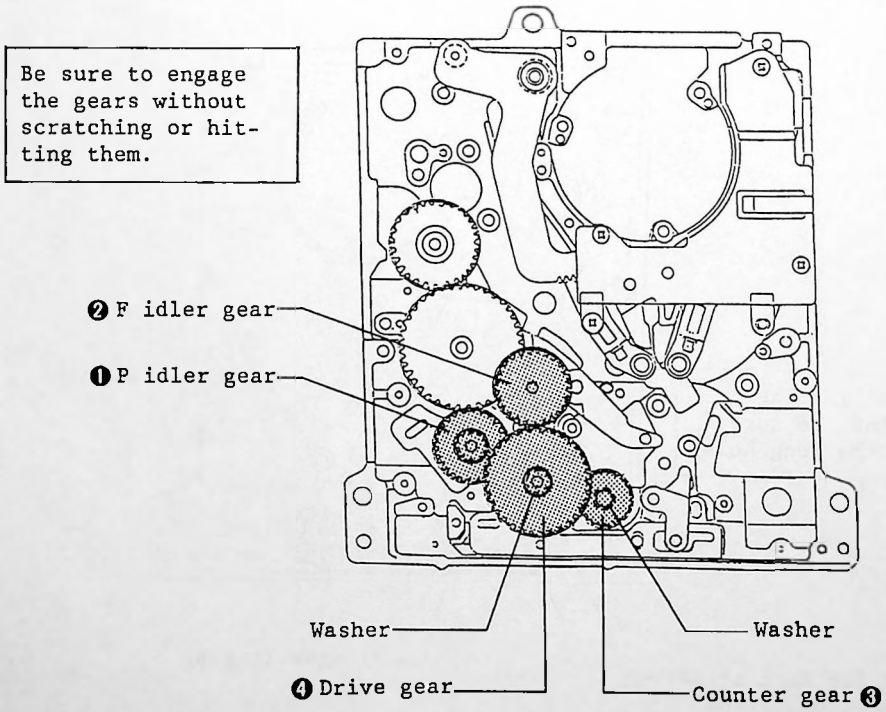
When assembling the plunger link, be sure "ⓐ" is in the long hole.



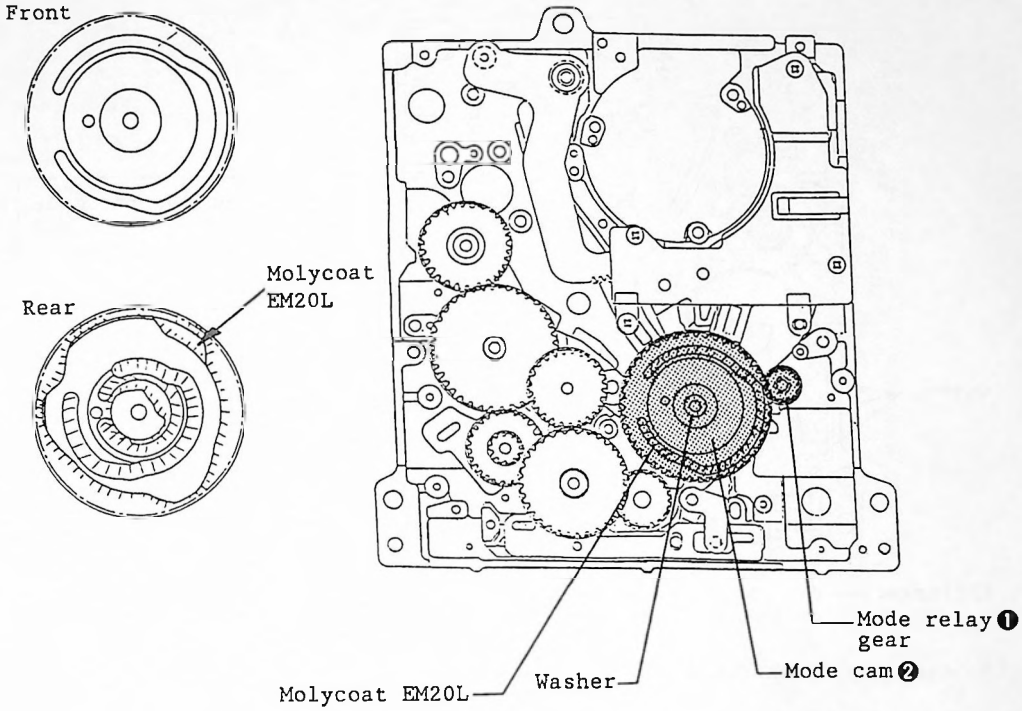
[G] Assembly of the M Gear A and B and T Brake Actuating Plate



[H] Assembly of the PF Idler Gear and Counter and Drive Gears

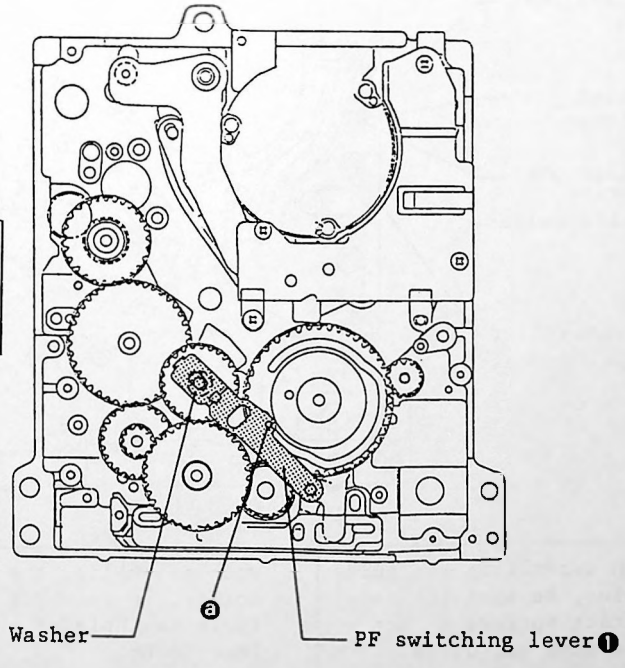


[I] Assembly of the Mode Cam and Mode Relay Gear

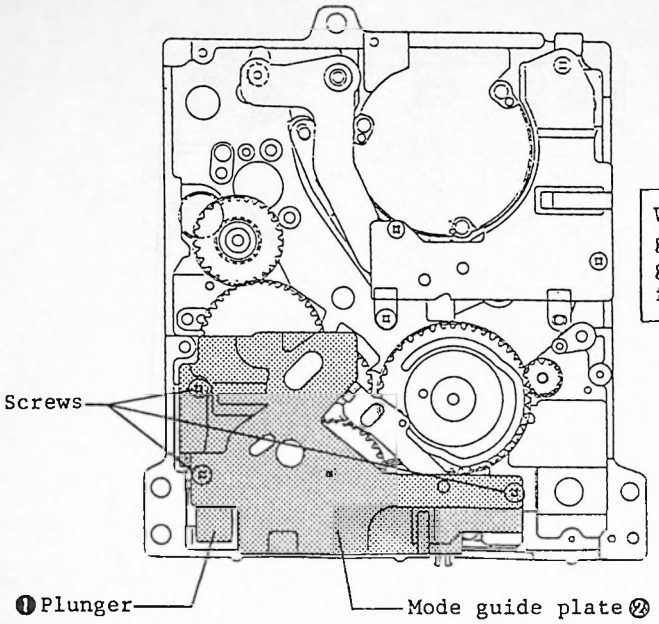


[J] Assembly of the PF Switching Lever

When assembling the PF switching lever, be sure "ⓐ" is in the cam's groove.

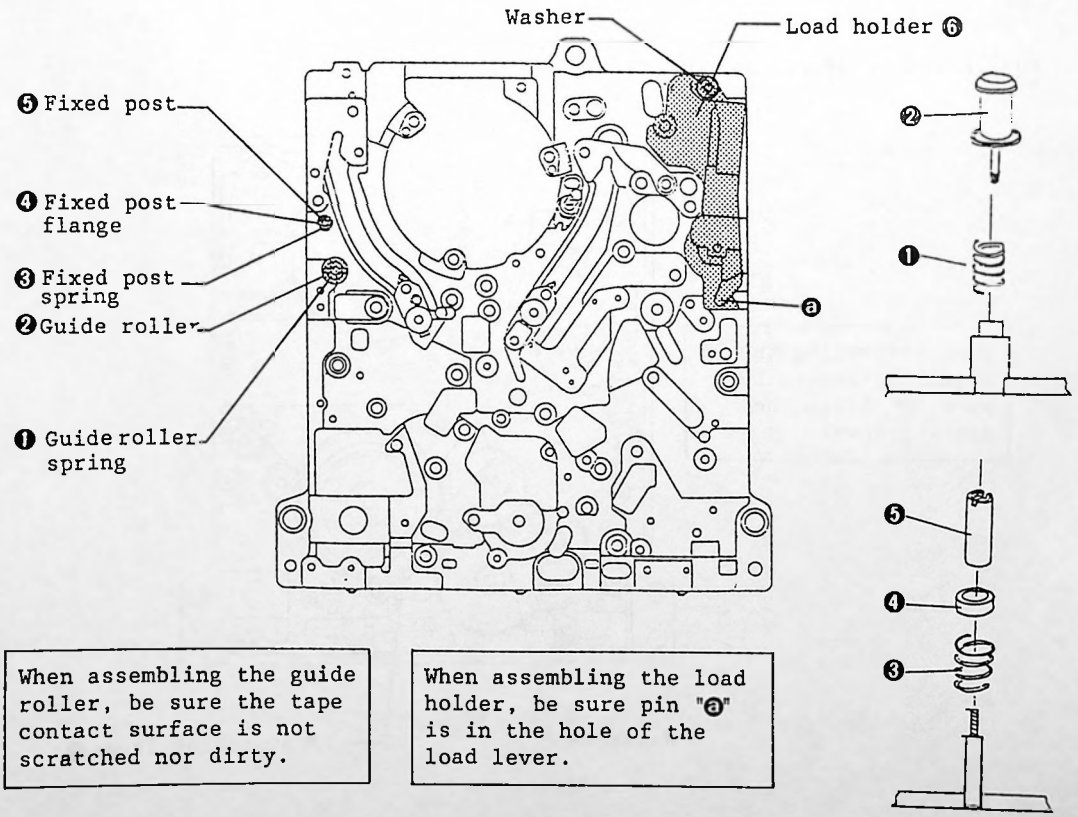


[K] Assembly of the Plunger and Mode Guide Plate



When assembling the mode guide plate, be sure the gears and plunger are firmly engaged.

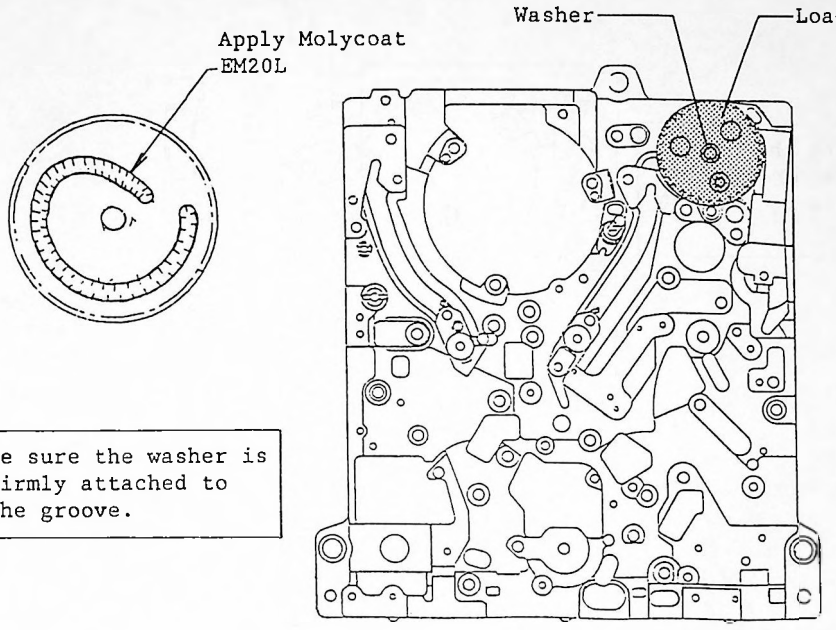
[L] Assembly of the Load Holder and Posts



When assembling the guide roller, be sure the tape contact surface is not scratched nor dirty.

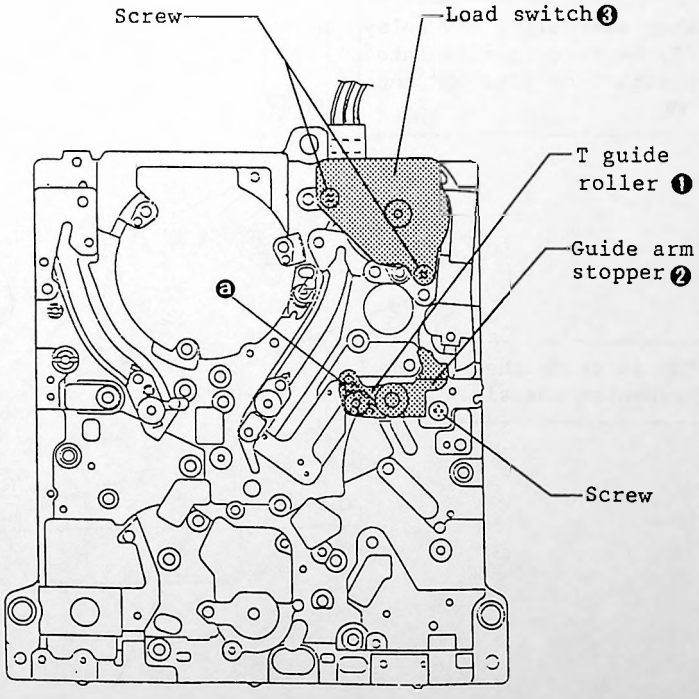
When assembling the load holder, be sure pin "ⓐ" is in the hole of the load lever.

[M] Assembly of the Load Cam



Be sure the washer is firmly attached to the groove.

[N] Assembly of the T Guide Roller and Load Switch

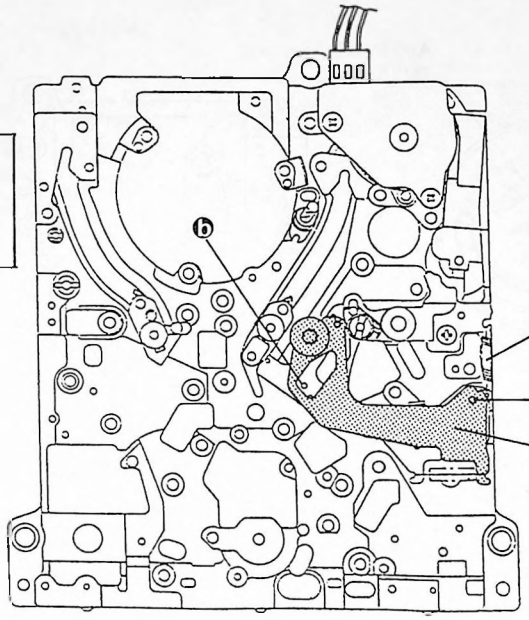


When assembling the T guide roller, be sure it is in the groove of the guide arm spring shaft of "ⓐ".

When assembling the load switch, be sure the positioning pin is in the hole of the load cam.

[O] Assembly of the Pinch Block and Return Spring

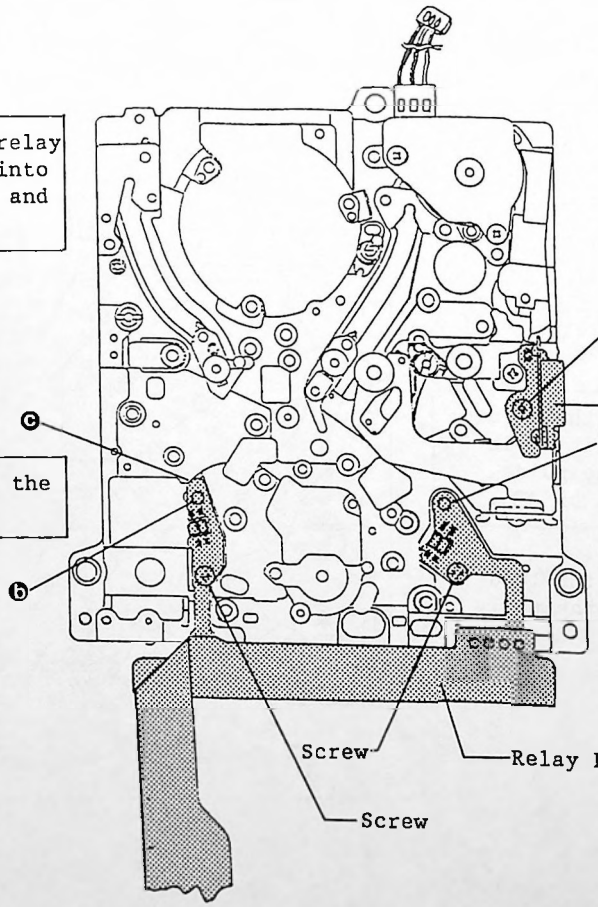
When assembling the pinch block, be sure "ⓐ" is not floating. Also be sure "ⓑ" is in the hole.



[P] Assembly of the Beginning of Tape Detector and Relay PB

When assembling the relay PB, be sure it fits into positioning pins "ⓐ" and "ⓑ".

"ⓒ" is sandwiched by the mechanism chassis.

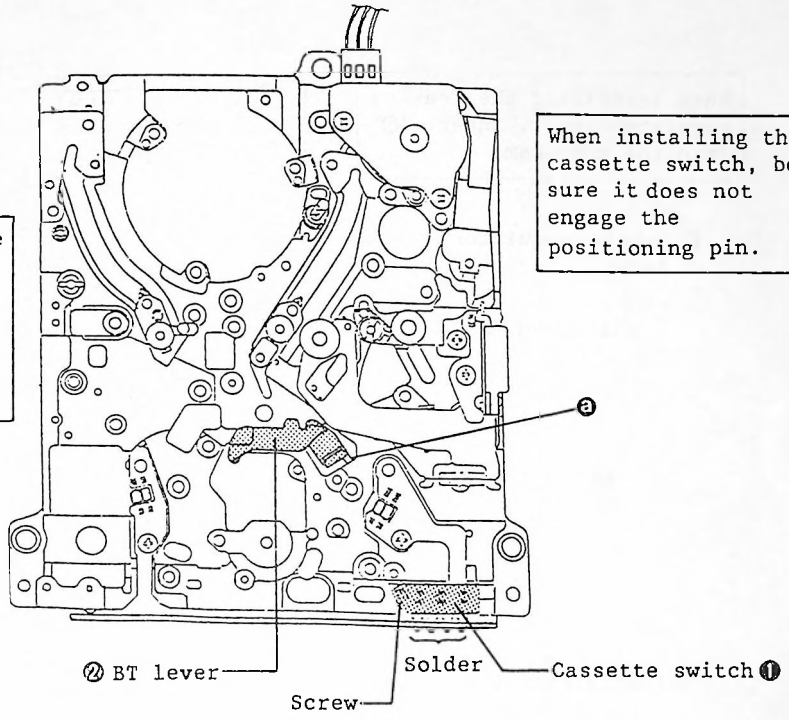


After installing the beginning of tape detector, check that the pinch arm rotates smoothly.

[Q] Assembly of the BT Lever and Cassette Switch

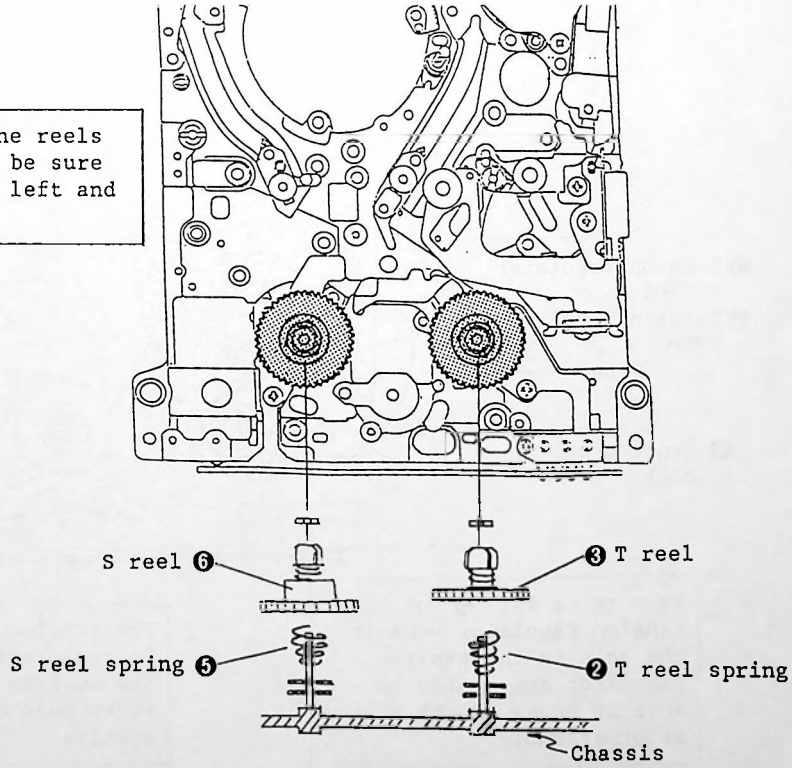
When assembling the BT lever, be sure "ⓐ" is below the chassis.
Also be sure the BT lever rotates smoothly.

When installing the cassette switch, be sure it does not engage the positioning pin.



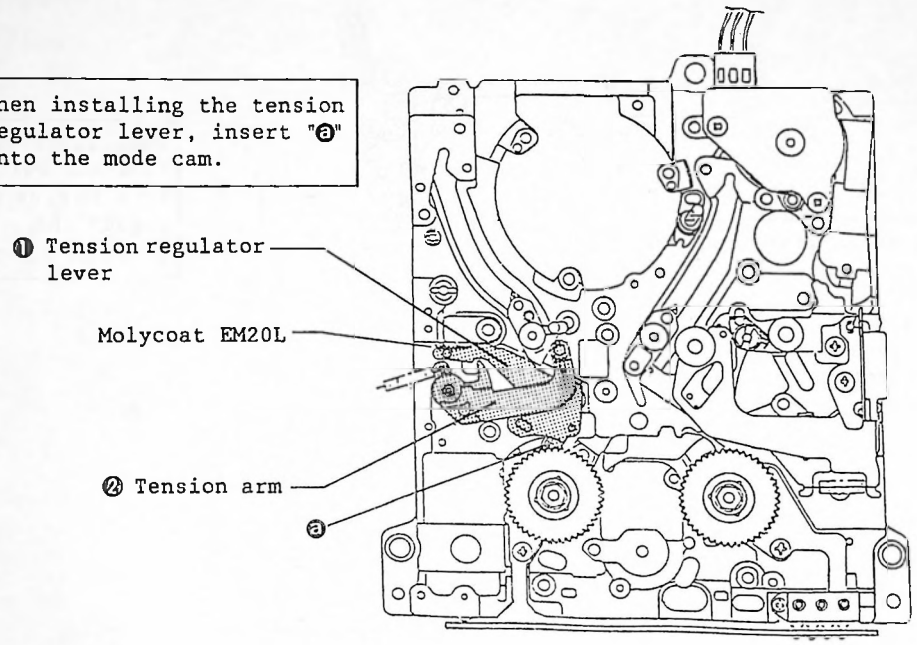
[R] Assembly of the S Reel and T Reel

When installing the reels and reel springs, be sure not to mix up the left and right parts.

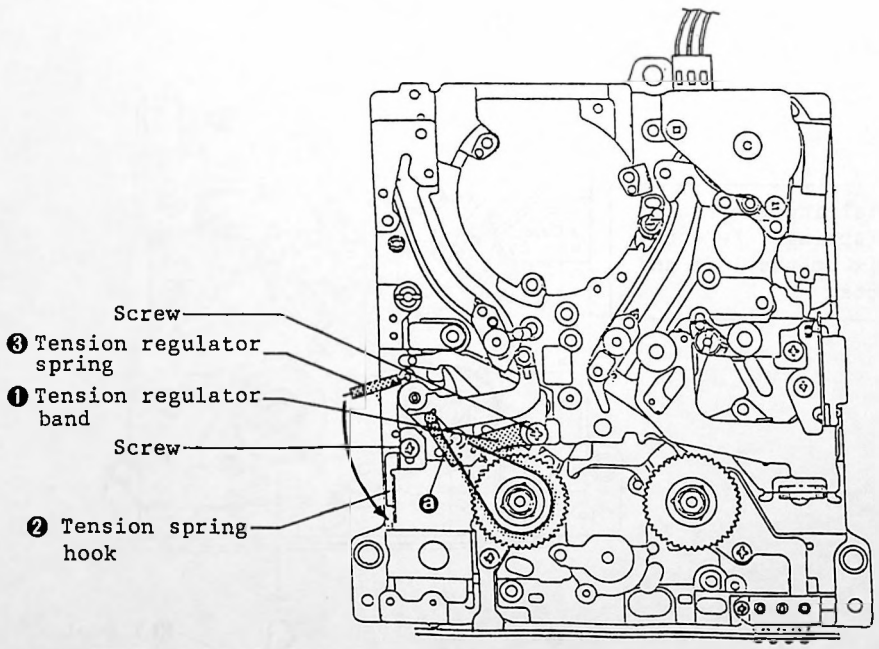


[S] Assembly of the Tension Regulator Lever and Tension Arm

When installing the tension regulator lever, insert "ⓐ" into the mode cam.



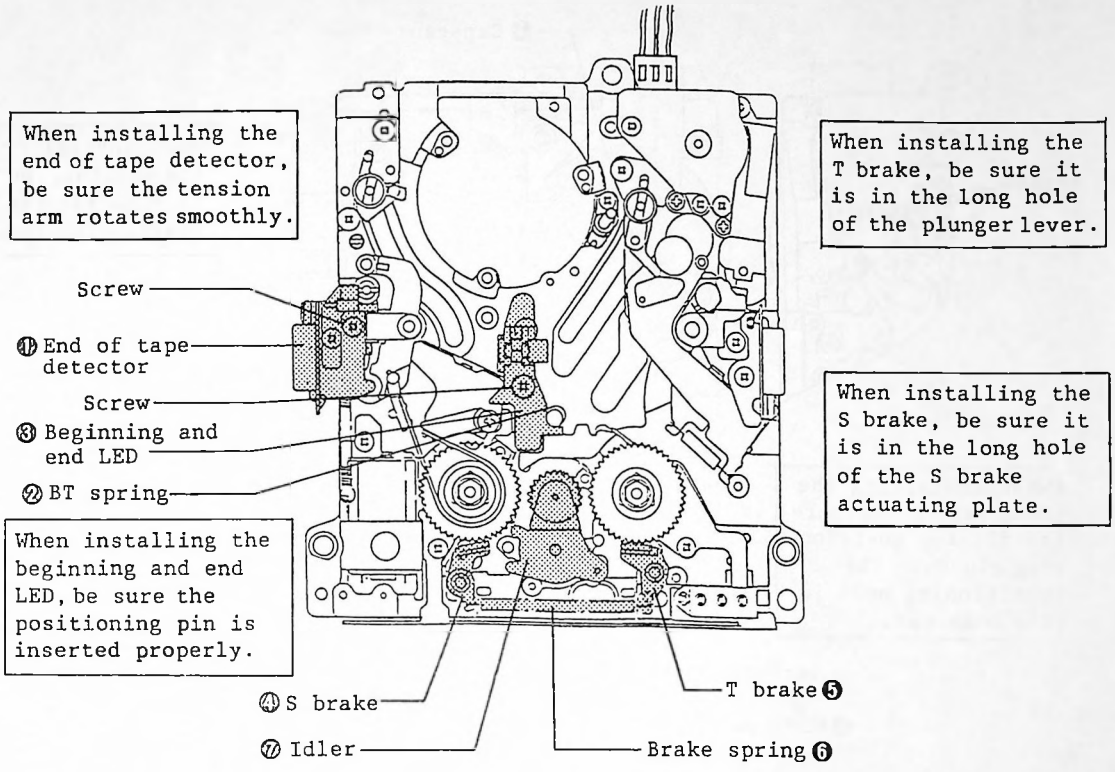
[T] Assembly of the Tension Regulator Band and Spring



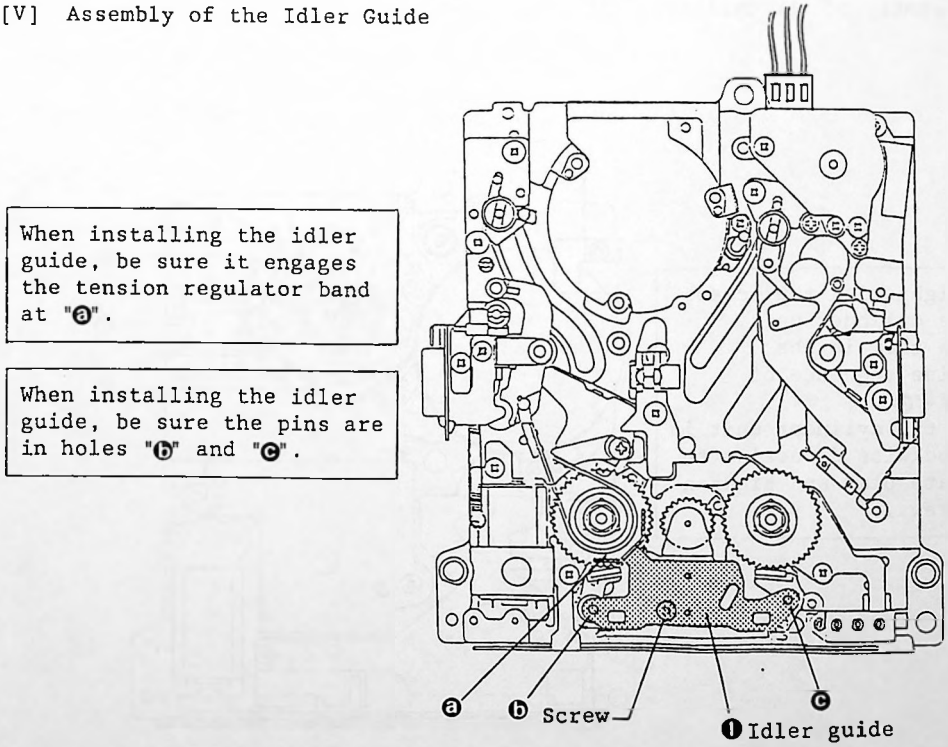
Be sure to fit "ⓐ" of the tension regulator band into the hole in the tension regulator arm. Also be sure it moves smoothly after assembly.

The tension regulator band is temporarily placed on the surface between the screw head and formed portion.

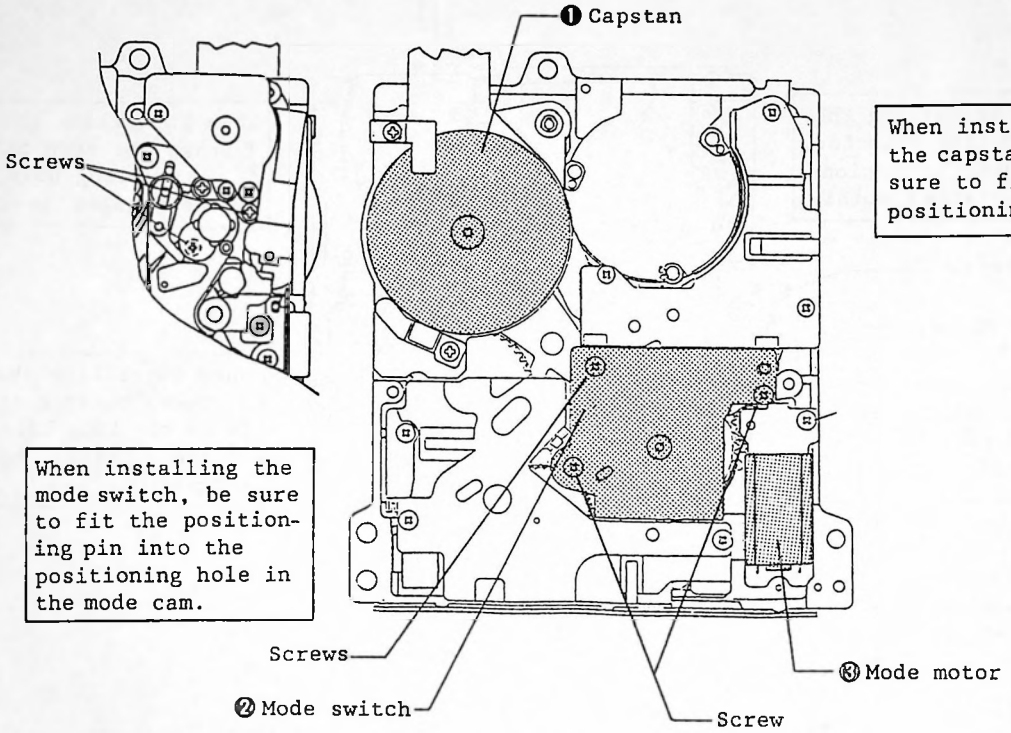
[U] Assembly of the S and T Brakes, Idler, Etc.



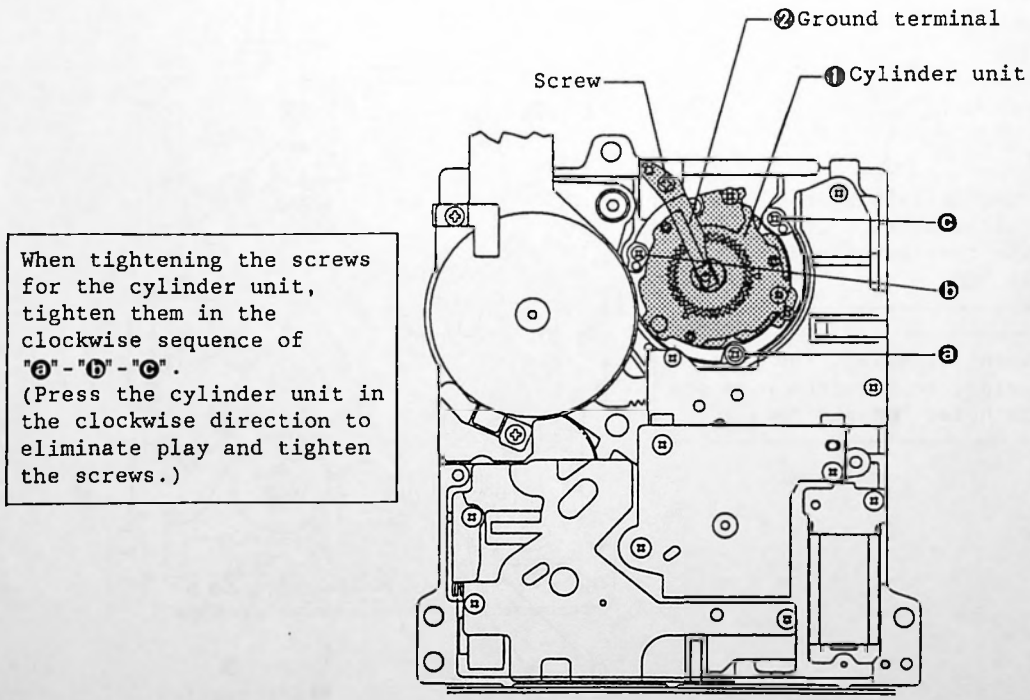
[V] Assembly of the Idler Guide



[W] Assembly of the Capstan, Mode Switch and Mode Motor



[X] Assembly of the Cylinder Unit



11. Troubleshooting Manual

1. Troubleshooting Flow-Chart

2. Servo Section

2-1 Block Diagram

2-2 Power On Flowchart: General

2-3 Trouble Analysis Manual

1) Capstan System
2) Cylinder System
3) Reel System
4) ATF System
5) Mode Motor System
6) Cassette Loading System
7) Tape Problems (includes EOT and BOT)

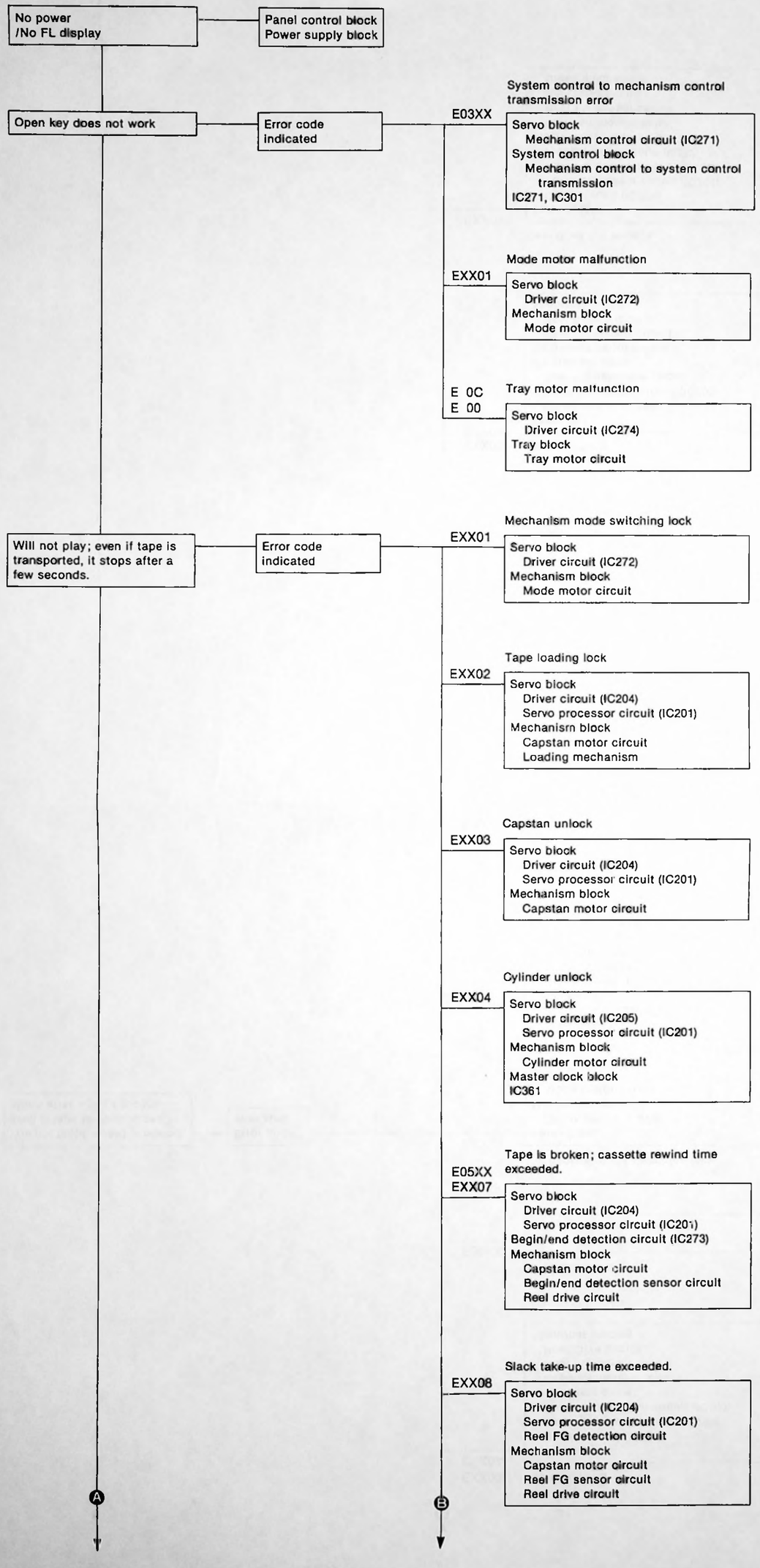
3. Digital Section

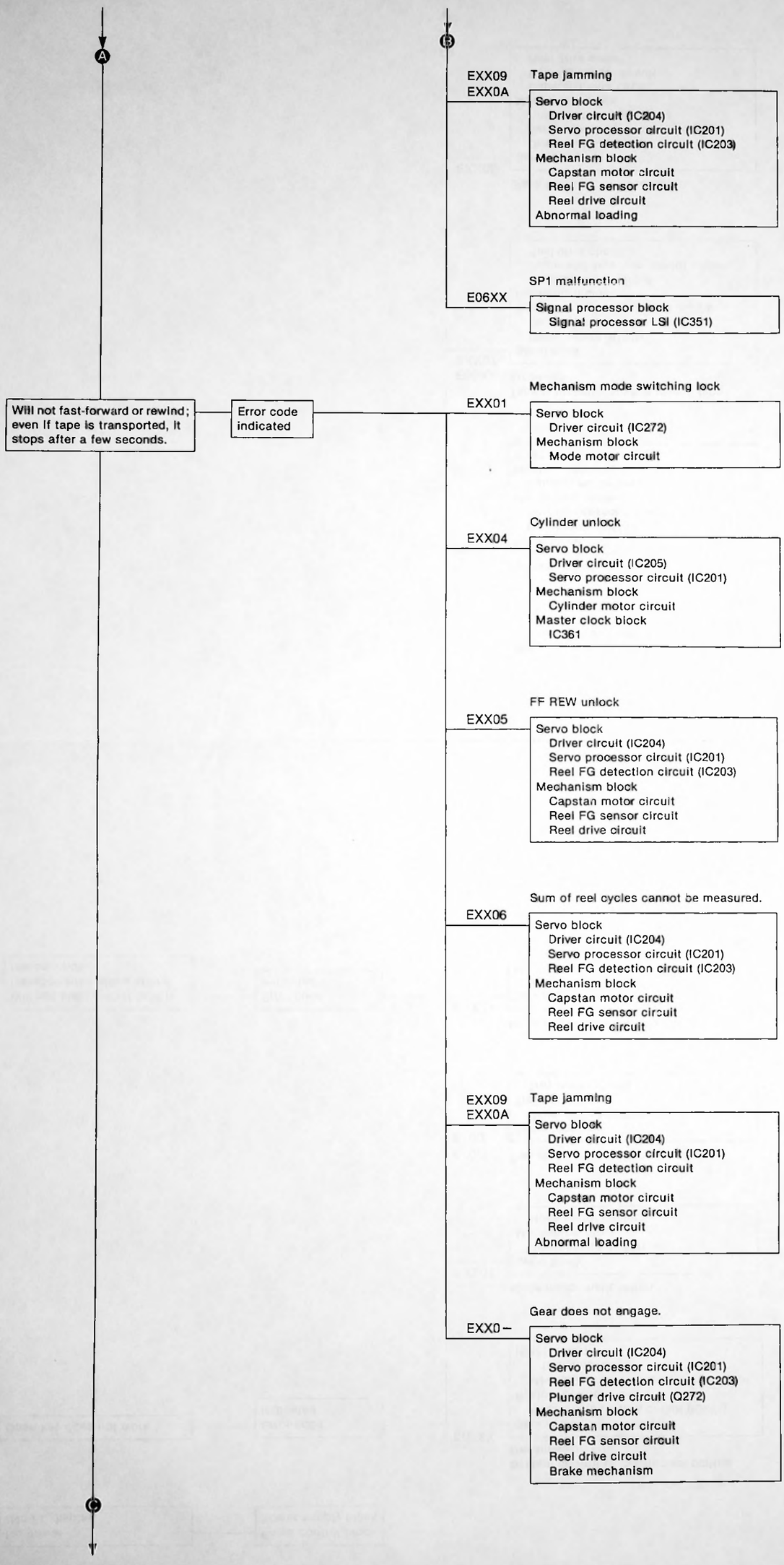
3-1 Operation Overview

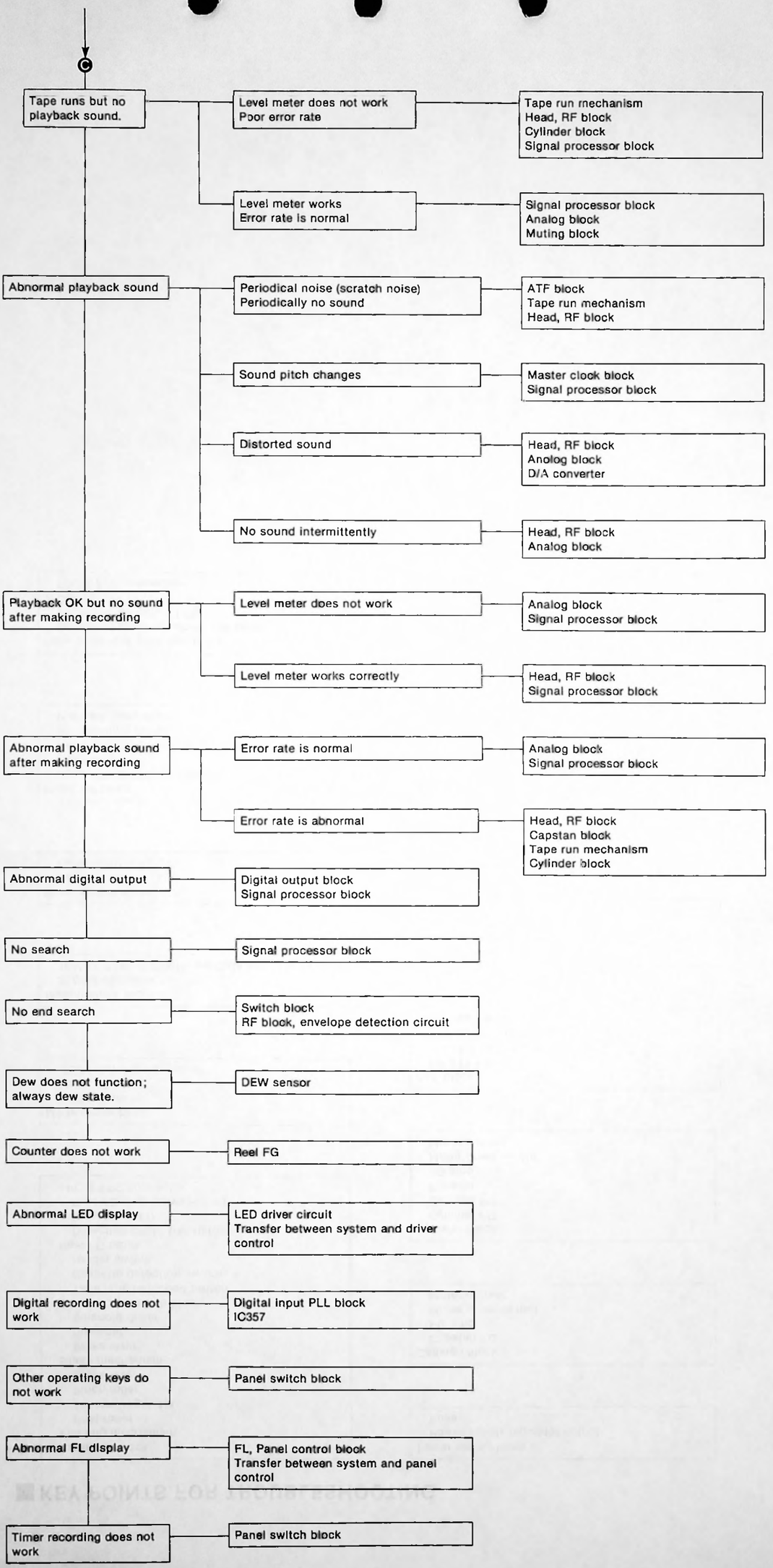
3-2 Detailed Operation of Each Section

3-3 Data Transfer in Each Section

4. Hints for Tape Transport Mechanism Adjustment


No power
/No FL display
Panel control block
Power supply block
Open key does not work
Error code indicated
System control to mechanism control transmission error
E03XX
Servo block
Mechanism control circuit (IC271)
System control block
Mechanism control to system control transmission
IC271, IC301
Mode motor malfunction
EXX01
Servo block
Driver circuit (IC272)
Mechanism block
Mode motor circuit
E 0C
E 00
Tray motor malfunction
Servo block
Driver circuit (IC274)
Tray block
Tray motor circuit
Will not play; even if tape is transported, it stops after a few seconds.
Error code indicated
Mechanism mode switching lock
EXX01
Servo block
Driver circuit (IC272)
Mechanism block
Mode motor circuit
Tape loading lock
EXX02
Servo block
Driver circuit (IC204)
Servo processor circuit (IC201)
Mechanism block
Capstan motor circuit
Loading mechanism
Capstan unlock
EXX03
Servo block
Driver circuit (IC204)
Servo processor circuit (IC201)
Mechanism block
Capstan motor circuit
Cylinder unlock
EXX04
Servo block
Driver circuit (IC205)
Servo processor circuit (IC201)
Mechanism block
Cylinder motor circuit
Master clock block
IC361
Tape is broken; cassette rewind time exceeded.
E05XX
EXX07
Servo block
Driver circuit (IC204)
Servo processor circuit (IC201)
Begin/end detection circuit (IC273)
Mechanism block
Capstan motor circuit
Begin/end detection sensor circuit
Reel drive circuit
Slack take-up time exceeded.
EXX08
Servo block
Driver circuit (IC204)
Servo processor circuit (IC201)
Reel FG detection circuit
Mechanism block
Capstan motor circuit
Reel FG sensor circuit
Reel drive circuit
A
B


A
B
C
Will not fast-forward or rewind; even if tape is transported, it stops after a few seconds.
Error code indicated
EXX09
EXX0A
Tape jamming
Servo block
Driver circuit (IC204)
Servo processor circuit (IC201)
Reel FG detection circuit (IC203)
Mechanism block
Capstan motor circuit
Reel FG sensor circuit
Reel drive circuit
Abnormal loading
E06XX
SP1 malfunction
Signal processor block
Signal processor LSI (IC351)
EXX01
Mechanism mode switching lock
Servo block
Driver circuit (IC272)
Mechanism block
Mode motor circuit
EXX04
Cylinder unlock
Servo block
Driver circuit (IC205)
Servo processor circuit (IC201)
Mechanism block
Cylinder motor circuit
Master clock block
IC361
EXX05
FF REW unlock
Servo block
Driver circuit (IC204)
Servo processor circuit (IC201)
Reel FG detection circuit (IC203)
Mechanism block
Capstan motor circuit
Reel FG sensor circuit
Reel drive circuit
EXX06
Sum of reel cycles cannot be measured.
Servo block
Driver circuit (IC204)
Servo processor circuit (IC201)
Reel FG detection circuit (IC203)
Mechanism block
Capstan motor circuit
Reel FG sensor circuit
Reel drive circuit
EXX09
EXX0A
Tape jamming
Servo block
Driver circuit (IC204)
Servo processor circuit (IC201)
Reel FG detection circuit
Mechanism block
Capstan motor circuit
Reel FG sensor circuit
Reel drive circuit
Abnormal loading
EXX0–
Gear does not engage.
Servo block
Driver circuit (IC204)
Servo processor circuit (IC201)
Reel FG detection circuit (IC203)
Plunger drive circuit (Q272)
Mechanism block
Capstan motor circuit
Reel FG sensor circuit
Reel drive circuit
Brake mechanism


Tape runs but no playback sound.
Level meter does not work
Poor error rate
Tape run mechanism
Head, RF block
Cylinder block
Signal processor block
Level meter works
Error rate is normal
Signal processor block
Analog block
Muting block
Abnormal playback sound
Periodical noise (scratch noise)
Periodically no sound
ATF block
Tape run mechanism
Head, RF block
Sound pitch changes
Master clock block
Signal processor block
Distorted sound
Head, RF block
Analog block
D/A converter
No sound intermittently
Head, RF block
Analog block
Playback OK but no sound after making recording
Level meter does not work
Analog block
Signal processor block
Level meter works correctly
Head, RF block
Signal processor block
Abnormal playback sound after making recording
Error rate is normal
Analog block
Signal processor block
Error rate is abnormal
Head, RF block
Capstan block
Tape run mechanism
Cylinder block
Abnormal digital output
Digital output block
Signal processor block
No search
Signal processor block
No end search
Switch block
RF block, envelope detection circuit
Dew does not function; always dew state.
DEW sensor
Counter does not work
Reel FG
Abnormal LED display
LED driver circuit
Transfer between system and driver control
Digital recording does not work
Digital input PLL block
IC357
Other operating keys do not work
Panel switch block
Abnormal FL display
FL, Panel control block
Transfer between system and panel control
Timer recording does not work
Panel switch block

■ KEY POINTS FOR TROUBLESHOOTING

- Mechanism block
  - Loading mechanism
    - Post roller
    - Tension regulator
    - Pinch roller
    - Brake lever
  - Brake mechanism
    - Brake lever
    - Solenoid
    - Solenoid driver
  - Mechanism switch block
    - Tape hole detection switch
    - Cassette detection switch
    - Holder switch
  - Reel FG block
    - Detection photo transistor
    - Detection LED
    - Reel FG amp (servo P.C.B.)
  - FPC & FPC connector

- Mode motor block
  - Mode motor
  - Mode switch
  - Mode motor driver circuit

- Master clock block
  - 28 MHz oscillator
  - 16 MHz, 22 MHz, 24 MHz oscillate and select circuit

- Panel switch block
  - Switch
  - Panel control IC

- Head, RF block
  - Head FPC & FPC connector
  - Head dirty
  - Head cracked or damaged
  - RF recording current
  - Playback eye pattern

- Tape begin/end detection block
  - Begin/end detection photo transistor
  - Begin/end detection LED
  - Comparator circuit
  - FPC & FPC connector

- Power supply block
  - Power supply regulator output
  - Fuse

- Capstan block
  - Capstan FG
  - FG amp
  - Motor driver output
  - Motor current

- Cylinder block
  - Cylinder FG
  - Cylinder PG
  - FG amp
  - PG amp
  - Motor driver output
  - Motor current

- ATF block
  - RF ATF output
    - ATF SYNC output
  - ATF select circuit
  - ATF gate allay

- Signal processor block
  - Data & clock to D/A
  - Data & clock to A/D
  - All clocks

- Digital output block
  - Digital output PB

- Panel control block
  - Panel control block
  - Transfer between panel and system control
  - Panel control reset

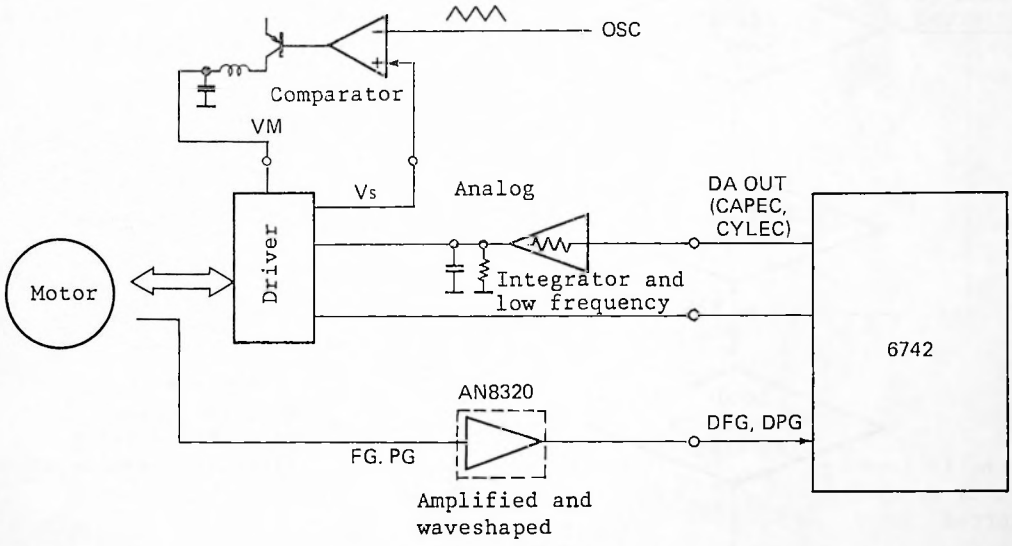
- Analog block
  - Input amplifier
  - Output amplifier
  - Muting circuit
  - A/D converter
  - D/A converter

2. Servo Section

2-1 Block Diagram

Mechanism control can be roughly divided into 2 parts:
1) Mode motor control which controls the mechanism modes
2) Capstan and cylinder motor control which controls tape travel

The mode motor control in 1) simply rotates the mode motor until the desired mode is achieved and is thus not complicated.
The control in 2) is illustrated in the block diagram below.

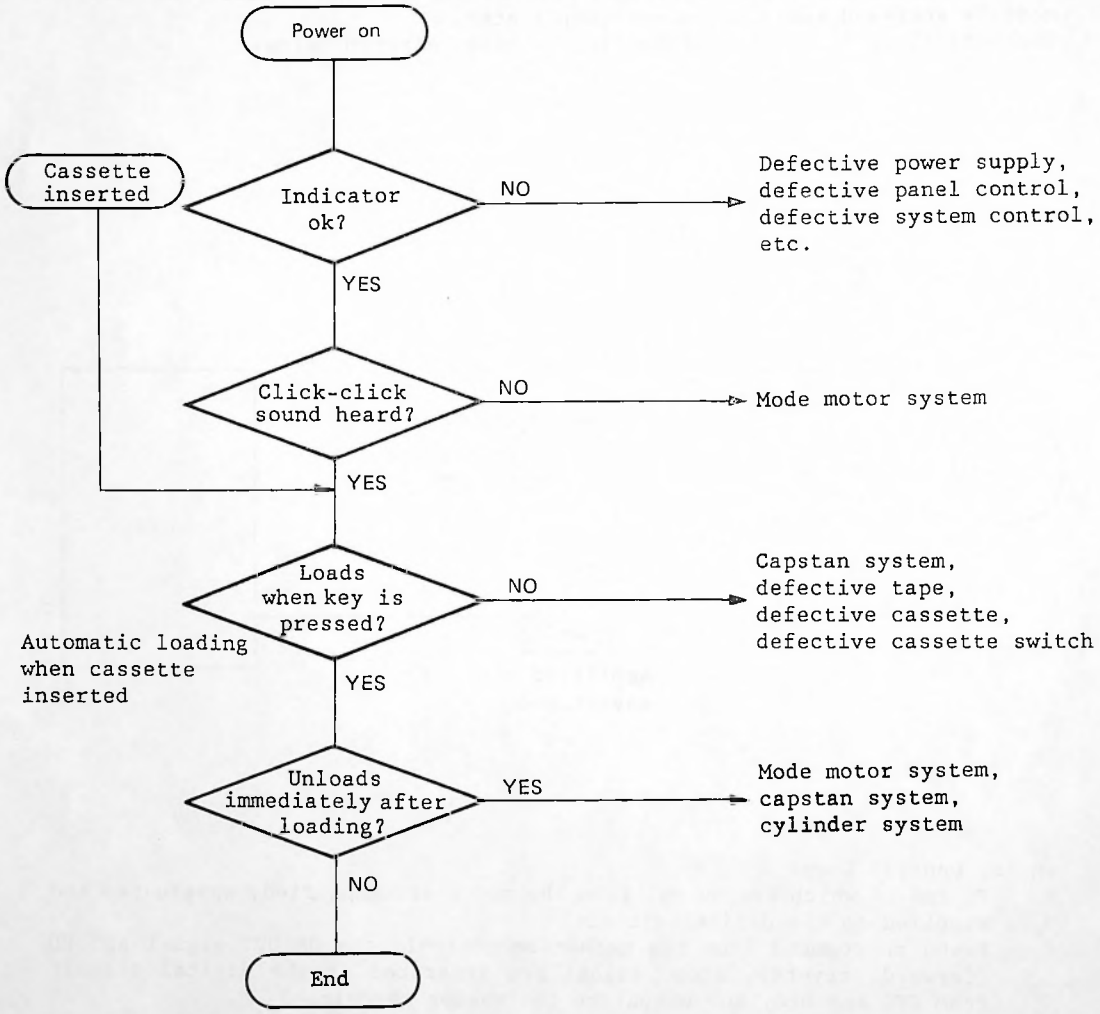


<Motor Control Loop>
- FG and PG which are output from the motor are amplified, waveshaped and supplied to the digital circuit
- Based on command from the mechanism control, the DA OUT signal and ED (forward, reverse, stop) signal are generated at the digital circuit from DFG and DPG, and output to the analog circuit.
- The DA OUT/ED signals are supplied to the mode driver after being interfaced.
- The motor is rotated using the motor driver.

<Voltage Control Loop>
- VS varies so that VM=Va+VCE(sat) is obtained.

2-2 Power On Flowchart: General

At power-on initialization (click-click sound), 90% of the mechanism and servo system is ok at a loading completion of 50%.
The general flowchart is shown below.



2-3 Trouble Analysis Manual

1) Capstan System

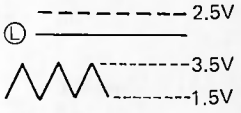
<Applicable Signals>

(1)	Capstan power supply:	CAVM, CAVS, VMREF
(2)	Capstan FG:	CADFG1, CADFG2
(3)	Capstan FG rotation command:	CAPED
(4)	Capstan DA output:	CAPEC

<Types of Trouble>

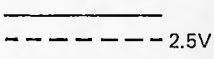
Motor trouble consists of 3 types: No rotation, erratic rotation, cogging.

(1) No rotation: If all ok, check the PCB below the mechanism.
- Is the unit mechanically locked?
- Is VM at 12 V?
- Is 5 V at CAPED?
- CAPEC output acceleration? ---------- Ⓛ



- VMREF is output? ----------

(2) Erratic rotation
- CADFG1 and CADFG2 output?
- CAPEC output deceleration? ---------- Ⓗ



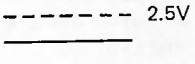
(3) Cogging
- Are CADFG1 and CADFG2 properly output when the cassette is removed and rotated by hand?
- Is the DA output natural?
  For example, repeated deceleration and acceleration, or full deceleration.
- Does CAPED match the rotational direction? (high for forward and low for reverse)
- Are H1 to H3 properly output when the cassette is removed and rotated by hand?

(4) Occasional stop: Temperature rise protection of the driver
- Is VM within 2.5 to 5 V? Is VS within 1.5 to 3.5 V?
- Is VMREF properly output?

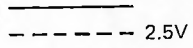
2) Cylinder System

<Applicable Signals>
(1) Cylinder power supply: CYLVM
(2) Cylinder FG and PG: DCYLFG, DCYLPG
(3) Cylinder rotation command: CYLED
(4) Cylinder DA output: CYLEC
(5) HSW, R3CP

<Types of Trouble>
(1) No rotation
- Is the unit mechanically locked?
- Is VM at 12 V?
- CYLED = 5 V?
- DA output acceleration? ---------- Ⓛ

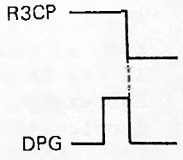


(2) Erratic rotation
- CYDFG being output? ---------- 1333Hz
- DA output deceleration? ---------- Ⓗ



(3) Cogging
- Is DCYLFG properly output according to the rotation when rotated by hand?
- Is the DA output natural? For example, repeated deceleration and acceleration.
- Is CYLED at 5 V?
- Are the CYL H1 to H3 properly output?

(4) Phase lock unlocks
CYL lock NG results. (EXX04)
- Is CYLDPG properly output?



- Is PG Gain switched during search?
- Does R3TV enter the 6742?

(5) HSW is not output.
- Are DCYLFG and DCYLPG output?

(6) Occasional stop: Temperature rise protection of the driver
- Is VM within 3-6 V?

3) Reel System

Check the following items.

<Applicable Signals>

(1) Reel FG: DRLFGT, DRLFGS
(2) Input capture switch: SELA, SELB
(3) Reset signal: NSRST

<Types of Trouble>

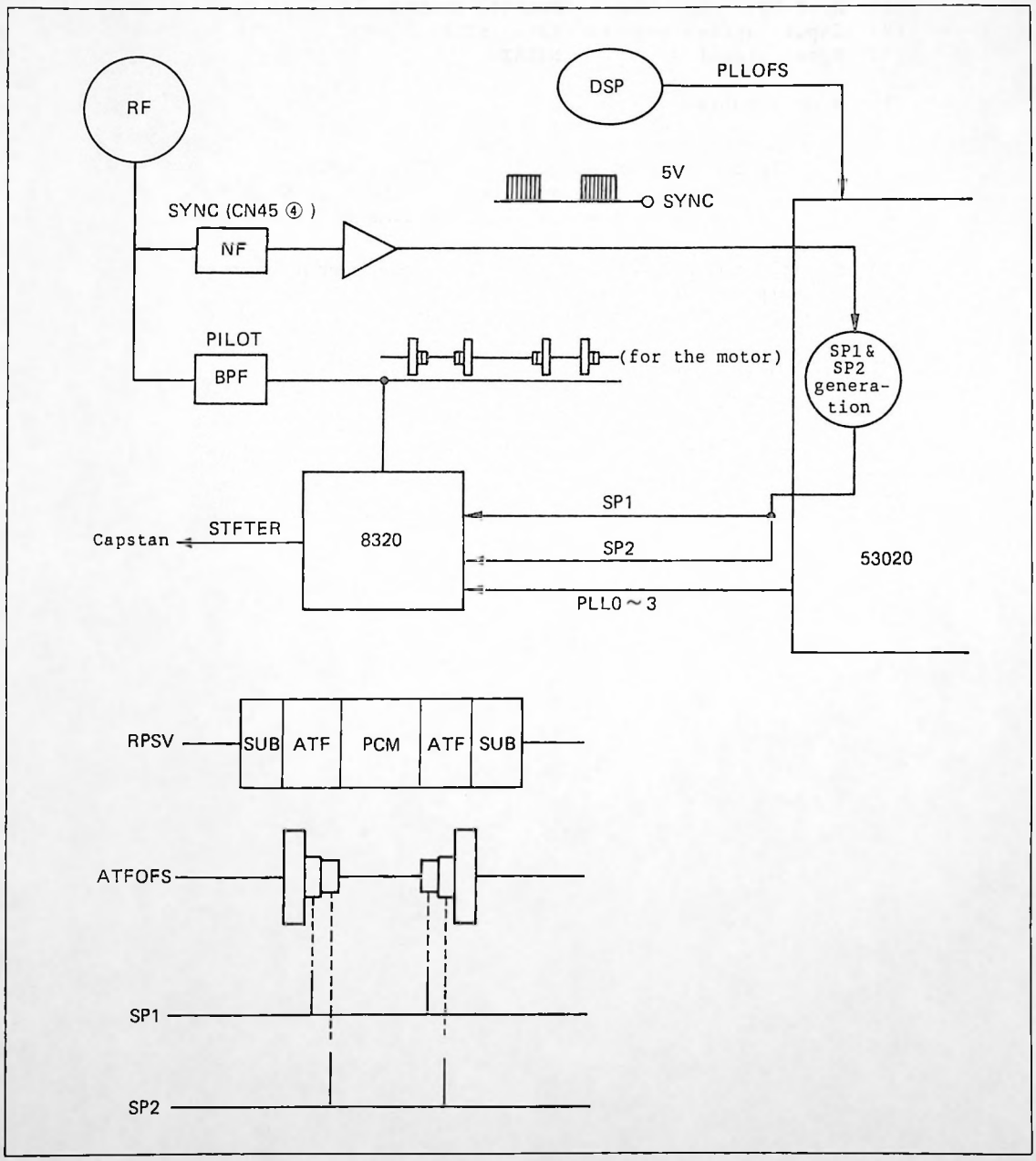
(1) Continues to move at x12.5 speed
- Is the reel FG output? (DRLFGT, DRLFGS)
- Are SELA and SELB switched? (SELA = L, SELB = H)
- Is the tape defective? Badly damaged?

(2) Erratic rotation in ff/rew: Time code cannot be read
- Is the reel FG output?
- Is the reset signal normal?

(3) Tape jamming display is shown (EXXOA).
- Is the reel FG output?

4) ATF System

The ATF system controls the head to keep it on track during play, obtains the pilot signal from the RF using the SYNC signal and activates the servo.



The difference of ATFOFS sampled with SP1 and SP2 is output to the capstan system as ATFTER.

<Applicable Signals>

(1) ATF error signal: ATFTER, ADIN
(2) Sampling pulse: SP1, SP2
(3) SYNC signal: SYNC
(4) ATF offset signal: ATFOFS
(5) ATF pilot signal: PILOT
(6) AD switching signal: TP62

<Types of Trouble>
Grinding sound (with a long period) is heard during play.

(1) Is the tape ok? (Bad spots?)
Check for scratches.
(2) Is the cassette seated properly?
Is foreign matter or paper attached to the outside of the cassette?
(3) Does the envelope flow?
Peak to peak level changes irregularly.
(4) Is ATFOFS output?
(5) Is the SYNC signal output?
(6) Are SP1 and SP2 output with correct timing?
(7) Are the ATFER and ADIN signals output?
(8) Is the PILOT signal properly output with correct timing?
(9) When the tray is turned on and off, does the AD switching signal go high and low?

5) Mode Motor System

Troubles relating to the mechanism mode transitions are summarized.

<Applicable Signals>
(1) Mode motor power supply: +12 V, AN6607
(2) Mode motor output: MDMTR (+), (-)
(3) Mode motor command: MODMT1-3

<Types of Trouble>
(1) No mode transition
° Is the mode motor power supply's +12 V ok?
° AN6607 output voltage ok?
° MDMTR (+), (-) ok? (Including rotational direction)
° Is the unit mechanically locked?
Note:
If the mechanism switching lock error display (E-XX01) is shown and the mechanism is locked, the mode motor, IC272 and Q271 may be damaged. Therefore, replace the mode motor, IC272 and Q271 at the same time.

(2) Mode motor overruns and does not stop.
° Rotational direction ok for MDMTR (+), (-)?
° Does the mode motor output change properly?

6) Cassette Loading System

<Applicable Signals>

(1) Cassette loading motor power supply: 12 V, TA7291S
(2) Cassette loading motor command: CLDMT (-), (+)
(3) Open signal
(4) Close signal
(5) Cassette hall signal: TH1, TH2
(6) Control command: LOAD0, LOAD1

<Types of Trouble>

(1) Open/close key does not function.
° Power supply 12 V ok?
° Command CLDMTR (-), (+) ok?
° Is command from mechanism control sent to TA7291S?

(2) Mechanism does not operate even if closed, immediately opens.
° Is close switch on?
If ok, check the mode motor system, tape or seating.

(3) Immediately closes if opened.
° Is open switch on?

(4) Click-click sound is heard after the cassette is inserted but loading is not performed.
° TH1 and TH2 turn on and off properly?

7) Tape Problems (includes EOT and BOT)

A defective tape may consist of the following items.

(1) Cut tape
(2) Does not move or excessive load from tape take up
(3) Reel lock from defective cassette hub brake
(4) Defective tape travel from tape damage
(5) Operational error from defective tape
° EOT and BOT not detected due to opaque leader tape
° EOT and BOT always detected due to transparent magnetic tape

Since the mechanism may be defective in (5), be sure to check the following items.
° EOT and BOT LEDs on?
° Turns on and off by blocking the light path?
° Adjusted properly? (VR271)

(6) Due to excessive tape load, the speed does not increase during FF/REW and the tape stops.
(7) Due to wide variations in tape load, an error code (EXXOA) is displayed and the tape stops.

3. Digital Section

3-1 Operation Overview

<When the Power is Turned On>

A reset signal (NRST1) is output from the reset IC (IC301: MN1281) and sent to the system control IC (IC301: MN188161SDS) to reset it when the power is turned on. The reset is cleared (NRST2) for the servo section (mechanism control), panel control (IC601: M50954) and signal processing IC (IC351: MN6624), 200 ms after the reset has been cleared at the system control.

<Normal Operation>

Operation commands from the panel key or remote controller are coded by the panel control (M50954) and transferred to the system control. The system control outputs various control signals to the servo section (IC271 in mechanism control), signal processing IC, clock oscillator, and analog section according to the operation commands to activate operations (e.g. for playback or recording). The system control monitors the operations of the various sections and outputs display data (NPRDY, PRXD, PCLK) to the panel control.

<Playback Operation>

During playback, the data (PBDT) recorded on the tape enters the signal processing IC through the RF section. At this time, a clock (PBCK) is extracted from the data in the RF section which also simultaneously enters the signal processing IC.
The signal processor receives a command from the system control and performs decoding. In the decoding process, a basic check based on the parity signal in the playback data is first performed. This check is monitored with the IDP signal. Furthermore, error correction is performed based on the error correction signal in the playback data and the corrected signal is output to the DA converter. At the same time, subcode data is separated from the playback signal and sent to the system control for use in the A-TIME and PNO displays.
The system control reads FS from the data on the tape and controls the clock oscillator according to its frequency.

<Recording Operation>

During analog recording, the digitized data signals (ADDAT, ADMCK, ADBCK, ADLRCK) from the AD converter are output to the signal processor to which an error correction signal generated at the signal processor and subcode data generated at the system control are added to generate the recording signal. The RF record-play switching signal (SRPR) is controlled and the recording signal (SRRF) is output to the RF section and recorded onto tape.
During digital recording, the system control controls the digital-in PLL section (IC357: M5238 and surrounding), inputs digital signals and performs the same process as during analog recording. Furthermore, the system control controls the clock oscillator, selects the clock generated at the digital-in PLL circuit and supplies it to the signal processor and analog section.

<Search Operation (including FF and REW)>

Basically the same as the playback operation except that error correction is not performed since the playback sound is not required. Only the subcode is extracted which the system control uses to implement the functions (e.g. program playback).

3-2 Detailed Operation of Each Section

<Reset Circuit>

The voltage detection IC (IC302: MN1281) generates a reset signal (NRST1) which is output to the system control while the power supply drops when turned on and off. (0 V during reset) While this reset signal is being input, the system control stops operation and all terminals enter a high-impedance state. At this time, the reset signal (RST2) for the signal processor and panel control goes high from resistor R301, and is inverted by transistor Q301. The low-level reset signal is supplied to the signal processor and panel control to reset them.
The power supply voltage rises, the voltage detection IC clears the reset signal (NRST1) to the system control and the system control begins operation. The reset state for the signal processor and panel control is cleared and normal operation begins 200 ms after the system control begins operation.
The reset signal (SEVRST) for the servo section is inverted by a transistor at the servo section. Otherwise, it is the same as the reset signal to the signal processor.

<Clock Oscillator>
(Refer to Fig. 1)

The crystal oscillations at 24 MHz, 22 MH and 16 MHz (512xFS) which are the master clocks for the AD and DA converters are performed at IC361. The system control activates or stops the oscillation through transistors Q315 and Q314.
The clocks generated here are supplied to the signal processor. One frequency is selected by the system control through IC363 and supplied to the DA converter. IC363 also selects crystal oscillation or digital-in PLL. Basically the crystal for the frequency corresponding to FS is oscillated during playback and other oscillation circuits including the digital-in PLL are stopped. During analog recording, only the 24 MHz crystal oscillates while the others do not. During digital recording, all crystals oscillate and the digital-in PLL also operates. Although the oscillation frequency of the digital-in PLL is normally selected and used, the frequency of the crystal is selected if the digital-in is not connected or does not lock.
This FS clock is used as the master clock for the DA converter. It is also divided in the signal processor and becomes the R3CP signal which is used as the cylinder rotation reference signal and system synchronization signal. Therefore, if there is trouble in this oscillation, it results in trouble in the DA converter's output and prevents the cylinder from synchronizing.
Besides this clock oscillator, an oscillation circuit for 28 MHz is found in the signal processor. This frequency is used to generate the recording signal in the signal processor and the divided clocks (M9CK, HFCH, FCH) are supplied to the servo section.

In addition, each microcomputer has its own self-oscillation clock.

<Digital-Out and Digital-In PLL Section>

(Refer to Fig. 2)

During digital recording, the signal (RX) from digital-in is directly output from digital-out by the control signal (pin 62) of the system control through IC358. At any other time, the output signal (TX) of the signal processor is output.
During digital recording, the signal (RX) from digital-in enters the signal processor and its phase difference with the clock (D512) of the digital-in PLL is detected. The phase difference outputs (DIOREF, DIOVAR) are sent to the low-pass filter (IC357) of the digital-in PLL. A control signal for the VCO consisting of a varicap (D351) and transistor (Q353) is produced from the phase difference signal at the low-pass filter. The oscillation signal of the VCO is waveshaped by IC359 and output to the signal processor (D512). If the digital-in PLL unlocks at this time, this is detected in the signal processor and the unlock signal (DUNLOK) is output. Using this signal, the digital-in signal (RX) is turned off by IC359. After this, the unlock information is transferred from the signal processor to the system control. The system control switches the clock to crystal oscillation and turns on transistor Q352 using the control signal DISCHG to discharge the PLL circuit. After the discharge operation, transistor Q352 is again turned off and the digital-in signal (RX) is passed through IC359 using the control signal UNLOK. After 200 ms, the control signal UNLOK is restored to its original state. If the PLL is locked, the operation for normal digital recording is performed. If the PLL is not locked, the same discharge operation which was performed when the first unlock occurred is repeated. At this time, the digital display on the panel flashes.
In any state other than digital recording, the digital-in PLL circuit (VCO) is stopped by the control signal DPLINH from the system control.

<Analog Section>

Data (DADAT) for the playback sound or monitor sound and clock signals (DALRCK, DABCK, DAMCK) which are sent from the signal processor to the DA converter are converted to analog signals and output from the SV-DA10. During analog recording, clocks (ADLRCK, ADBCK, ADMCK) from the signal processor are sent to the AD converter. The data (ADDAT) converted to a digital signal is sent from the AD converter to the signal processor.
A muting signal (SGMUT or SGM) from the system control is sent to the analog section to actuate the mute relay.
When the signal being played back is emphasized, the system control reads the emphasis information from the subcode and sends a control signal (DEMPH or DEM) to the analog section.
When cue or review is performed during shuttle operation, the system control lowers the level in the signal processor and sends a control signal (ATT) to the analog section to cut off the high frequencies in the playback sound.

3-3 Data Transfer in Each Section

<Between Panel Control and System Control>

Operation commands based on panel keys and remote controller receive data are sent from the panel control to the system control. FL and LED display data are sent from the system control to the panel control.
Transfers between the panel control and system control are performed serially using the control signal PRDY, data signals (PRXD, PTXD) and clock signal (PCLK). The transfer timing chart is shown in Fig. 3.
Between System Control and Signal Processor
Mode information such as record-play switching and commands such as data selection are sent from the system control to signal processor. During recording, the subcode data generated by the system control is also sent to the signal processor.
Subcodes extracted from the data on the tape and playback and recording level data are sent from the signal processor to the system control.
Transfers between the system control and signal processor are performed on an 8-bit bus using control signals (SPSTB, SPAW, SPRDY) and data signals (SPDT0-7). The transfer timing chart is shown in Fig. 4.

<Between System Control and Servo (mechanism control)>

Mode select commands (e.g. play, ff) and speed commands are sent from the system control to the servo. Status information consisting of the current mode, speed and cassette detect is sent from the mechanism control to the system control.
Transfers between the system control and servo (mechanism control) are performed on a 4-bit bus using control signals (NMSTB, NMRDY) and data signals (MDT0-3). The transfer time chart is shown in Fig. 5.

Error Rate
If the error rate is normal, the system until the signal processor is normal. In other words, it can be assumed that the transport for the RF head mechanism is normal.
Therefore, if the playback sound is abnormal and the error rate is normal, the problem may be in the analog system.
If the head's error rate is extremely poor, the problem may be in the RF head switching or in one of the heads.

Level Meter
Like with the error rate, if the level meter operates normally, it is clear the signal reaches the signal processor.
In other words, if the level meter is normal during playback, it is clear the mechanism, head and RF section are outputting the signal.
If the level meter is normal during recording, it is clear the analog section (input amplifier, AD) is functioning normally.

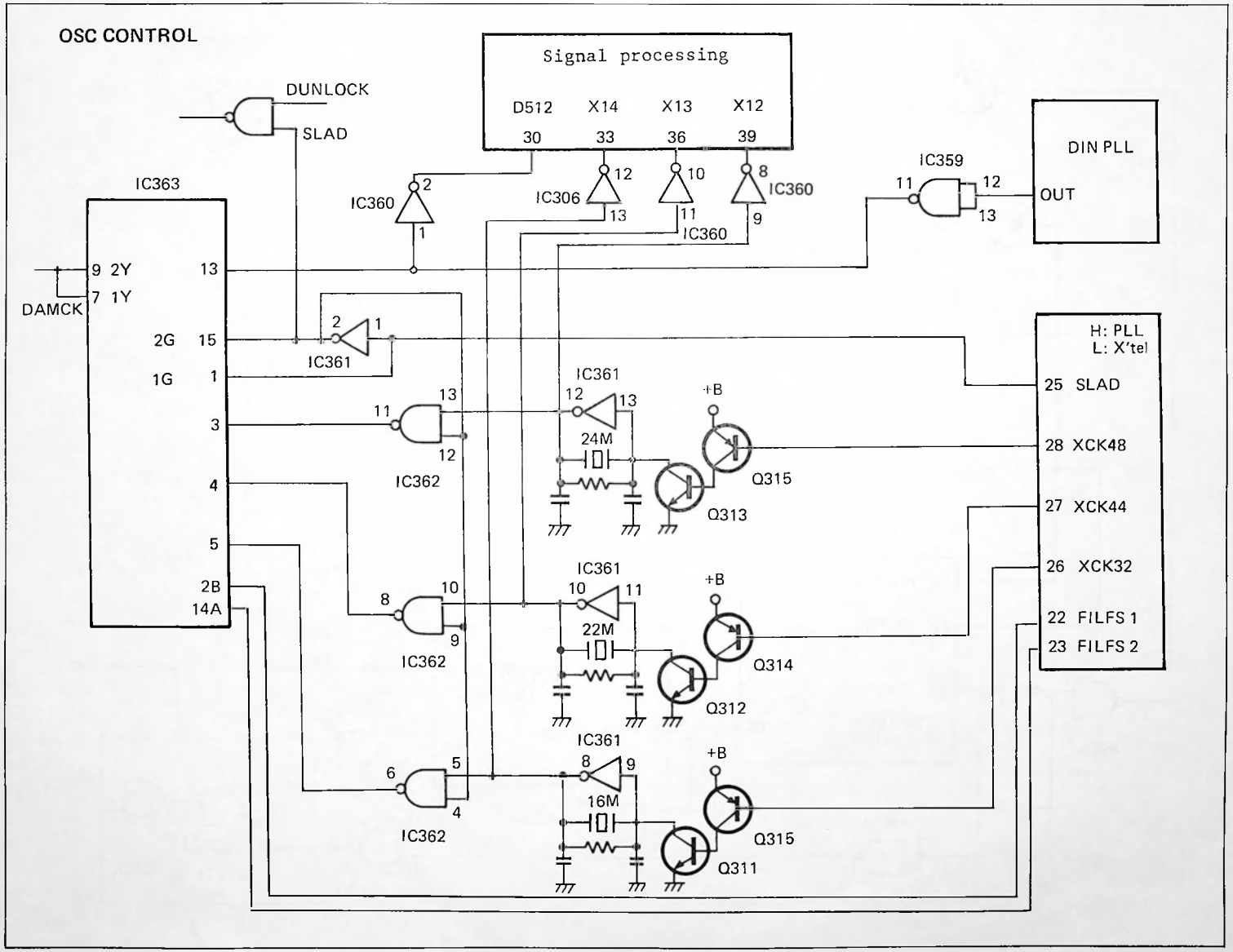

OSC CONTROL
Signal processing
D512 X14 X13 X12
30 33 36 39
DUNLOCK
SLAD
IC363
IC360
IC306
IC360
IC360
IC359
DIN PLL
OUT
9 2Y
7 1Y
DAMCK
2G
1G
IC361
IC362
IC361
24M
Q315
Q313
+B
IC362
IC361
22M
Q314
Q312
IC362
IC361
16M
Q315
Q311
H: PLL
L: X'tel
25 SLAD
28 XCK48
27 XCK44
26 XCK32
22 FILFS 1
23 FILFS 2

Fig. 1

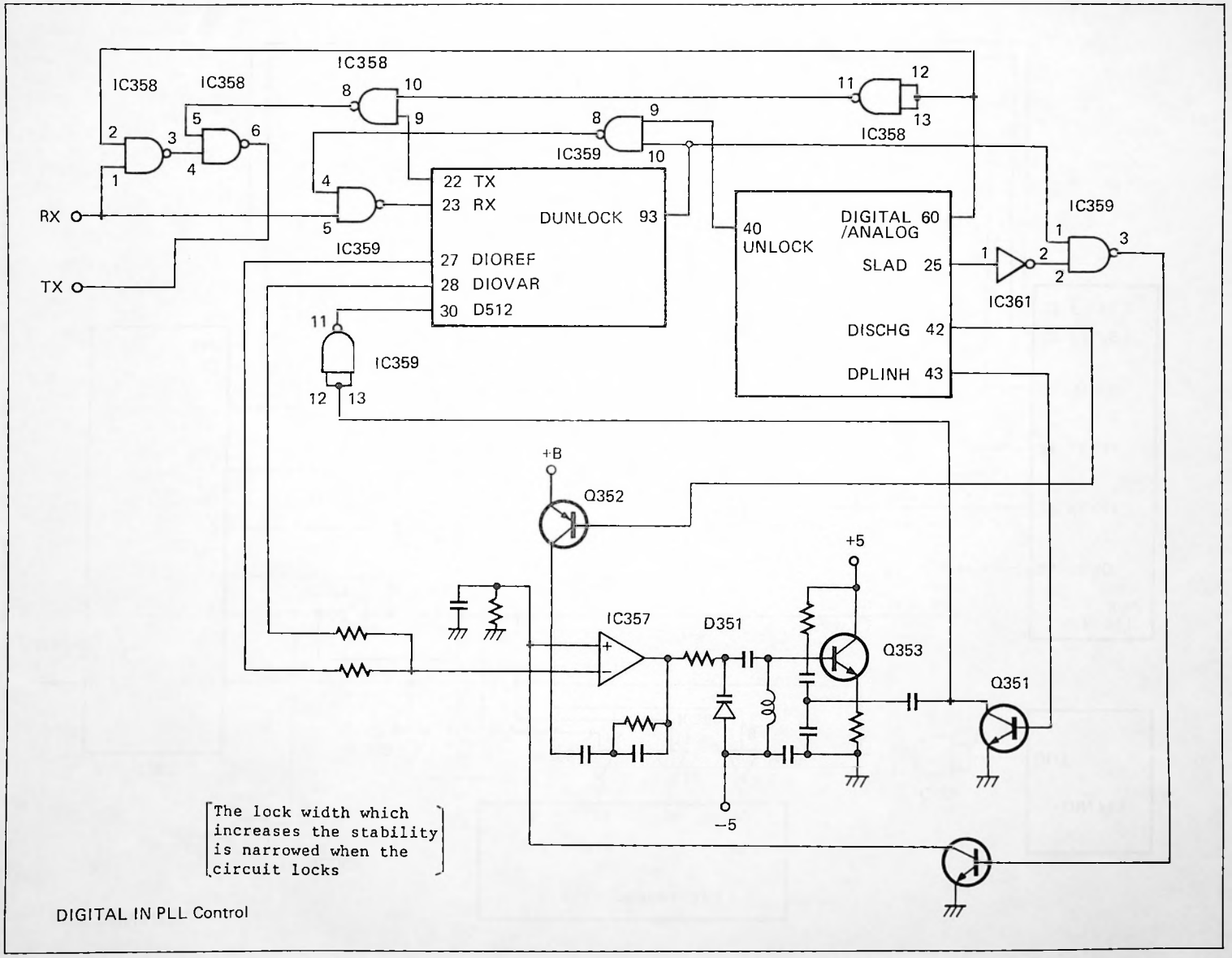
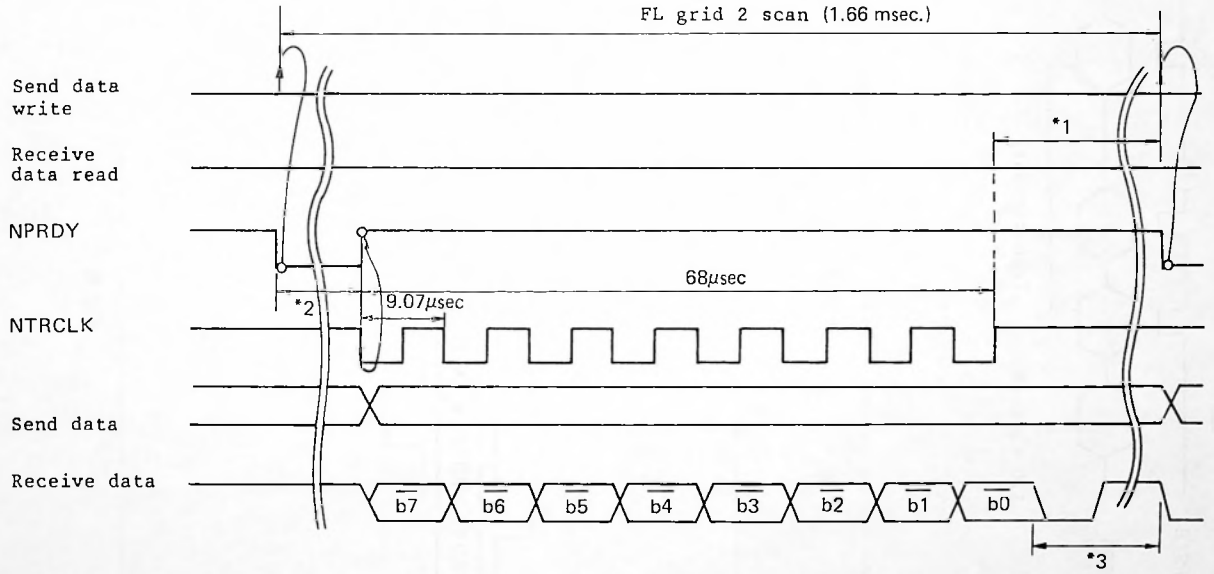

IC358
IC358
IC358
IC358
IC359
IC359
IC359
IC359
IC361
RX
TX
22 TX
23 RX
DUNLOCK 93
27 DIOREF
28 DIOVAR
30 D512
40 UNLOCK
DIGITAL 60 /ANALOG
SLAD 25
DISCHG 42
DPLINH 43
+B
Q352
+5
IC357
D351
Q353
Q351
−5
The lock width which increases the stability is narrowed when the circuit locks
DIGITAL IN PLL Control

Fig. 2

Serial Data Transfer Data Bit Format and Handshaking Procedure



*1: Receive data must be read at this interval.
*2: To create the interval in *1, adjust it at the system control to within 1 ms.
*3: The receive waveform during this interval may differ from that shown in the figure.

Fig. 3

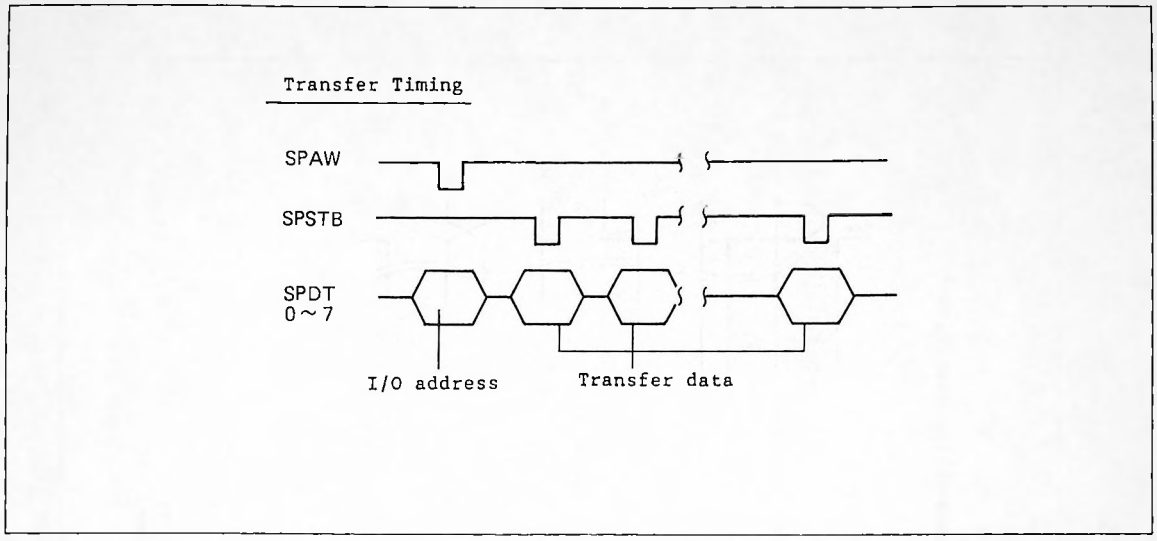

Transfer Timing
SPAW
SPSTB
SPDT
0 ~ 7
I/O address
Transfer data

Fig. 4

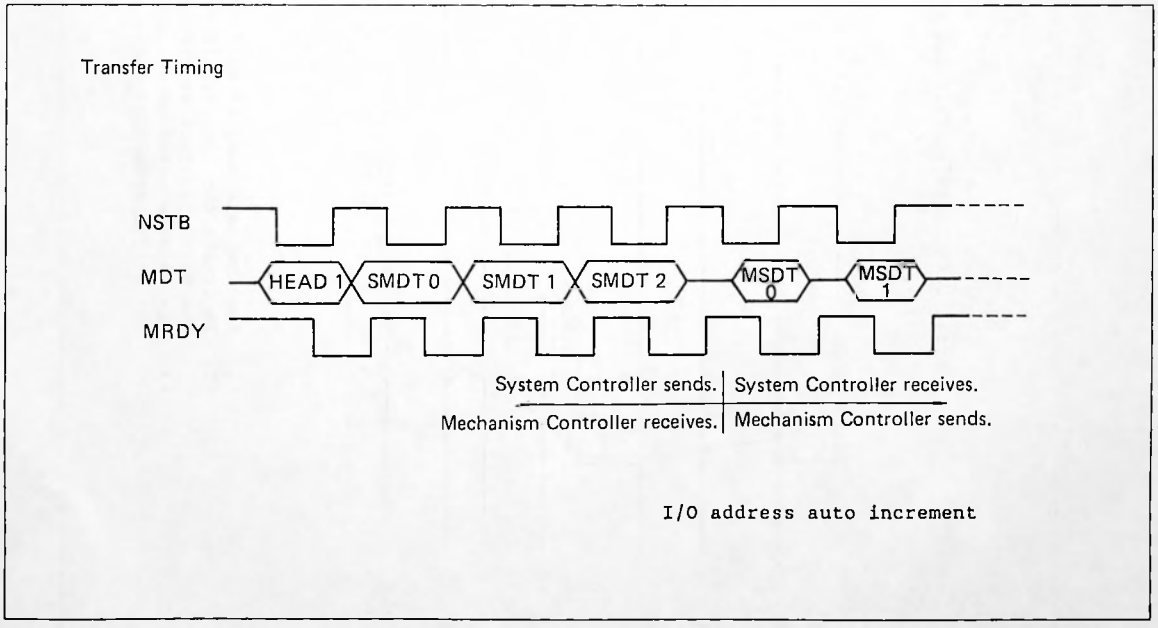
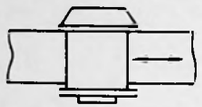

Transfer Timing
NSTB
MDT
MRDY
HEAD 1
SMDT 0
SMDT 1
SMDT 2
MSDT 0
MSDT 1
System Controller sends.
System Controller receives.
Mechanism Controller receives.
Mechanism Controller sends.
I/O address auto increment

Fig. 5

4. Hints for Tape Transport Mechanism Adjustment

Adjusting Post Roller on Entrance Side

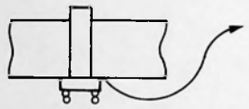


This roller should limit the upper edge of tape in the PLAY, CUE, or REView modes. The roller surface should be clean of dust or debris.
(The roller should not limit the lower edge of tape at the beginning of tape running at x1 or x15 speeds in the REView mode.)

If tape transport linearity on the entrance side does not settle in the specified time interval, the post roller will limit the lower edge of tape.

(1) Adjust S-guide post.
(2) Adjust S-fixed guide post.
(3) Check S-post roller base's contact.
(4) Check for lowered back tension in the Play mode.

Adjusting S-Fixed Guide Post

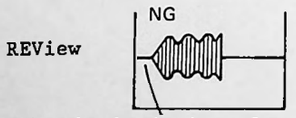


This guide post should limit the lower edge of tape. (The lower edge of tape should lightly touch the post's lower flange).

This is effective for improving linearity settlement on the entrance side during transition from loading into PLAY.

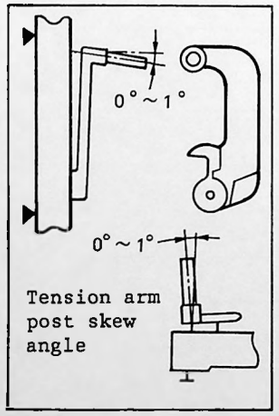
Adjusting S-Guide Post

Using the entrance-side guide post height adjusting jig, adjust the post's lower flange height. For this adjustment, normalize the jig's master gauge reading of 5.10 mm to zero.



At the beginning of tape, the envelope on the entrance side must be observed.

In case of NG, verify that the post roller skew angle is 30' ±15'.



Adjusting Tape Transport Linearity

Ideal linearity:

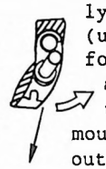
Tape Transport Linearity Settling Interval

(1) Loading ⇨ PLAY	Linearity must settle within ±3 µm in less than 3 seconds.
(2) REView ⇨ PLAY	
(3) STOP ⇨ PLAY	

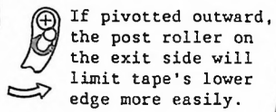
Lead

Tape should be stably guided in the PLAY or REView mode.

T-Inclined Base



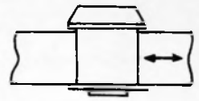
Pivot slightly outward (use the jig for final adjustment) until the mounting area outline on the chassis is slightly hidden.



If pivotted outward, the post roller on the exit side will limit tape's lower edge more easily.

If pivotted inward, the self record/play envelope will be obtained more easily.

Adjusting Post Roller on Exit Side



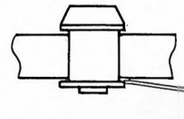
This roller should limit the upper edge of tape in the PLAY, CUE, or REView modes. The roller surface should be clean of dust or debris.

If tape transport linearity on the exit side does not settle in the specified time interval, the post roller will limit the lower edge of tape.

(1) Adjust T-guide post.
(2) Verify that the T-inclined base is pivotted slightly outward.
(3) Check for pinch roller shaft skew and T-fixed post shaft skew.
(4) Check for lowered back tension in the REView mode.

The tape should not be twisted in the REView mode. Correctable by adjusting T-guide post height.

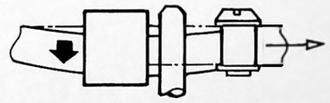
Adjusting T-Guide Post



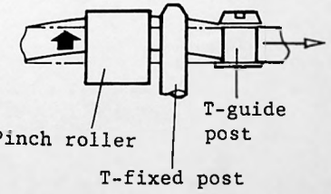
Adjust this guide post so it will limit the lower edge of tape, with a slight clearance between the tape and lower flange.
Leave a slight clearance here.

Remove tension regulator.

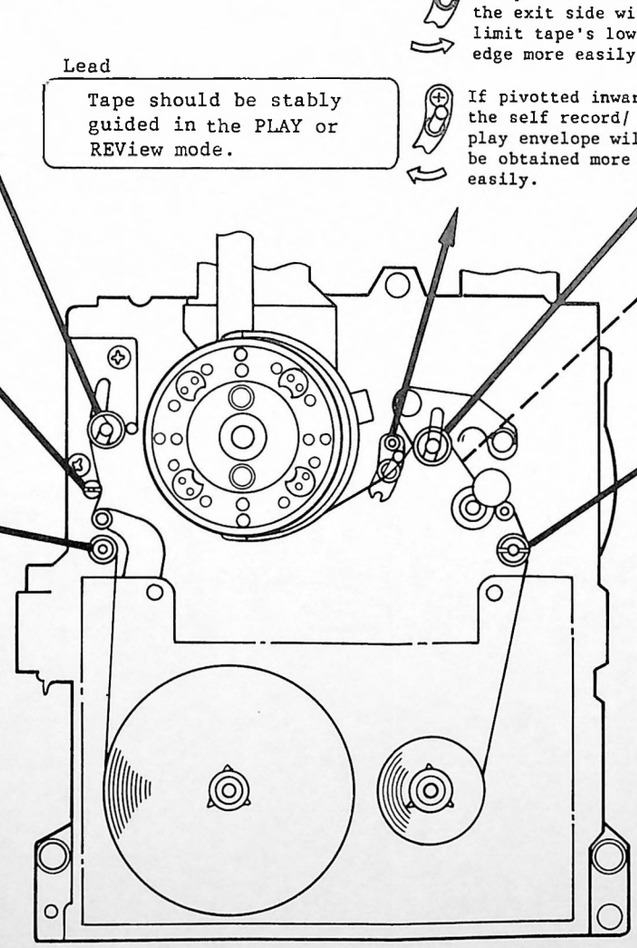
At x15 speed



If the tape slips downward, turn the T-guide post clockwise to lower it.



If the tape slips upward, turn the T-guide post counterclockwise to raise it.



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12. Name of Signal and Description

SIGNAL	DESCRIPTION		CIRCUIT
A IN	Analog In	IC-405 24 Pin	AD Converter
AG	Analog Ground	IC-405 23 Pin	AD Converter
AVDD	Analog VDD (5 & 12 Volt)		
A5RF	Analog 5 Volt	CN45 1 Pin	SERVO → RF
ATFSYNC	Auto Track Finding Sync Signal	CN45 4 Pin	RF → SERVO
ADDAT	Analog to Digital Data	IC-351 18 Pin	DSP
ADLRCK	Analog to Digital L/R Select Clock (fs)	IC-351 19 Pin	DSP
ADBCK	A/D Serial Bit Clock (32fs)	IC-351 20 Pin	DSP
ADMCK	A/D Master Clock (512fs)	IC-351 21 Pin	DSP
ADC	Analog to Digital Converter		
ATFER	ATF Error Signal (After Amplitued)	IC-201 35 Pin	SERVO
ATFTER	ATF Error Signal (Original)		
ATFSYNC	ATF Sync Signal		
ATT	Attenuation		
ANRST	Analog Rest Signal		
APNO	Auto Program Number		
BCLK	Bit Clock (32fs)	IC-405 5 Pin	DSP → ADC
BOT	Beginning of Tape		
CLOCK	Clock	IC-201 4 Pin	SERVO
CAPFGT	Capstan Motor FG Signal and Take-up		
	Reel FG Signal		
CAPER	Capstan Rotation Direction	IC-202 43 Pin	ATF
CAPEC	Capstan Error Signal	IC-204 16 Pin	SERVO
CAPED	Capstan Direction	IC-204 11 Pin	SERVO
CYLEC	Cylinder Error Signal	IC-205 16 Pin	SERVO
CYLED	Cylinder Direction	IC-205 11 Pin	SERVO
CAPVS	Capstan Voltage Control Command	IC-204 17 Pin	SERVO
CAPM1-3	Capstan Amateur Coil 1 - 3		
CAPH1-3	Capstan Hall Element 1 - 3		
CYLH1-3	Cylinder Hall Element 1 - 3		
CYLM1-3	Cylinder Amateur Coil 1 - 3		
CYLPG	Cylinder Phase Generator Signal	IC-203 6 Pin	SERVO

SIGNAL	DESCRIPTION		CIRCUIT
CYLFG	Cylinder Frequency generator Signal	IC-203 6 Pin	SERVO
CAPFG1&2	Capstan Frequency Generator 1-2 Signal	IC-203 2 Pin	SERVO
CAPFGTU	Capstan Frequency Generator or Take-up		
	Frequency Generator Sugnal	IC-201 37 Pin	SERVO
CLOSE	Close Signal		
D OUT	Digital Out (L/R Serial Data)	IC-405 39 Pin	AD Converter
DVDD	Digital VDD (5 Volt)		
DADAT	Digital to Analog Data	IC-501 36 Pin	DSP → DAC
DALRCK	Digital to Analog L/R Clock (32fs)	IC-501 34 Pin	DSP → DAC
DABCK	Digital to Analog Serial Bit Clock		
	(512fs)	IC-501 35 Pin	DSP → DAC
DUNLOK	Digital Input PLL Unlock Signal	IC-351 93 Pin	DSP
DINSEL	Digital Input/Analog Input Select		
	Signal		
DPLINH	Digital Input PLL Inhibit Signal	IC-301 43 Pin	SYSTEM
DIOVAR	Digital Input PLL Variable Signal	IC-351 28 Pin	DSP → PLL
DIOREF	Digital Input PLL Reference Signal	IC-351 27 Pin	DSP → PLL
DI512	Digital Input 512fs Clock Signal	IC-351 30 Pin	DSP → PLL
DAC	Digital to Analog Converter		
DSP	Digital Signal Prossesor		
DISCHG	Discharge	IC-301 42 Pin	SYSTEM
DRLFGT	Digital Reel FG Take-up Signal	IC-203 35 Pin	SERVO
DRLFGS	Digital Reel FG Supply Signal	IC 203 36 Pin	SERVO
DCYLPG	Digital Cylinder Phase Generator		
	Signal	IC-203 4 Pin	SERVO
DCYLFG	Digital Cylinder Frequency Generator		
	Signal	IC-203 27 Pin	SERVO
DCAPFG2	Digital Capstan Frequency Generator		
	2 Signal	IC-202 9 Pin	SERVO
DCAPFG1	Digital Capstan Frequency Generator		
	1 Signal	IC-202 8 Pin	SERVO
DCYLPG	Digital Cylinder Phase Generator 1		
	Signal		
DRLFGSU	Digital Reel Frequency Generator		
	Supply Signal	IC-201 55 Pin	SERVO

SIGNAL	DESCRIPTION		CIRCUIT
DRLFGTU	Digital Reel Frequency Generator		
	Take-up Signal	IC-202 10 Pin	SERVO
DIGTL	Digital Signal		
DEW	Dew Sensor Signal (Element)		
EXCLK	External Clock (24.576MHz)	IC-405 15 Pin	DSP → ADC
ENVT	Envelop "T" 66.6Hz (R3CP x 2Time)	CN43 13Pin	DSP → SERVO
EBLED	EOT/BOT Detection Signal		
EOT	End of Tape		
FILFS1-2	Sampling Frequency Select Signal		
	32KHz	IC-301 26 Pin	SYSTEM
	44.1KHz	IC-301 27 Pin	
	48KHz	IC-301 28 Pin	
FCH	Clock Frequency (M9CK)	CN43 14 Pin	DSP → SERVO
1G - 6G	Grid Signal		
HSW	Head Switching Signal	CN45 5 Pin	SERVO → RF
HFCH	Half Clock Frequency (4.7MHz)	CN43 16 Pin	DSP → SERVO
KR0 - 6	Key Return Signal (7 bit)		
LRCK	L/R Channel Select Signal	IC-405 4 Pin	DSP → ADC
LOADS	Tape Lording Start Signal		
LOADE	Tape Lording end Signal		

SIGNAL	DESCRIPTION		CIRCUIT
LOAD 0-1	Tray Lording Control Signal (2 bit)		
MDT 0-3	Mechanism Control Signal (4 bit)	CN44 9-12 Pin	SERVO → SYSTEM
M9CK	(FCH) Clock Frequency		
MRDY	Mechanism Ready Signal	IC-301 46 Pin	SYSTEM
MBUSS 0-3	Mechanism Control Data Buss	IC-301 53-56 Pin	SYSTEM
MMOD 1-3	Mechanism Mode Detection		
MODMT 1-3	Mechanism Mode Control Signal		
NRST	Negative Rest Signal		
NCS	Negative Chip Select Signal	IC-351 66 Pin	DSP
NOE	Negative Output Enable Signal	IC-351 63 Pin	DSP
NWE	Negative Write Enable Signal	IC-351 58 Pin	DSP
NSSDA	Negative Serial Servo Data		
NRTRST	Negative Rotation Rest		
NRST2	Negative Reset 2	CN43 11 Pin	SYSTEM
NSSTB	Negative Servo Processor Strobe	IC-201 20 Pin	SERVO
NRDY	Negative Servo Processor Ready	IC-201 3 Pin	SERVO
NSCLK	Negative Servo Processor Clock	IC-201 2 Pin	SERVO
NSRST	Negative Servo Processor Reset	IC-301 61 Pin	DSP
NLNROK	Negative Linearty OK Signal	IC-202 44 Pin	SERVO
NSNCOK	Negative Sync OK Signal	IC-202 1 Pin	SERVO
NCYLPG	Negative Cylinder Phase Generator		
	Signal	IC-201 36 Pin	SERVO
NRLFGS	Negative Reel Frequency Generater		
	Supply Signal	IC-201 55 Pin	SERVO
NDENP	Negative Deenphasis Control Signal		
NPRDY	Negative Panel Ready		
NMRDY	Negative Mechanism Ready		
NMSTB	Negative Mechanism Strobe		
NSERVRST	Negative Servo Reset		
NRST 1	Negative Reset 1		
NSPSTB	Negative DSP Strobe		
NSPAW	Negative DSP Address Write		

SIGNAL	DESCRIPTION		CIRCUIT
N1G - N6G	Negative Grid 1 - 6		
OPEN	Open Signal		
OFCLR	Clock Detection Terminal		ADC
PBDT	Playback Data	CN42 2 Pin	RF → DSP
PBCK	Playback Clock	CN42 4 Pin	RF → DSP
PLLOFS	PLL Offset Data (Serial Data)	CN43 17 Pin	DSP → SERVO
PRXD	Panel RX Data	CN30 3 Pin	SYSTEM
PTXD	Panel TX Data	CN30 2 Pin	SYSTEM
PILOT	Pilot Signal	CN45 3 Pin	SERVO
PLL 0-3	PLL Offset Data (Parallel)	IC-202 34-37Pin	SERVO
PCMOK	Playback PCM Data OK	IC-202 3 Pin	SERVO
PCLK	Panel Clock		
PILOT ATF	Pilot Auto Track Finding Signal	CN45 3 Pin	SERVO
RPRF	Reproduce RF Signal	TP101	RF
RFENV	RF Envelope	CN42 5 Pin	DSP
R3CP	Rotation Signal	TP301	DSP → SERVO
RDT 0-7	Ram Data 0 - 7	IC-351 68-75Pin	DSP
RAD 0-9	Ram Address Data 0 - 9	IC-351 45-52Pin	DSP
RX	Digital Interface Input	IC-351 23 Pin	DSP
R3TU	R3CP/Take-up Reel FG Signal	IC-201 31 Pin	SERVO
RLFGSU	Reel FG Supply	IC-203 32 Pin	SERVO
REWGT	Rew PG Amp Gain Control		
SRPR	DSP to RF and Play/Rec Selector	CN41 7 Pin	DSP → RF
SRRF	DSP to RF and RF Signal	CN41 8 Pin	DSP → RF
SRWND1	DSP to RF and Window Signal 1	CN41 9 Pin	DSP → RF
SRWND2	DSP to RF and Window Signal 2	CN41 10 Pin	DSP → RF

SIGNAL	DESCRIPTION		CIRCUIT
SLAD	Selector (Analog/Digital)	IC-301 25 Pin	SYSTEM
SPDT 0-7	DSP Data (Data Buss)	IC-301 2-9 Pin	DSP
SPRDY	DSP Ready Signal	IC-301 10 Pin	DSP
SYNC	ATF Sync Signal	CN45 4 Pin	RF ⟶ ATF
SELAB	A and B Select	IC-201 13 Pin	SERVO
SVAL	ATF Select Signal	IC-202 1 Pin	SERVO
SP1	Sample Hold Pulse 1	IC-203 12 Pin	SERVO
SP2	Sample Hold Pulse 2	IC-203 13 Pin	SERVO
SPE	Sample Hold Pulse Error	IC-203 15 Pin	SERVO
SELB	Select B	IC-201 13 Pin	SERVO
SELA	Select A	IC-201 12 Pin	SERVO
SGMTG	Signal Muting Control		
S1 - S26	Segment Data		
SRDATA	Serial Data	IC-501 36 Pin	DAC ⟶ DSP
TX	Digital Interface Output	IC-351 22 Pin	DSP
TH1-2	Tape Hole Detector 1 and 2		
UNLOCK	PLL Unlocked Control Signal	IC-301 40 Pin	Main
VFPLFS	Validity of PLLOFS Signal	CN43 15 Pin	DSP ⟶ SERVO
VM	Voltage Supply for Capstan Motor		
XCK32	Xtal OSC Master Clock of 32KHz	IC-301 26 Pin	SYSTEM
XCK44	Xtal OSC Master Clock of 44.1KHz	IC-301 27 Pin	SYSTEM
XCK48	Xtal OSC Master Clock of 48KHz	IC-301 28 Pin	SYSTEM
XI1	Xtal Input (28MHz)	IC-351 42 Pin	DSP
XI0	Xtal Outpot	IC-351 41 Pin	DSP
XI2	Xtal Input (24MHz)	IC-351 39 Pin	DSP
XI3	Xtal Input (22MHz)	IC-351 36 Pin	DSP

SIGNAL	DESCRIPTION	CIRCUIT
XI4	Xtal Input (16MHz) IC-351 33 Pin	DSP
ZFLGB	Digital Zero Detection Signal IC-501 31 Pin	DA Converter

— MEMO —

13. Reference

1. An Audio Section Designed for the Recording and Playback of Minute Signals

2. Newly Developed ø30 Cylinder Mechanism

3. Newly Developed DAT LSI System

4. Shuttle Search

5. Hyper Memory Search

6. Newly Developed Single-Chip LSI Signal Processor

The advent of various digital equipment such as CD players, broadcast satellite tuners, amplifiers with built-in DAC, surround processors and DAT has broadened the range of digital sources for digital audio, thus welcoming the age of serious digital audio. Among these, DAT, with functions to record and play back various digital sources and analog sources, is expected to play a central role in the audio equipment scene. Furthermore, it has been three years since the introduction of DAT, and its technical maturity and the adoption of SCMS have finally introduced DAT to the consumer market. Since the development of DAT, Panasonic has compiled its accumulated storehouse of technology and know-how, and revamped all the necessary technologies for the mechanism, LSI devices, software and audio circuitry to develop a new second-generation DAT deck.

1. An Audio Section Designed for the Recording and Playback of Minute Signals

1) MASH 1-bit ADC

For a DAT recorder, one must not forget the obvious: once music has been recorded, the quality of the playback audio cannot be expected to surpass the recording performance, no matter how high the performance of the playback equipment.
The MN6460 MASH 1-bit ADC is designed to correctly convert the minute signals included in the input signal to digital data.

Fig. 1 shows the block diagram of the MN6460 MASH 1-bit ADC which consists of an A/D converter section and a decimation digital filter section. The A/D converter section comprises a MASH quantization circuit containing 1-bit noise shaping quantizers in three cascaded stages.

The analog signal which is input by the MASH 1-bit ADC is quantized at the A/D converter section using 64-times oversampling and converted to 4-bit digital data. The quantization noise generated in the first stage of the A/D converter section is requantized in the second stage, and in turn the quantization noise generated in the second stage is requantized in the third stage. Adding all the outputs, the quantization noises of the first and second stages cancel out each other, and only the quantization noise of the third stage which provides third-order noise shaping characteristics is added to the input signal and output. The first stage has a differential configuration to improve the anti-noise characteristics.

The output of the A/D converter section enters the digital filter section consisting of a first stage digital filter which has comb transfer characteristics and a 256-tap second stage digital filter. The first stage digital filter prevents loopback and performs 16:1 decimation, and the second stage filter performs 4:1 decimation and outputs 16-bit data for the normal sampling period.

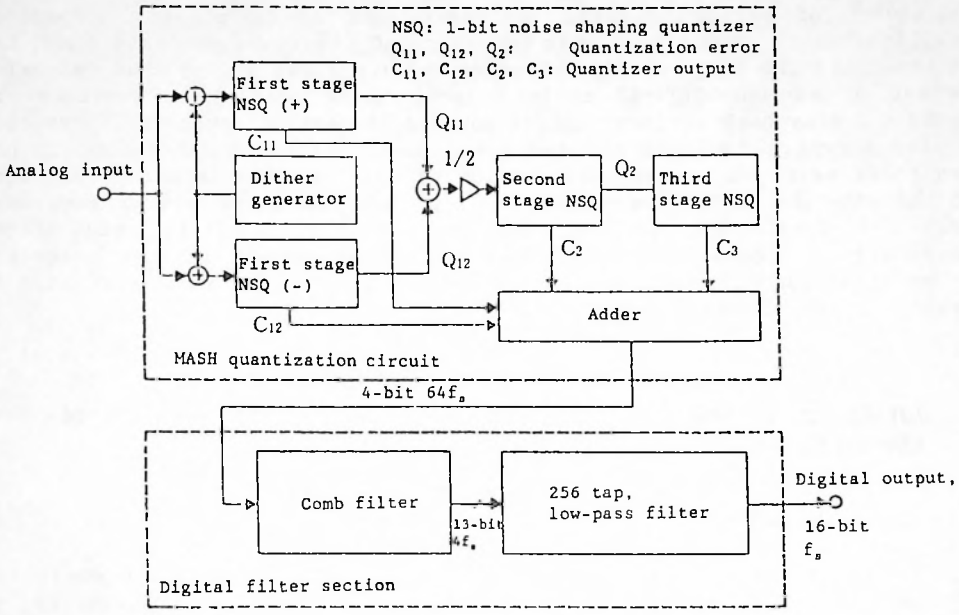


Fig. 1–1 MN6460 ADC Block Diagram

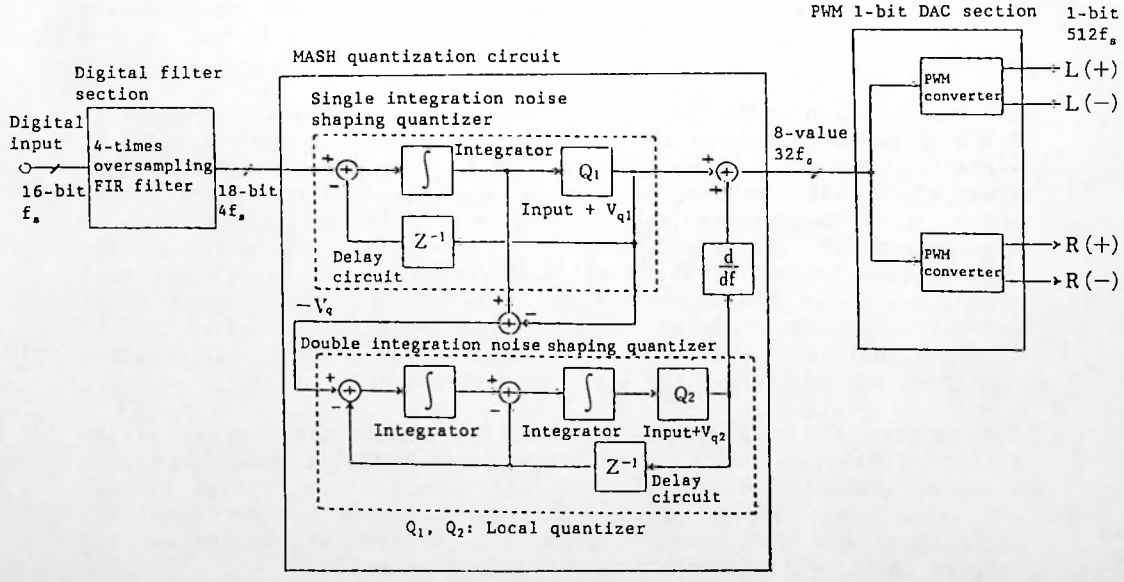


Fig. 1–2 MN6470 DAC Block Diagram

2) MASH 1-bit DAC

Panasonic already uses the MASH 1-bit technology in CD players and now uses the newly developed MN6470 for DAT applications. Fig. 1-2 shows the block diagram of the MASH 1-bit DAC which consists of an oversampling digital filter section, a MASH quantization circuit and a PWM (Pulse Width Modulation) 1-bit D/A section. The MASH quantization circuit comprises a single integration noise shaping quantizer and a double integration noise shaping quantizer connected in cascade.

The 16-bit digital data which is input by the MASH 1-bit DAC is output by the digital filter section as a 4-times oversampling 18-bit data. At the MASH quantization circuit, it is subjected to third-order noise shaping and then bit compressed to a 32-times oversampling 4-bit data. At the PWM 1-bit D/A section, the 4-bit data is output corresponding to an 8-value PWM waveform. The output at this time is either high or low, or what is called a bit.

3) Separate Clock Circuits

Since the accuracy of the PWM output directly affects the characteristics in the MASH 1-bit DAC, the use of a clock with excellent time-axis accuracy becomes an extremely important factor.
It is necessary for DAT to simultaneously operate the sampling master clocks corresponding to the three sampling frequencies of 48 kHz, 44.1 kHz and 32 kHz, and the system clock which controls the overall system. When the oscillations for the system clock and sampling master clocks are performed using the internal circuitry of the signal processor LSI device as shown in Fig. 1-3, mutual interference between the clocks and data occur within the LSI device. This causes a sampling master clock to contain many frequency components as shown in Photo 1-1.

As a result, the noise level during playback is around -100 dB as shown in the -60 dB playback spectrum of Photo 1-2. In other words, even if high-accuracy quartz oscillators are used for the sampling master clock oscillations, the accuracy of a clock deteriorates when it is subjected to interference from the other clocks in the circuit before entering the DAC.

To eliminate this sort of interference from the other clocks, a separate clock circuit system is used in our DAT recorder which separates the sampling master clock oscillation circuit from the signal processor LSI device as shown in Fig. 1-4. Through this system, the interference from the other clocks and data is completely eliminated in the sampling master clock as shown in Photo 1-3 and the noise level in the -60 dB playback spectrum is improved by approximately 20 dB at the low frequencies as shown in Photo 1-4.

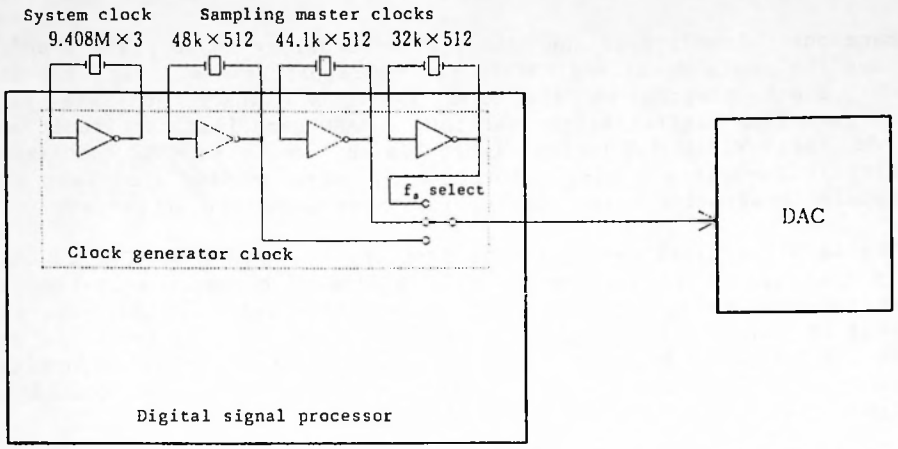


Fig. 1–3 Conventional Clock Circuit

4) Simplified Analog Circuits

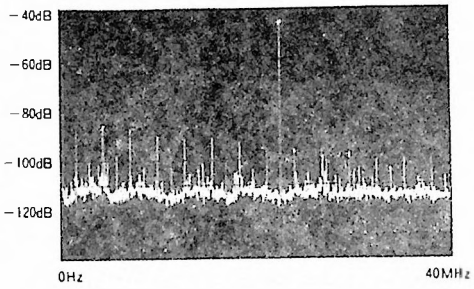
The use of the MASH 1-bit ADC/DAC eliminates the need for the sample and hold circuit and deglitch circuit which are indispensable in the conventional successive comparison ADC or ladder resistor DAC. Further, by performing a very high oversampling of 64 times or 32 times, the analog circuits connected to the front and rear of the ADC/DAC can be greatly simplified so that a third-order filter is sufficient for the analog low-pass filter.

Photo 1-5 compares the amplitude characteristics of the seventh-order low-pass filter for the 2-times oversampling successive comparison ADC and the third-order low-pass filter for the MASH 1-bit ADC. Compared to the steep amplitude characteristics of the seventh-order, the gradual amplitude characteristics of the third-order are sufficient and greatly improve the group delay frequency characteristics within the band.

5) Low-Distortion Overall Characteristics

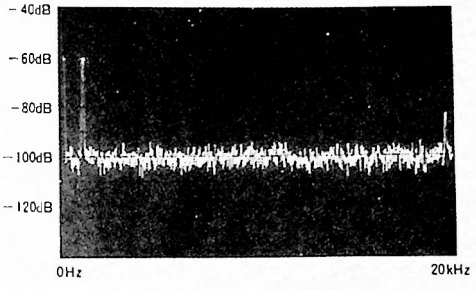
Due to non-uniform accuracy of each bit, the effect of the differential error increases as the signal level lowers in the conventional successive comparison ADC and ladder resistor DAC.
Photo 1-6 shows the overall -60 dB recording and playback spectrum from the combination of a successive comparison 16-bit ADC and our 4DAC 18-bit system. To eliminate the zero-cross distortion resulting from the MSB error, the MSB of the ADC is adjusted. However, many frequency components are generated and many errors are generated on the bits other than the MSB.

Photo 1-7 shows the overall -60 dB recording and playback spectrum produced by our DAT recorder. The high frequency components are about the same as the noise level and there are no bit errors of the conventional type from the MASH 1-bit ADC/DAC.
In this way, the effect of the MASH 1-bit ADC/DAC and its resulting simplified analog circuits enables our DAT recorder to accurately record and play back even the sound reverberations for minute signals. We have completely changed the prevailing image of digital audio equipment which was "it sounds digital" and now offer the enjoyment of soft and natural sounds which are much closer to those of analog equipment.



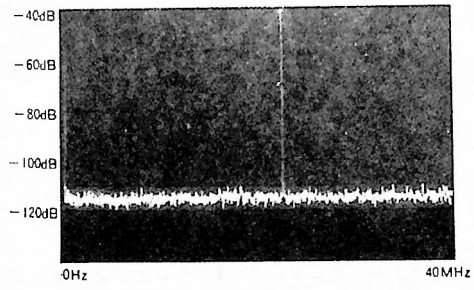
DAC input clock spectrum
(conventional clock circuit)

Photo 1—1



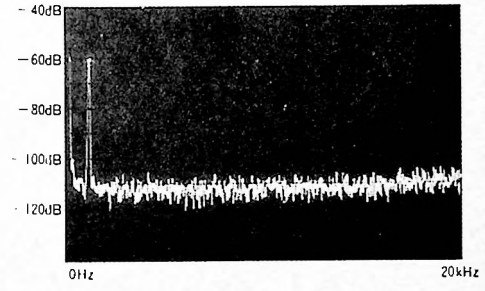
1 kHz -60 dB playback spectrum
(conventional clock circuit)

Photo 1—2



DAC input clock spectrum
(separate clock circuit)

Photo 1—3



1 kHz -60 dB playback spectrum
(separate clock circuit)

Photo 1—4

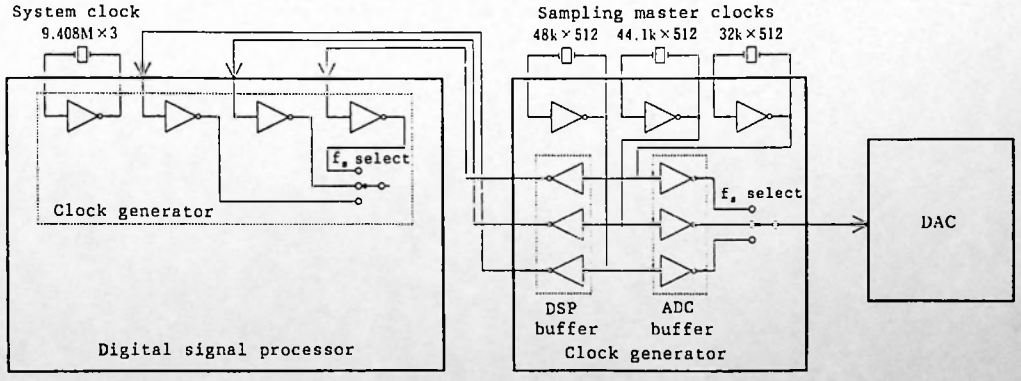
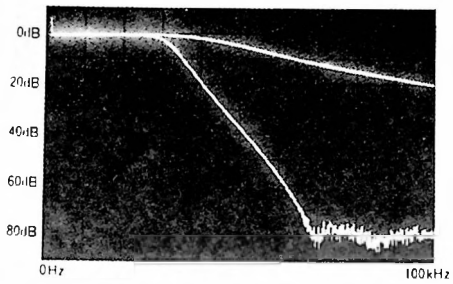


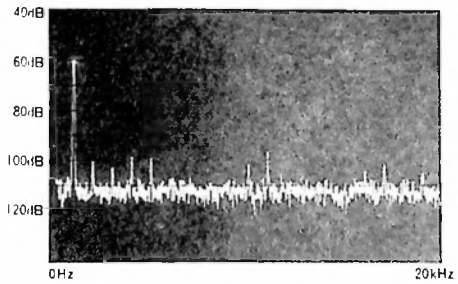
Fig. 1—4 Separate Clock Circuit



Low-pass filter amplitude characteristics

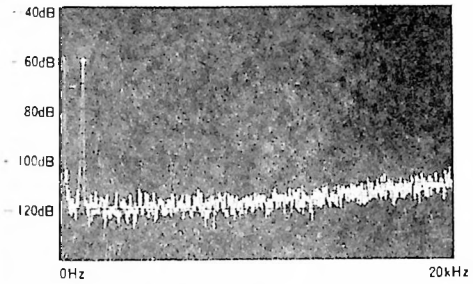
Top: Third-order
Bottom: Seventh-order

Photo 1–5



1 kHz -60 dB recording and playback spectrum (one example of conventional ADC/DAC)

Photo 1–6



1 kHz -60 dB recording and playback spectrum (our recorder)

Photo 1–7

6) Class AA Circuit and Carefully Selected Audio Parts

Unaffected by the influence of circuit load, the class AA circuit which performs ideal class A operation is used in the line out circuit. It performs faithful waveform transfers and greatly improves the audio quality in actual use.

The power supply circuit, dedicated for the audio circuit, is configured independently from the transformer winding, and high audio quality carbon-film resistors, high audio quality electrolytic capacitors, and film capacitors dedicated for audio use were selected from exhaustive auditions to reproduce musically rich sounds with low distortion and high clarity.

2. Newly Developed ø30 Cylinder Mechanism

From the precision and solid construction of our first DAT recorder, we have improved the accuracy, added advanced functions, and streamlined the design to achieve a high performance and high reliability mechanism with a ø30 cylinder. It features quick operation functions such as x400 tape travel and variable speed cue and review, and low noise design concepts.

1) Newly Developed ø30 Cylinder

The standard size ø30 cylinder incorporates the technologies for high reliability and low noise. A newly developed SSB (Sleeved Shaft Bearing/Silent Bearing) is used for the bearing, a key component of the rotating cylinder. It has a deflection precision of 2 μ or less which is half that of the conventional bearing, and permits high precision tracking.

Furthermore, vibrations have been successfully reduced to a minimum, and together with the improvement of the rotary balance from the use of a one-touch connector between the head and rotary transformer, it was possible to lower the noise considerably and achieve a quietness comparable to that of high-grade analog cassette decks. The SSB incorporates a bearing system which integrates the inner rings for the top and bottom bearings with the shaft and also integrates the outer rings with a rigid stainless steel sleeve. (Refer to Fig. 1-5.)

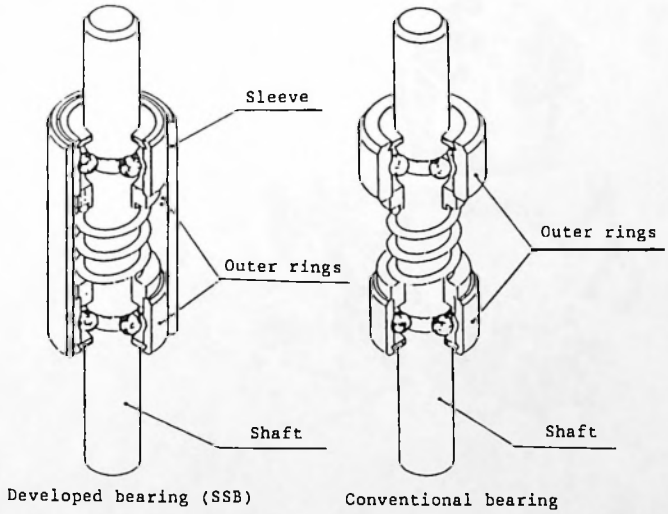


Fig. 1–5 Bearing Comparison (new and old)

2) New High-Precision Mechanism

The use of a precision aluminum die cast chassis resulted in high rigidity and high precision. This together with the fixed inclined post contribute to the improvement in the reliability of the tape transport mechanism. Efficient component placement based on the 2DD and 1DC motor drive achieves a compact and lightweight mechanism with 54% the volume and 45% the weight of our previous mechanism.

Furthermore, the low power consumption design in the high efficiency capstan motor incorporating a large rotor and small diameter capstan and in the all-gear low-load drive mechanism has resulted in a mechanism with a power consumption which is 1/2 that of our previous mechanism when compared during play. As a result, it offers the features of a standard mechanism which can be developed not only for stationary decks but also for car portables.

3) Super FF and REW at x400

The newly developed mechanism features an ultra high-speed drive with FF and REW speeds of x400. This was achieved by the effective use of adjustable speed optimization control and the air-film effect in the start and stop operations, and by the high-precision designs of the tape drive mechanism and guide rollers.
The large improvement in the access speeds enabled a 120-minute tape to be wound in approximately 27 seconds.

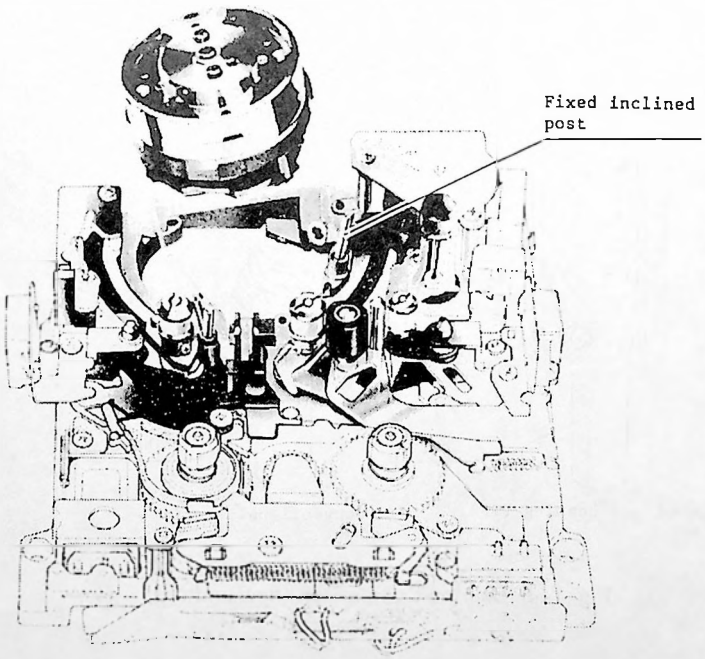


Photo 1–8 Mechanism and ϕ30 Cylinder

3. Newly Developed DAT LSI System

Along with the mechanism, the DAT LSI system was also redesigned. Fig. 1-6 shows the system block diagram of our DAT recorder. The LSI system features simplicity yet advanced functions and high performance in general-purpose applications.

Software Servo System

1) Servo Processor (MN6742)

The new generation of DAT servo systems incorporates a software servo system for adaptability to new models and for optimum control of the mechanism. The servo processor, the main control unit for the servo, uses a servo-dedicated 16-bit microcomputer (MN6742) which has demonstrated high performance and reliability in Panasonic VCRs. The use of this software servo system has resulted in software ATF control and the New CRV (Constant Relative Velocity) servo to produce the variable speed shuttle search and ultra high-speed memory search which our DAT recorder features.

2) Software ATF Control

The shuttle search requires a tracking servo which performs accurate head tracing for a wide range of tape speeds from a low of x1/2 to a high of x15.
Consisting of complex analog circuits assembled from many components, the conventional ATF control has the disadvantages of increased complexity and ambiguity when used to produce multiple speeds such as those in shuttle search.

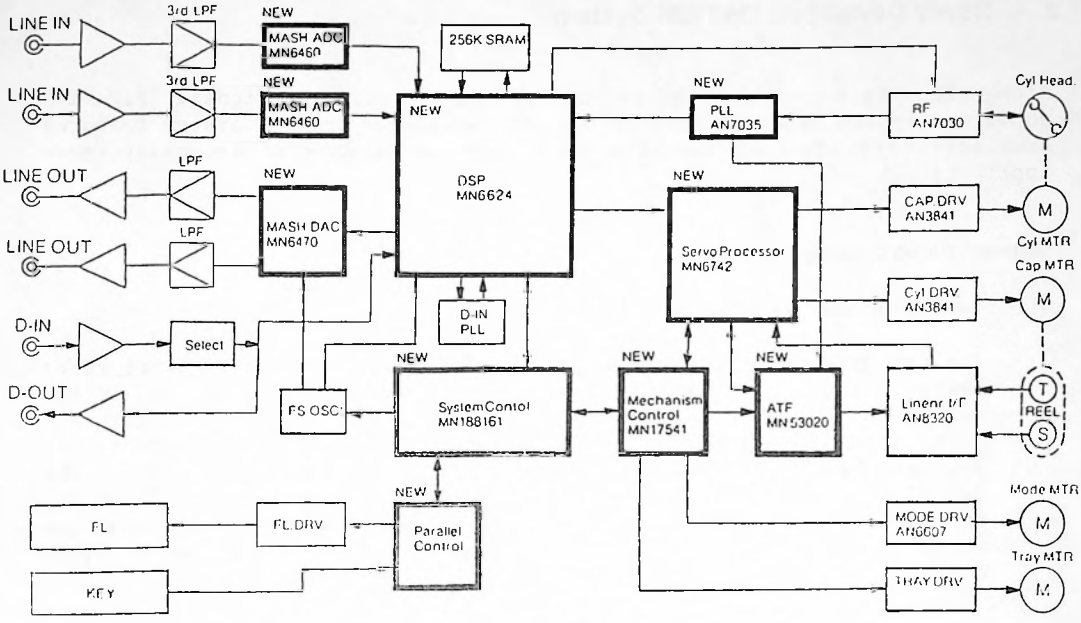


Fig. 1–6

The software ATF control system has been greatly simplified by incorporating the conventional servo circuit into the servo processor. Accurate tracking characteristics based on the software ATF control which performs digital operations and optimum tracking control for a wide range of tape speeds are achieved.

3) New CRV Servo

To correctly read the subcode data when a high-speed search, a DAT feature, is performed, the playback signal is given the same frequency as that during normal playback even at tape speeds over x200.
For this reason, the rotational speed of the cylinder during high-speed search is varied from less than 1/2 to more than 1.5 times the normal speed so that the relative speed between the head and tape remains the same as that during normal playback.
To achieve a higher reliability subcode search, smoother adjustable tape speeds and faster search speeds, the New CRV servo used in our DAT recorder introduces software control into the reel servo, increases the number of adjustable speed steps and optimizes the control characteristics.
Fig. 1-7 shows the mode transition diagram for the New CRV servo. Control data for the reel servo is created only once at the start of the search.

Next, the New CRV servo enters the search mode and sequential acceleration processing is executed. Compared to the conventional x200 speed, the speed has been greatly increased to x250 in normal search and to x400 in ultra high-speed search which is twice the conventional speed. Furthermore, the number of steps in the transition period process has also been increased from the conventional 6 steps to 19 steps, and the speed is controlled, not only during acceleration, but also during deceleration to achieve smooth reel servo operations.

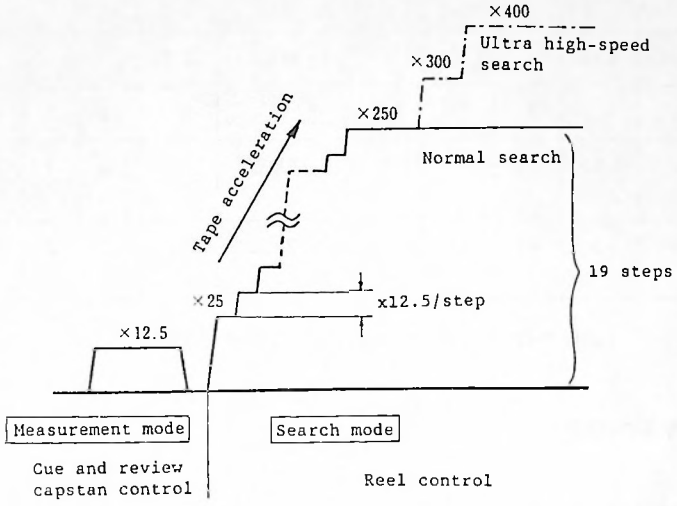


Fig. 1–7 New CRV Servo Mode Transition

4. Shuttle Search

Subcode post-recording, a self-editing function for the recording tape, is a major feature of DAT. This function is very convenient and permits cut and paste editing of recorded music as well as renumbering of programs.

The problems during tape position search in subcode post-recording and dubbing edit for the DAT were "FF and REW are too fast," "cue and review are too slow," or "precise operations cannot be accomplished with cue and review."

The shuttle dial has been placed at the center of the panel and on both sides the subcode post recording keys have been laid out. Along with the display, tray and rounded major control buttons, a distinctive design with ergonomic controls has been achieved.
The center position to forward and to reverse each consist of four shuttle search speeds and two modes, play and pause, are provided for easier operation.

Table 1-1 shows the speeds and modes for the shuttle search. As shown in the table, a wide range of speeds and modes, 7 forward and reverse speed modes of x0.5 to x1.5, are available. Furthermore, in the playback function, the newly developed single LSI chip signal processor (MN6624) provides powerful error correction and data interpolation, and selects the best quality portions of digital data reproduced from tape to obtain a higher quality playback sound.

Play Direction	REV				MODE	CUE			
Dial position	4	3	2	1		1	2	3	4
Play speed in play mode	-15	-9	-5	-3	PLAY 1	3	5	9	15
Play speed in pause mode	-3	-2	-1	-1/2	PAUSE 0	1/2	1	2	3

Table 1—1 Shuttle Search Speeds and Modes

5. Hyper Memory Search

The hyper memory search is realized from the x400 speed super FF/REW based on the newly developed mechanism and the x250 speed New CRV servo and from utilizing the learning function of a microcomputer-based program. Its mode transition diagram is shown in Fig. 1-8.
In this way, the hyper search achieves an ultra high speed search of x400 by combining the super FF/REW and the search program (PNO) memory function. Along with the significant increase in the speed of the normal search from the conventional x200 to a maximum of x250, search times have been achieved for far searches which are less than 2/3 the conventional search times. Since a data correspondence memory system is adopted using the program number (S-ID, PNO) and reel counter, the hyper memory search provides a feature which enables it to also operate for ordinary tapes which do not contain a recording of a TOC (Table of Contents). The maximum number of memory programs is 20.

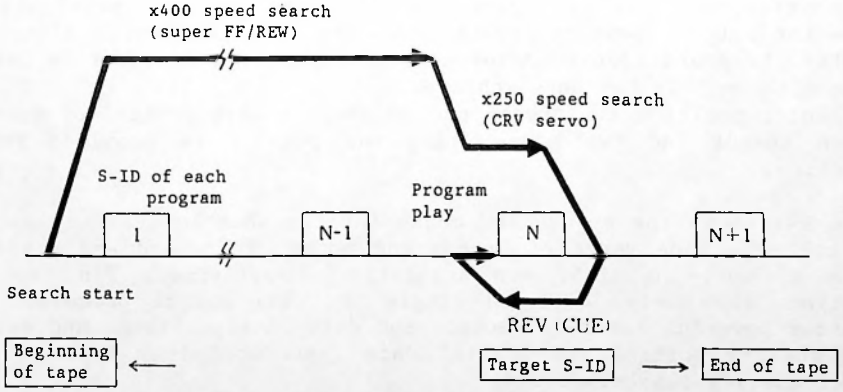


Fig. 1—8 Mode Transition Diagram of the Hyper Memory Search

6. Newly Developed Single-Chip LSI Signal Processor

1) MN6624 LSI Signal Processor

The MN6624 LSI signal processor was developed to achieve high performance and advanced functions of the DAT digital system. It provides all the functions required for DAT signal processing in a single-chip 38,000-gate 124-pin package.
For higher performance, improvements were added to the error correction system. Double correction or triple erasure correction is performed for C1 and triple correction or 6 erasure correction is performed for C2 to achieve powerful error correction which fully utilizes the maximum capability of the error correction code in the DAT standard
For the more advanced functions, additional functions are built-in such as the SCMS-compatible digital audio interface function, the peak level capacity function for the level meter display, the soft mute function, the wide range, variable speed cue and review playback functions, and the digital attenuation function which controls the volume level of the digital audio data.
The block diagram of the MN6624 LSI signal processor is shown in Fig. 1-9.

2) Digital Fade In/Out

Our DAT recorder features an auto fade function. Previously impossible to achieve, fade-in and fade-out recordings of digital input signals can be easily made. As soon as the fade-out button is pressed, the level gradually lowers. After approximately five seconds of the fade-out operation, the operation transfers to auto REC mute and the recording pauses. For fade-in, the fade time is approximately 2.5 seconds. The auto fade function can also be used for analog recordings.
Our DAT recorder provides a function which permits confirmation during recording or playback of whether a digital signal can be recorded as is. When the digital input indicator flashes during recording, it indicates that the digital signal cannot be recorded as is. During playback, when the display is switched to the TOC display mode and the sampling frequency indicator flashes, it indicates that the digital signal cannot be recorded as is from the tape.

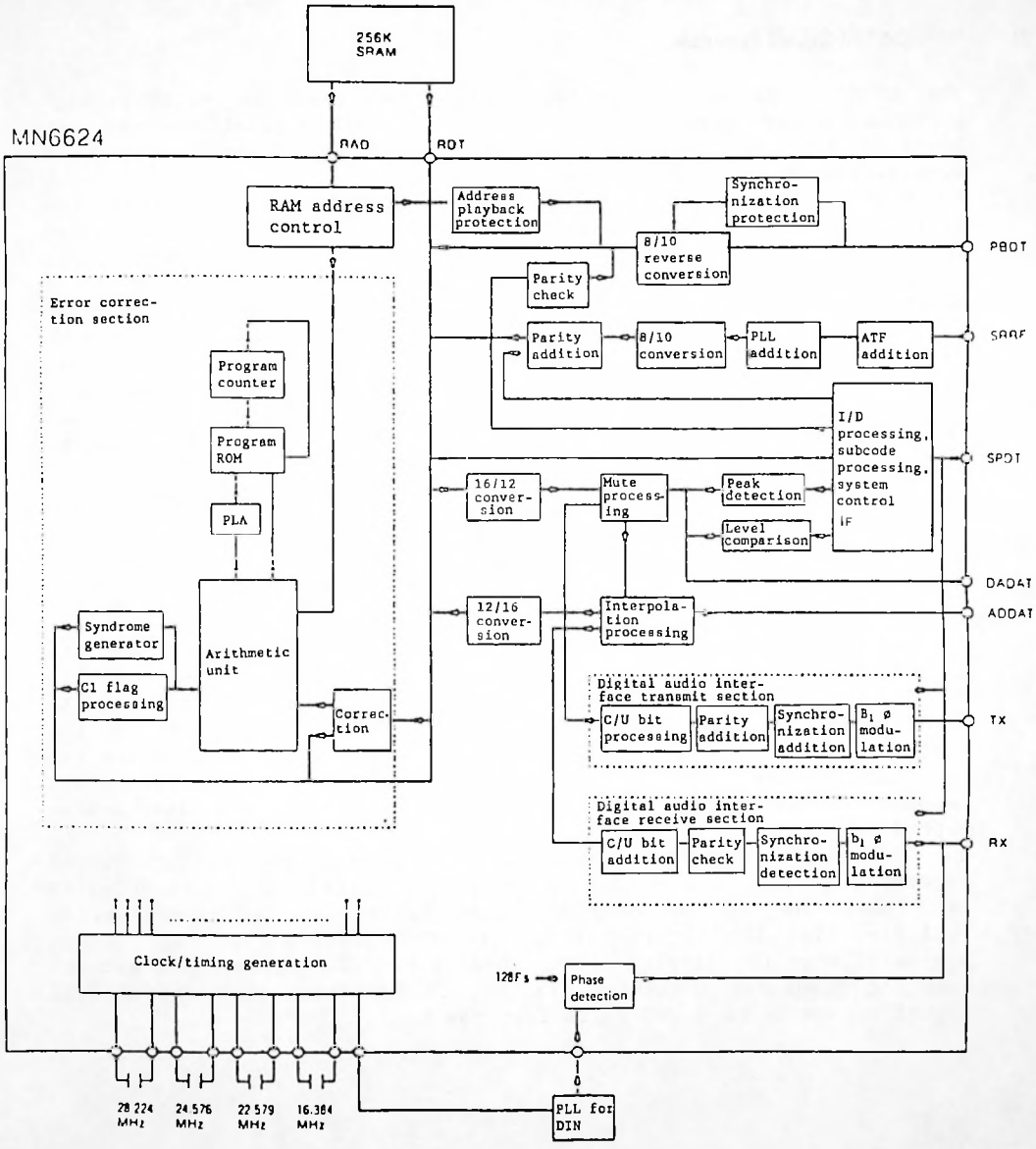
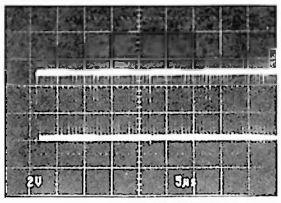


Fig. 1–9 Block Diagram of MN6624

■ BLOCK DIAGRAM

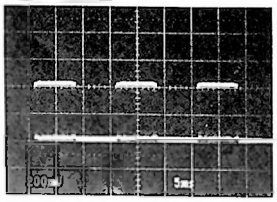
SV-DA10

Ⓐ REC MODE



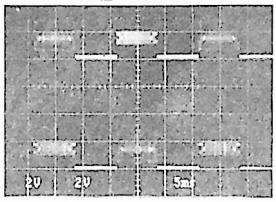
D OUT

Ⓑ REC MODE



SRRF

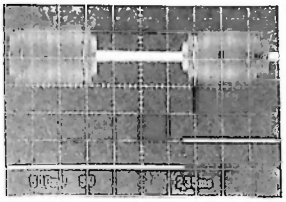
Ⓒ REC MODE



A HEAD

B HEAD

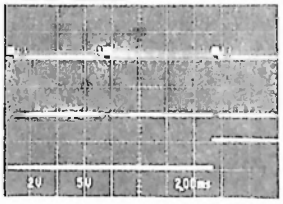
Ⓓ REC MODE



RSRF

HSW

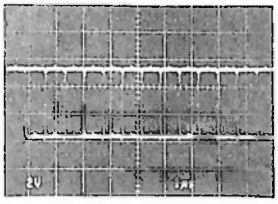
Ⓔ PLAY MODE



VFPLFS

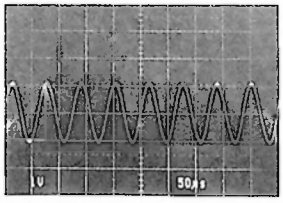
R3CP

Ⓕ PLAY MODE



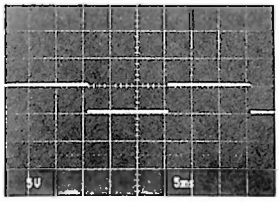
SRDATA

Ⓖ PLAY MODE



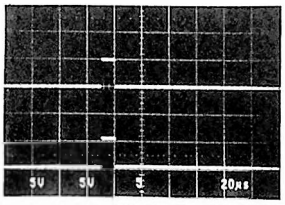
LINE OUT

Ⓗ



R3CP

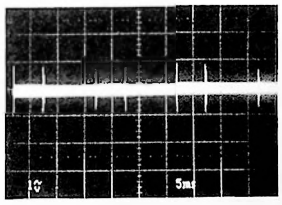
Ⓘ Ⓙ



SP 1

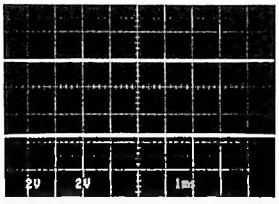
SP 2

Ⓚ



PILOT

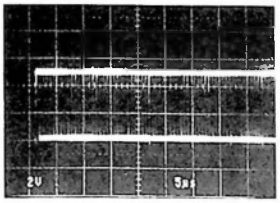
Ⓛ Ⓜ



CYE

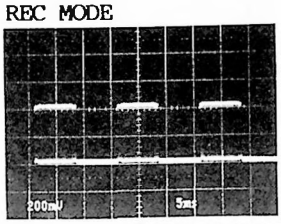
CAE

Ⓐ REC MODE



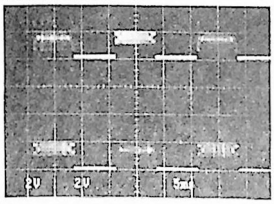
D OUT

Ⓑ REC MODE



SRRF

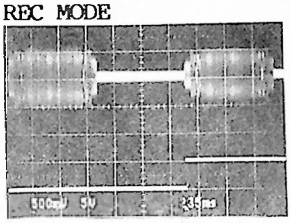
Ⓒ REC MODE



A HEAD

B HEAD

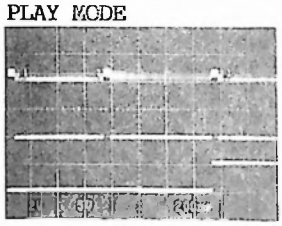
Ⓓ REC MODE



RSRF

HSW

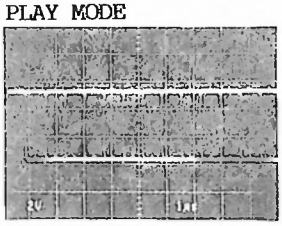
Ⓔ PLAY MODE



VFPLFS

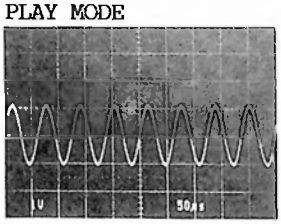
R3CP

Ⓕ PLAY MODE



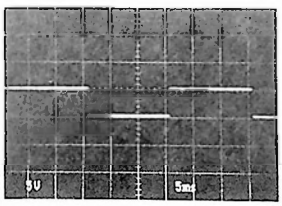
SRDATA

Ⓖ PLAY MODE



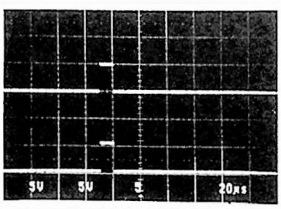
LINE OUT

Ⓗ



R3CP

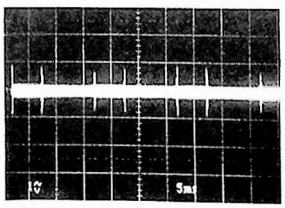
Ⓘ Ⓙ



SP 1

SP 2

Ⓚ



PILOT

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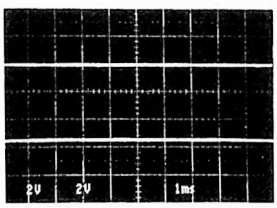

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