ORDER NO. VKD81090572C1

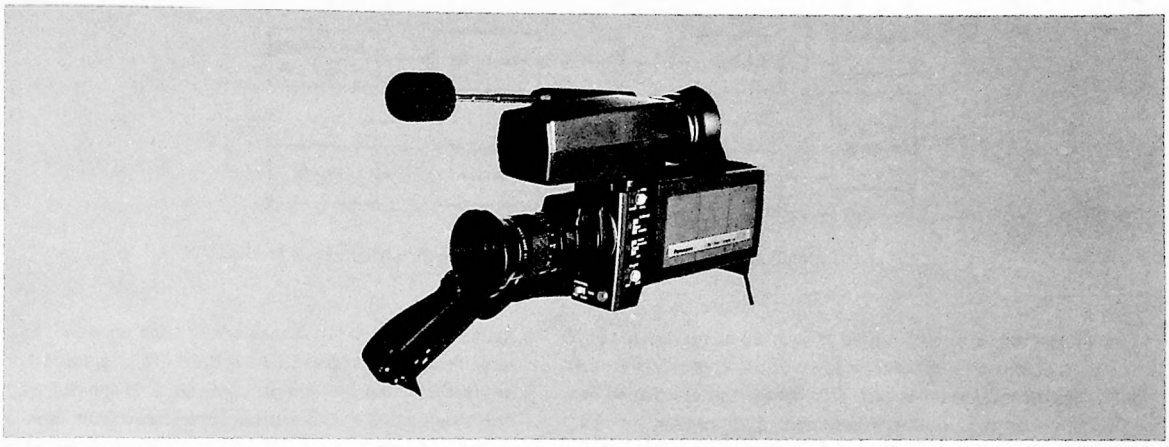
Service Manual

Vol. 1

Circuit Description

Color Video Camera

WV-3110



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CIRCUIT DESCRIPTION OF CAMERA HEAD

1. Principle of Single Carrier Frequency Multiplexing System using a Single Tube.

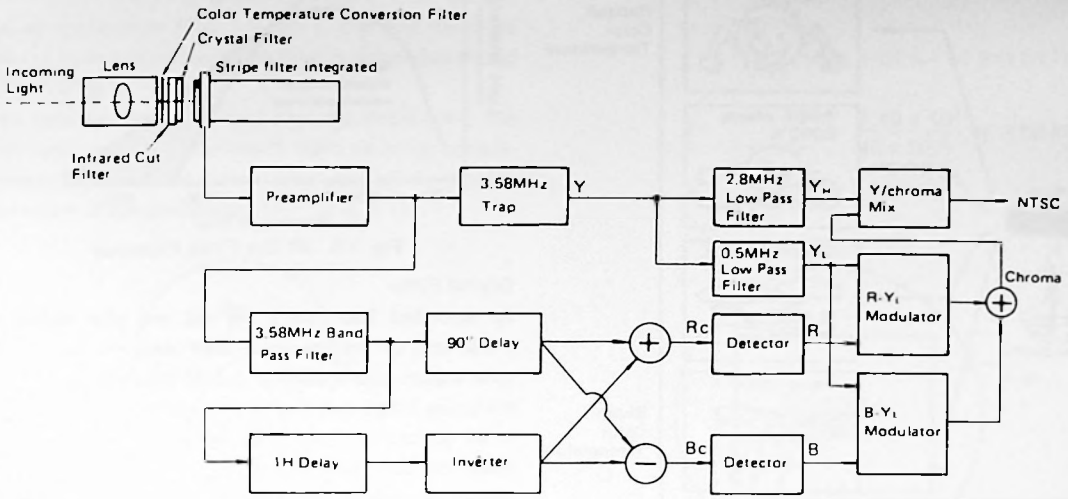


Fig. 1-1 Principle of Single Carrier Frequency Multiplexing System using a Single Tube.

The incoming light to the camera which passes through the automatic iris control (AIC) lens, the color temperature conversion filter, the infrared (IR) cut filter and the crystal filter reaches the surface of the integrated stripe filter in a 2/3" vidicon (S4094).

The diffusion filter is inserted between the AIC lens and the color temperature coversion filter when the white balance switch is set to CHECK or SET position.

Color Temperature Conversion Filter

Generally, the human eye is sensitive to electromagnetic waves from 380mμ (mμ=nm) to 780mμ in wavelength (the visible region). In addition, the human eye also discerns the wavelength difference as a color difference. The human eye responds to the light between 400mμ to 500mμ wavelength as predominantly blue information, the light between 500mμ to 600mμ as green information, and the light between 600mμ to 700mμ as red information. The entire light in the "visible" range of wavelength from 380mμ to 780mμ is "seen" as different amount of white light.

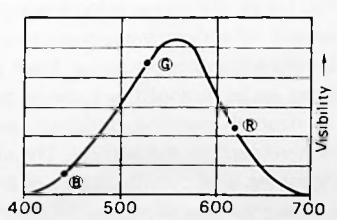


Fig. 1-2 Standard Luminosity Curve

When a carbon is burned, it emits light of a different quality depending on how hot it is. Various natural light can be expressed in terms of a color temperature which may be refered to a light emitted from the burning carbon used as a standard. A light source of 3200°K (K=Kelvin: −273°C corresponds to 0°K an absolute temperature) color temperature, which is used in studios, implies that its quality (color) is the same as that emitted from the carbon burning at 3200°K (2927°C). The relationship between the color temperature of light sources used for illumination and weather conditions are shown in Fig. 1-4. The color temperature goes up as the weather turns overcast from clear. This may be related to the burning carbon (charcoal) as follows. When the charcoal is heated and begins to glow (at low temperature), it emits a reddish light. But when it is so-called white hot (at high temperature), a bluish light is emitted. In other words, the light at a low color temperature is considered reddish and at high color temperature is considered bluish.

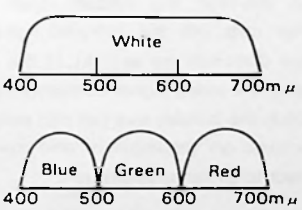


Fig. 1-3 The Visible Spectrum

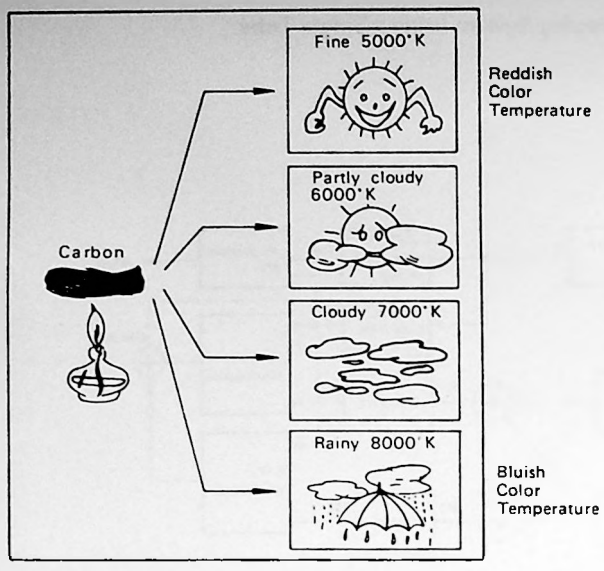


Fig. 1-4 Color Temperature and Weather Conditions

When a color camera is pointed at an object illuminated by a light of low color temperature, it reproduces a reddish picture.

When a color camera is pointed at an object illuminated by a light of high color temperature, it reproduces a bluish picture. The color camera has the indoor-outdoor selection switch which corrects for the color temperature of the light. When the switch is set to the outdoor position, the 5500°K COLOR TEMPERATURE CONVERSION FILTER is inserted into the light path to convert the color temperature from 5500°K to 3200°K. In addition to the indoor-outdoor selection switch utilizing the color temperature conversion filter, this camera is designed so that the level of red and blue signals can be changed independently to meet the color temperature of the light source in order to ensure proper color reproduction.

Infrared Cut Filter

As shown in Fig. 1-5, the vidicon has some sensitivity in the infrared region beyond the visible range. The infrared(IR) cut filter cuts off the infrared light rays which the human eye does not see as light. If the color signal is made by using the video signal corresponding to the infrared rays which the human eye can not normally see, the color of pictures on the monitor and that seen with the naked eye would differ substantially.

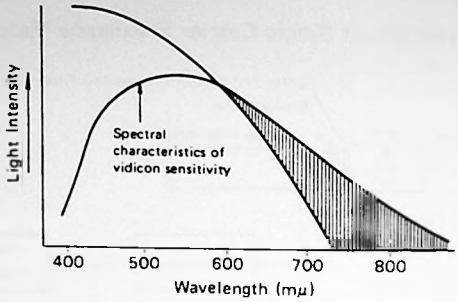


Fig. 1-5 IR Cut Filter Response

Crystal Filter

As described later, since the red and blue images are modulated by the fine stripe filter built into the vidicon, false signals could develop due to interference between the stripe filters and fine detail objects. The crystal filter is an optical low pass filter which prevents the occurrence of such false signals by blocking the high frequency components of images.

Diffusion Filter

When the white balance switch is set to CHECK or SET position, the diffusion filter is inserted between the AIC lens and the color temperature conversion filter to diffuse the incoming light, and the whitish light reaches the vidicon.

Vidicon

Different from that of the black and white camera, the vidicon used in this color camera has a built-in stripe filter, a metallic strip called the optical black(OB) located on the face-plate. The video signal's black level is set in reference to the signal from the optical black.

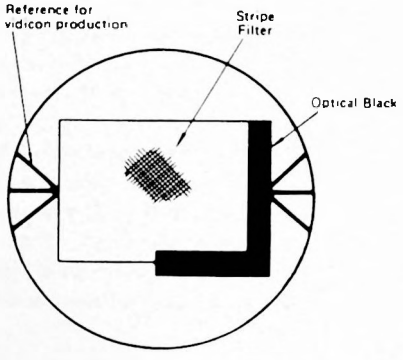


Fig. 1-6 Front View of S4094 Vidicon

As shown in Fig. 1-9 Ⓑ, the stripe filter integrated into the vidicon consists of a cyan/transparent stripe filter section and a yellow/transparent stripe filter section. These stripe filters are so arranged as to be of the same pitch in the horizontal scanning direction, and have equal angles with respect to the vertical. The vidicon's even and odd scanning lines pass the tracks of the stripe filters that are arranged in the same way. In other words, the even and odd scanning lines are spaced "a" apart.

For easy understanding, let's assume that light of uniform level containing green(G), red(R), and blue(B) reaches the vidicon (Fig. 1-9 Ⓐ), and that the cross-point of cyan and yellow stripe filter is scanned as shown in Fig. 1-9 Ⓑ

Let's consider the light output from the stripe filter. The cyan filter cuts off the red(R) light which is complementary to it, and the yellow filter cuts off the blue(B) light which is complementary to it. (Fig. 1-7).

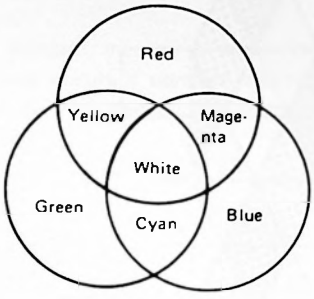


Fig. 1-7 Complementary Color

The light output C , which corresponds to the Nth scanning line containes the modulated R and B components, riding on top of unmodulated G component.

The light output D , which corresponds to the N+1st scanning line contains the modulated R and B components, riding on top of the unmodulated G component. Light output E , F , and G correspond to N+2nd, N+3rd and N+4th scanning lines respectively. The light C for the Nth line and the light G for the N+4th line are exactly same.

The stripe filters have the same pitch in the horizontal scanning direction, and the same angle in the vertical directions so that there is a phase difference of 90° among modulated components.

The vidicon produces the video signal whose waveform is the same as that of the light which comes from the stripe filter.

The modulation frequency for the R and B signals can be calculated from the following equation.

$$f = \frac{w \times 10^3}{p \times t} \quad (MHz)$$

Here, f: Modulation frequency (MHz)

w: Horizontal width of effective scanning area of vidicon (mm)

p: Stripe filter pitch (μm)

t: Horizontal video signal duration [line duration (1H)-horizontal blanking duration (H. BL)] (μs)

Specifically;

w = 7.49 mm

p = 40 μm

t = 1H − H.BL = 63.5 - 11.2 (11.17) = 52.3 μs

$$f = \frac{w \times 10^3}{p \times t} = \frac{7.49 \times 10^3}{40 \times 52.3} \fallingdotseq 3.58 \text{ MHz}$$

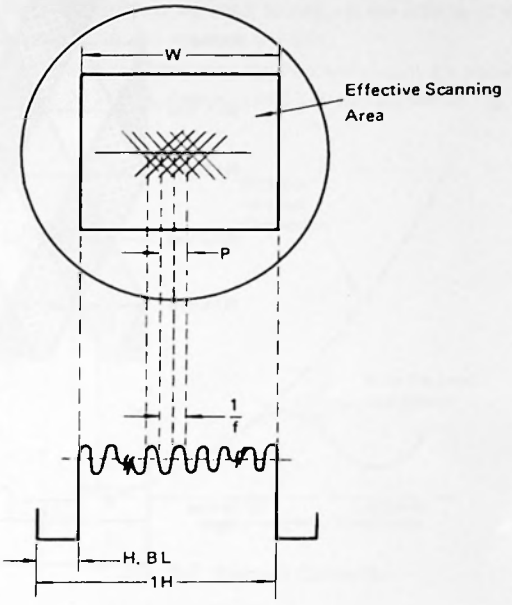


Fig. 1-8 Modulation Frequency

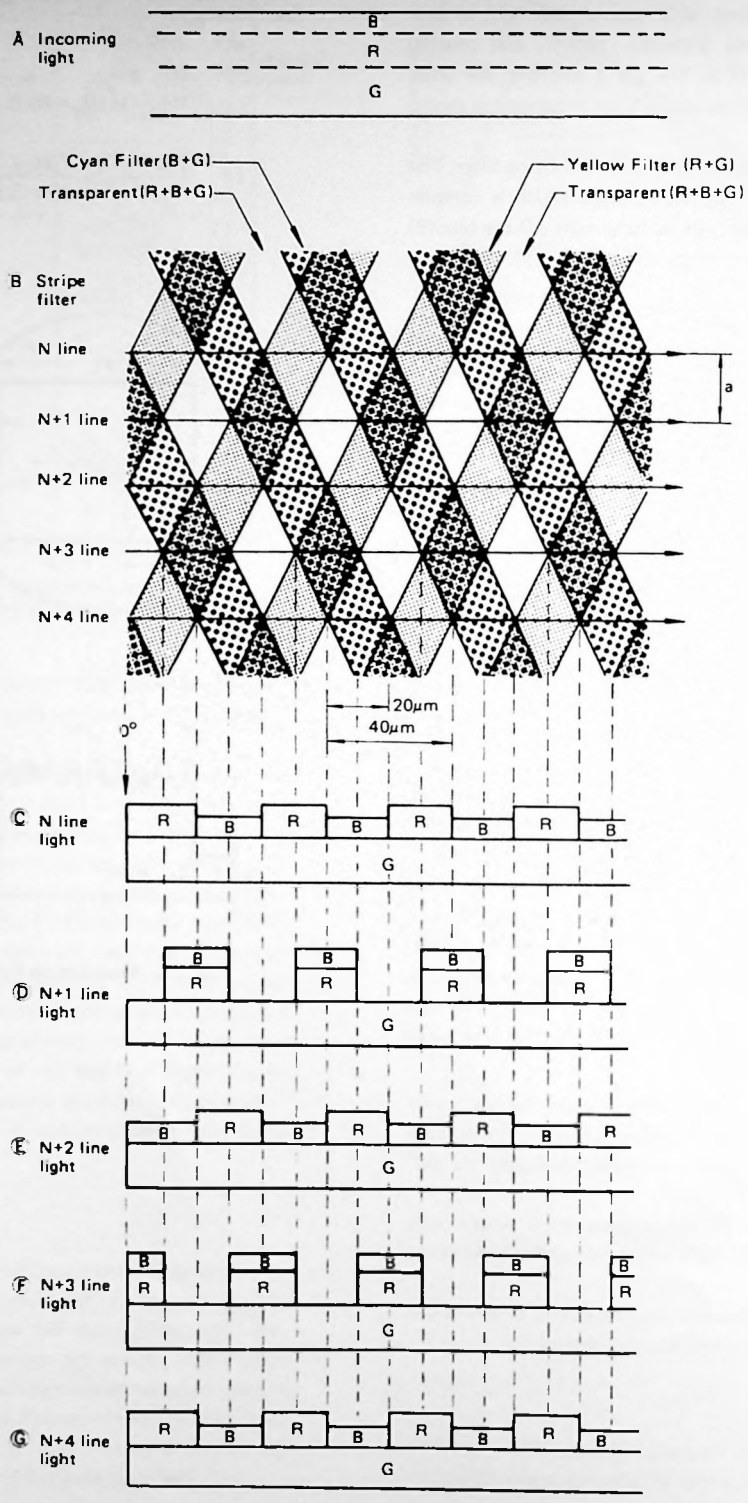


Fig. 1-9 Light from Stripe Filter

The incoming light is thus covnerted by the integrated stripe filter into a signal which contains R and B signals modulated by 3.58 MHz, and the G signal.

This signal is sent to the preamplifier, where it is amplified. The amplified signal Ⓗ (see Fig. 1-11) from preamplifier is sent to the 3.58 MHz trap circuit, which passes only the luminance (Y) signal Ⓘ comprising the G signal and the mean value of the modulated R and B signals. The mean value of modulated R and B signals on adjacent scanning lines are equal so that the luminance signal corresponding to two successive lines is also equal (see Fig. 1-10) due to the characteristics of the trap circuit.

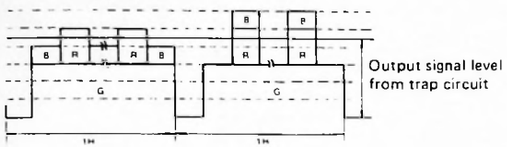


Fig. 1-10 Detection of Y signal

The Y signal thus obtained is supplied to the 2.8MHz low pass filter and the 0.5MHz low pass filter. The luminance (Y_H) signal having high frequency response and the luminance signal (Y_L) having low frequency response come out from these low pass filters.

The Y_H signal is supplied to the Y/chroma mix circuit and the Y_L signal to the R-Y_L and B-Y_L modulator circuits.

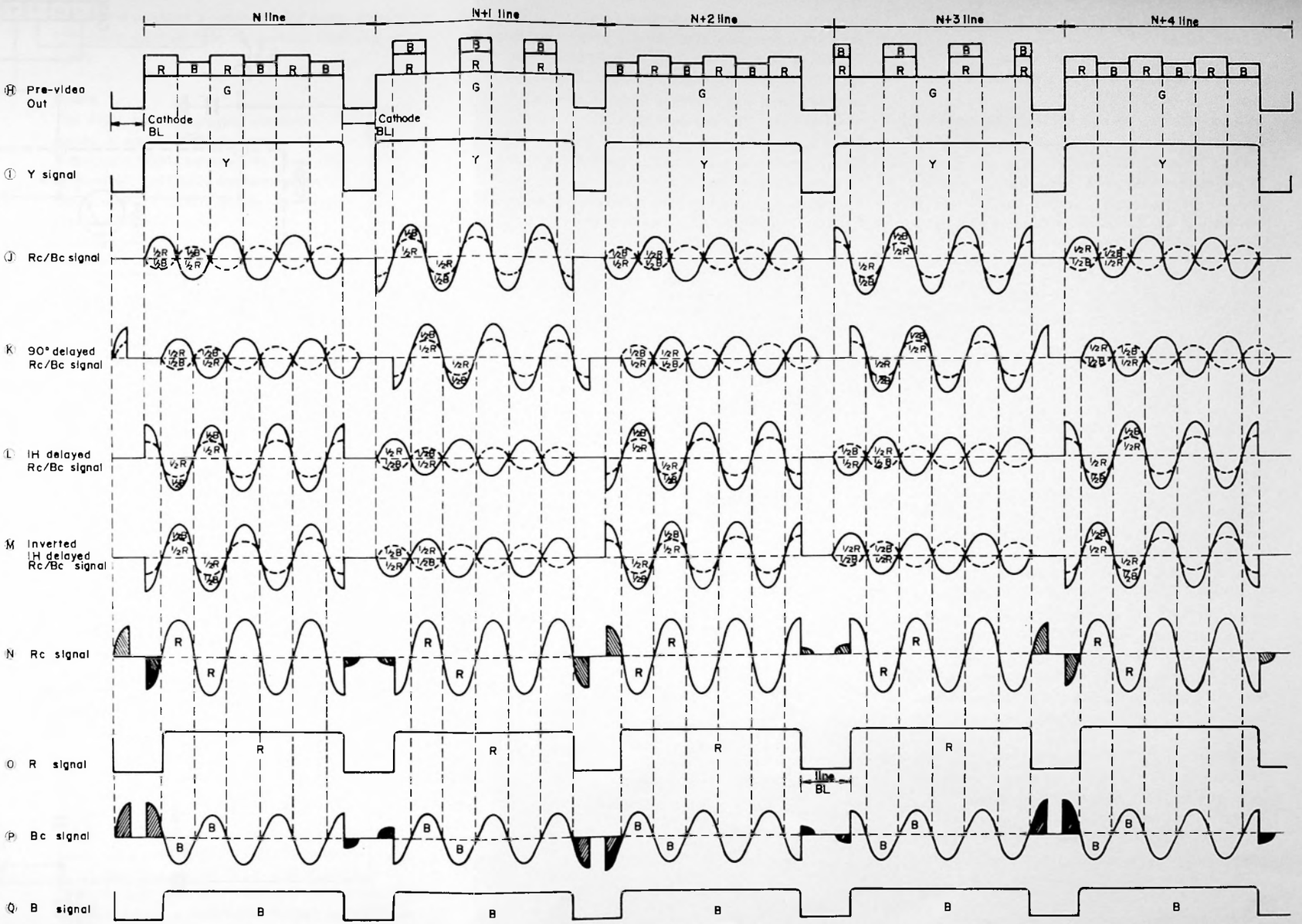
The amplified signal Ⓗ is also supplied to the band-pass-filter (B.P.F.) whose center frequency is 3.58 MHz and through which only the 3.58 MHz modulated signal Ⓙ passes.

The modulated signal Ⓙ is sent to the 90° phase shift circuit and the 1H (1 line) delay circuit, from which 90° phase shifted and 1H delayed modulated signals Ⓚ and Ⓛ are obtained.

The 1H-delayed modulated signal Ⓛ is inverted and the signal Ⓜ is obtained. The modulated R(Rc) signal Ⓝ is obtained by adding the modulated signals Ⓚ and Ⓜ, and the modulated B(Bc) signal Ⓟ is obtained by subtraction of the modulated signals Ⓚ and Ⓜ. The shaded portions on the signals Ⓝ and Ⓟ are removed by mixing the line blanking pulse.

The Rc and Bc signals obtained by addition and subtraction are supplied to detectors, from which R signal Ⓞ and B signal Ⓠ are obtained. The R signal and B signal thus obtained are fed to the R-Y_L and B-Y_L modulator circuits respectively.

The chrominance signal obtained by mixing the R-Y_L and B-Y_L modulated signals is supplied to the Y/chroma mix circuit where it is mixed with the luminance (Y_H) signal to result in an NTSC signal.



* Shaded portion: are removed by mixing the line blanking pulse.

Fig. 1-11

2. Preamplifier Circuit Board (YWCC007ZK05)

Outline

This circuit amplifies the video current Is (0.2μA-0.3μA) from the vidicon.

The amplified video signal is delivered to the AGC & tracking signal generator circuit on the Process circuit board.

The preamplifier is a low output impedance and negative feedback amplifier which uses a low noise FET at the input.

To maintain the low noise in the signal, a so-called Percival circuit is used. It improves the S/N ratio at relatively high frequencies (where color components are located).

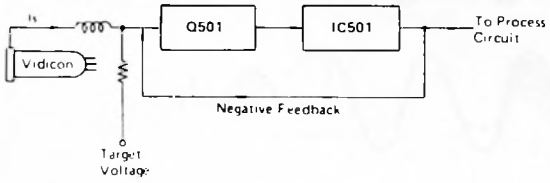


Fig. 2-1 Preamplifier

Details

The signal current from the vidicon, comprising the modulated red(R) and blue(B) components, and the green(G) component, is supplied to the target terminal of the preamplifier circuit and converted to the video signal by R503 through L501 Percival coil. This video signal is amplified approx. 30dB by the amplifier which consists of Q501 FET and Q5001 inside IC501. The amplified signal is then fed to Q5002 and Q5003 which amplify the input signal approx. 66dB.

The signal at the collector of Q5003 inside IC501 is negatively fed back to the gate of Q501 through a feedback circuit which consists of R5013, R5014, C507 and C508.

The VC501 (FREQUENCY RESPONSE ADJUST) adjusts the frequency response of the feedback signal and corrects the frequency response of video signal.

The video signal whose frequency response is shaped by the negative feedback is converted to the low impedance video signal with the use of a buffer Q5004 inside IC501. It is then supplied to the Process circuit board. (YWV3110PZK2).

The target voltage for the vidicon is supplied from the Deflection circuit board to terminal No. 1 (Target voltage in) of the multi-pin connector CN201. The target voltage, controlled due to the vidicon temperature drift, is supplied to the vidicon target through R501, R502 and L501.

Percival Circuit

The vidicon's output is a low noise signal, so that the video S/N is determined by the noise of the preamplifier. The S/N of the modulated R and B signal is lower than the S/N of the non-modulated signal in the low frequency range due to effects of the vidicon output capacitance and the input capacitance of the preamplifier.

Percival circuit is adopted to reduce the effects of these capacitances and improve the S/N.

The beneficial effects of the Percival circuit are shown in Fig. 2-2. The equivalent circuit is also shown in Fig. 2-3.

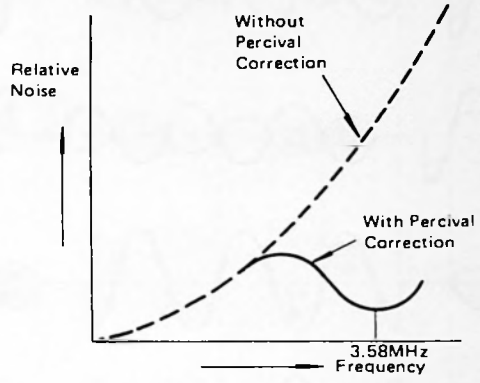


Fig. 2-2 Percival Correction

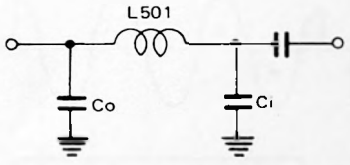


Fig. 2-3

Where: L501; Percival coil
Co ; Output capacitance of vidicon
Ci ; Input capacitance of pre-amp.

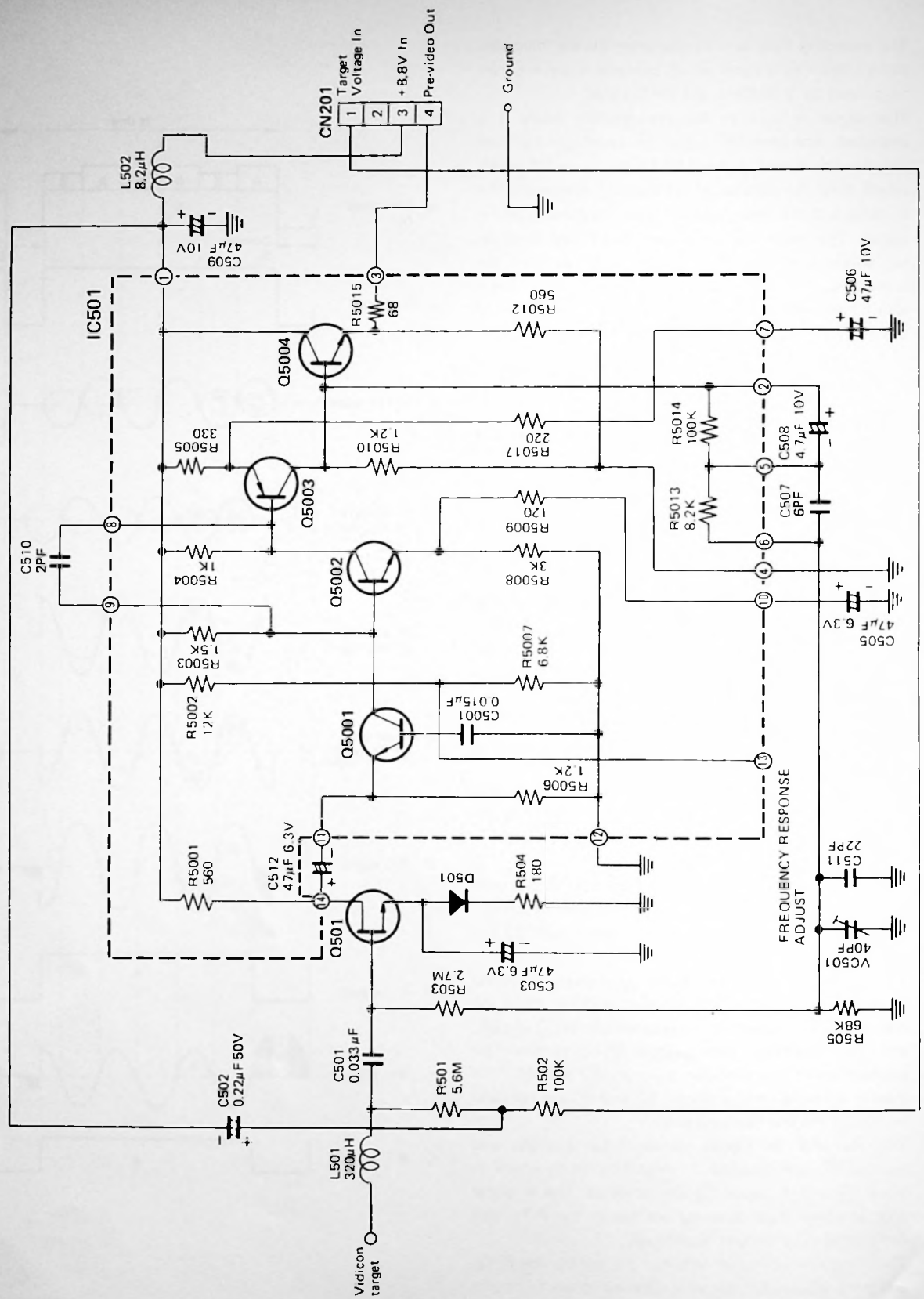


Fig. 2-4 Preamplifier Circuit

3. Deflection Circuit Board (YWV3110PZK1)

The Deflection Circuit Board (YWV3110PZK1) contains following circuits.

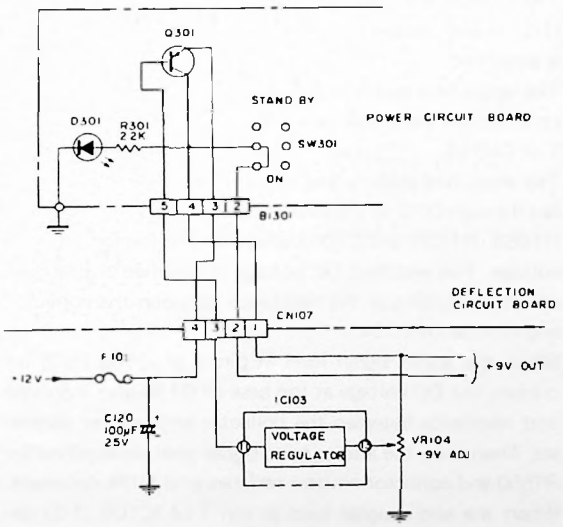


Fig. 3-1 +9V Regulator Circuit

3-1. +9V Regulator Circuit

Outline

This circuit produces a regulated +9V power from the 12V power supplied from the portable VCR or power supply.

Details

The +12V power from the portable VCR or power supply is applied through terminal No. 10 of VCR connector CN004, terminal No. 4 of CN106, F101, terminal No. 4 of CN107 and terminal No. 3 of BI301 to the emitter of Q301 on the Power circuit board (YWV3100PZK3).

A voltage regulator in IC103 amplifies the error between the reference and the potential set by VR104 (+9V ADJ) and forwards it to Q301 base. If the Q301 collector potential changes, the potential set by VR104 also changes, and a voltage change appears at the output of the voltage regulator.

This change controls the base current of Q301 in the direction which opposes the voltage change at Q301 collector.

As a result, the output voltage remains constant. VR104 is adjusted for 9V. D301 is the power indicator LED on the rear panel.

3-2. +6V/+4.5V Regulator Circuit

Outline

+6V and +4.5V are generated by regulating the +9V generated in the +9V regulator circuit. They are used as sub-power supply for other circuits.

Details

The +6V power is generated by regulating the +9V power supply using IC104 (1/2). The output voltage of IC104 (pin 7) is applied to pin 6 of IC104 through Q130 and Q137 to form a feedback loop, and thus stabilizing the voltage. The reference voltage is obtained by dividing the +9V using R138 and R139.

The +4.5V is generated by regulating the +9V power supply using another IC104 (1/2). The output voltage of IC104 (pin 1) is applied to pin 2 of IC104 to form a feedback loop, and thus stabilizing the voltage. The reference voltage is obtained by dividing the +9V using R151 – R153.

3-3. Battery Warning Indicator Circuit

Outline

This circuit flashes the recording tally (REC) in the viewfinder when the DC power supplied from the portable VCR to the camera becomes below the specified level.

Details

The +12V DC power supplied through terminal No. 4 of CN106 is divided by R1546, R1545 and VR120 (BATTERY WARNING LEVEL) and fed to pin 3 of IC108. The output voltage at pin 1 of IC108 is also supplied to pin 3 of IC108 through R1542 and the reference voltage obtained by dividing the output voltage with R1544 and R1541 is supplied to pin 2 of IC108.

Under normal condition, the voltage at pin 3 of IC108 is higher than the voltage at pin 2 and the output of IC 108 at pin 1 stays HIGH.

If the DC power voltage becomes below the specified level (approx. +11V at terminal No. 10 of VCR connector CN004), the voltage at pin 3 becomes lower than that of pin 2. In this case, the output of IC108 at pin 1 turns to LOW to light the battery warning indicator (REC) D1002 on the viewfinder. At the same time, the voltage at pin 2 starts decreasing gradually due to discharging C1005 through R1541 and R1544. Then the voltage at pin 2 becomes lower than the voltage at pin 3 and the output of IC108 turns to HIGH to goes off the indicator D1002. If the output of IC108 becomes HIGH, the voltage at pin 2 starts increasing gradually by charging to C1005 through R1544, then the voltage at pin 2 becomes higher than the voltage at pin 3 and the output of IC108 turns to LOW to lights D1002.

In this way, if the DC power becomes below the specified level, this process is repeated and the battery warning indicator (REC) D1002 is kept flashing.

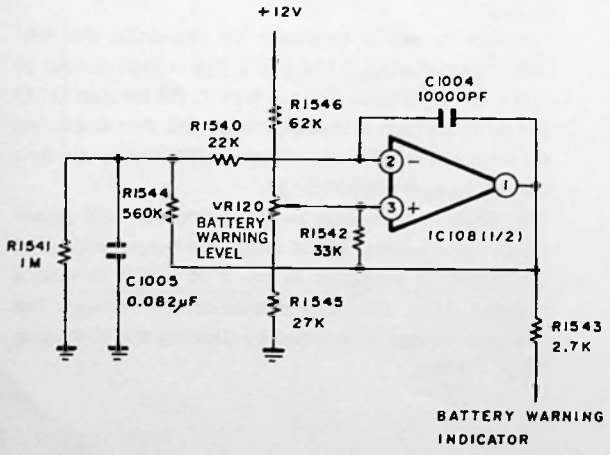


Fig. 3-3 Battery Warning Indicator Circuit

3-4 Audio Amplifier Circuit

Outline

This circuit amplifies the output from the mounted boom microphone or external microphone, and sends out the amplified audio signal to the VCR for recording.

Details

The −72dB output from the electret condenser microphone (which is mounted on the camera), or an external microphone is amplified +52dB by IC101 (1/2). The low-frequency response characteristic of the audio output is set by C105, C107, R1023 and its high-frequency response characteristic by C106.

The −20dB audio output is sent directly from pin 1 of IC101 to the portable VCR, or via power supply to the table model VCR through terminal No. 7 of VCR connector through terminal No. 6 of CN106.

It is also sent to the earphone amplifier circuit.

3-5 Earphone Amplifier Circuit

Outline

This circuit amplifies the audio output from audio amplifier circuit and sends out the amplified audio signal to the earphone jack on the rear of camera for audio monitoring.

Details

The −20dB audio output at pin 1 of audio amp IC101 (1/2) is sent to pin 6 of audio amp IC108 (1/2) where it is amplified.

The amplified audio signal is sent from pin 7 of IC108 (1/2) to the earphone jack CN007 through terminal No. 1 of CN114.

The amplified audio signal at pin 7 of IC108 (1/2) is also fed through D112 to the peak-rectifier consisting of Q135, R1053, R1055 and C1001 where it is converted into DC voltage. The rectified DC voltage is supplied to the base of Q134 to control the resistance between the collector and emitter of Q134.

When the audio signal level at pin 7 of IC108 (1/2) increases, the DC voltage at the base of Q134 also increases and resistance between the collector and emitter decreases. Therefore, the audio input signal level determined by R1550 and collector-emitter resistance of Q134 decreases. When the audio signal level at pin 7 of IC108 (1/2) decreases, the reverse operation takes place. In this way, the earphone output signal level is kept constant.

3-6. Zoom Control Circuit

Outline

This circuit drives zoom lens motor.

Details

When the TELE switch SW802 is depressed, DC voltage obtained by dividing +9V with R1015 and R1017 is supplied to the base of Q101, and Q101 and Q104 turn ON. Therefore, the current flows into the zoom motor through Q101 and Q104 for zoom-in (telephoto) operation.

When the WIDE switch SW801 is depressed, Q103 and Q102 turn ON. Therefore, the current flows into the zoom motor (in the reverse direction) through Q103 and Q102 for zoom-out (wide angle) operation.

SW602 is a zoom speed switch to set the zooming speed by changing the DC voltage at the base of Q101 and Q103.

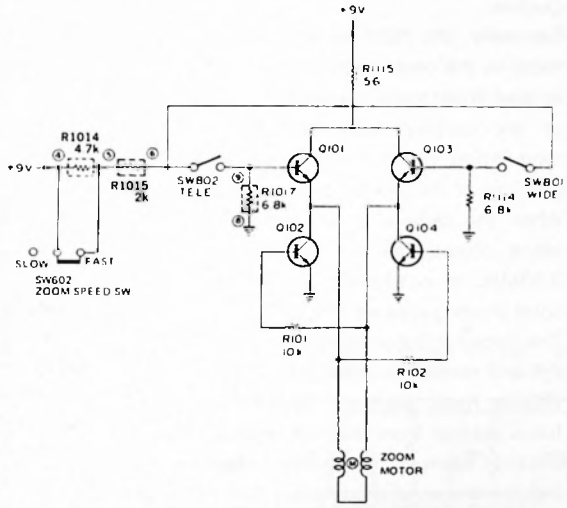


Fig. 3-6 Zoom Control Circuit

3-7. Horizontal Sawtooth/Parabola Generator Circuit

Outline

This circuit generates the horizontal sawtooth and parabola waveforms needed in the dark shading correction circuit and dynamic focus correction circuit on the Deflection circuit board.

The horizontal sawtooth and parabola signals are also fed to the Process circuit board for shading correction.

Details

The horizontal scanning start pulse (Hs) from the Process circuit board enters the base of Q105 through terminal No. 7 of BI103. The Hs pulse is then fed to a miller integrator consisting of R103, C108 and IC101 (1/2) and converted into a sawtooth signal.

The H. sawtooth signal at pin 7 of IC101 is fed to the wiper arms of VR102 (H. SAWTOOTH) for the dark shading correction, VR132 (H. SAWTOOTH) in Variable Resistor Block BVR1 for the dynamic focus correction and the Process circuit board through terminal No. 3 of BI101.

The H. sawtooth signal at pin 7 is also supplied to another miller integrator consisting of R104, C110 and IC102 (1/2) to convert it into a parabola signal.

The H. parabola signal obtained at pin 7 of IC102 is fed to the wiper arms of VR101 (H. PARABOLA) for the dark shading correction, VR131 (H. PARABOLA) in Variable Resistor Block BVR1 for the dynamic focus correction and the Process circuit board through terminal No. 2 of BI101.

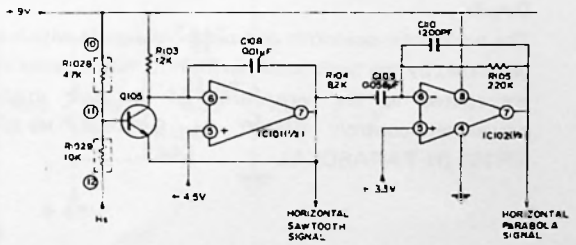


Fig. 3-7 Horizontal Sawtooth/Parabola Generator Circuit

3-8. Dark Shading Correction & Cathode Blanking Circuit

Outline

The vidicon produces dark current when the light is blocked by capping the lens for example. The dark current is not uniform along the entire target structure, but has a "shading" Ⓐ.

As described in the section on the principle of single carrier frequency multiplexing, the red and blue signals are obtained by detecting the modulated signals from the preamplifier output using a band pass filter. Therefore, the red and blue signals are free from dark shading.

However, the luminance signal is obtained by removing the modulated signal using a trap circuit. Therefore, the luminance signal receives undesirable dark shading.

The dark shading correction circuit supplies horizontal sawtooth and parabola signals Ⓑ to the vidicon cathode (K) to correct color shading at low illumination levels.

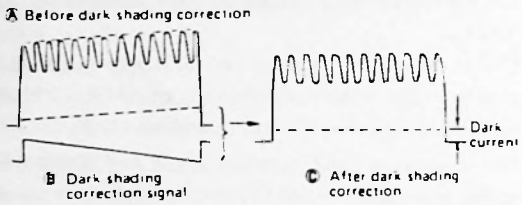


Fig. 3-8-1 Dark Shading Correction

This circuit also generates a cathode blanking pulse and supplies it to the vidicon cathode (K) together with the dark shading correction signal in order to eliminate the retrace scanning lines.

Details

The horizontal sawtooth and parabola signals which are generated by the horizontal sawtooth/parabola generator are routed to the wiper arms of the dark shading correction controls VR102 (H. SAWTOOTH) and VR101 (H. PARABOLA).

These signals are applied to both the inverted (pin 2) and non-inverted input (pin 3) of IC102 (1/2), where they are amplified.

The output of IC102 at pin 1 produces a positive or negative dark shading correction signal which depends on the position of these controls.

The horizontal (H) flyback pulse at the collector of H. deflection output Q116 and the vertical scanning start (Vs) pulse from terminal No. 4 of BI103 are supplied to the base of Q106 respectively.

The mixed signal obtained at the collector of Q106 is fed to buffer Q108 through switching amplifier Q107 as a cathode blanking (BL) pulse and mixed with the dark shading correction signal supplied through D101.

The mixed signal at the emitter of Q108 is supplied to the cathode (K) of vidicon.

3-9. Dynamic Focus Correction Circuit

Outline

Generally, the focus voltage which brings the beam in focus in the center part of the pick-up tube is different in level from the voltage which brings the edge portions of the pick-up tube into best focus so that the modulation depth for the center part and the edge portions of the pick-up tube differ.

When the camera is directed at an evenly illuminated white object, the red and blue signals modulated at 3.58MHz do not have a uniform level, and as a result, a color shading appears (Fig. 3-9-1 Ⓐ)

The dynamic focus correction circuit supplies horizontal (H) and vertical (V) sawtooth and parabola signals to the vidicon focus electrode (grid-4) together with the DC focus voltage from the high voltage circuit to focus the electron beam along the entire scanning area for correcting unevenness of modulation factor (Fig. 3-9-1 Ⓑ).

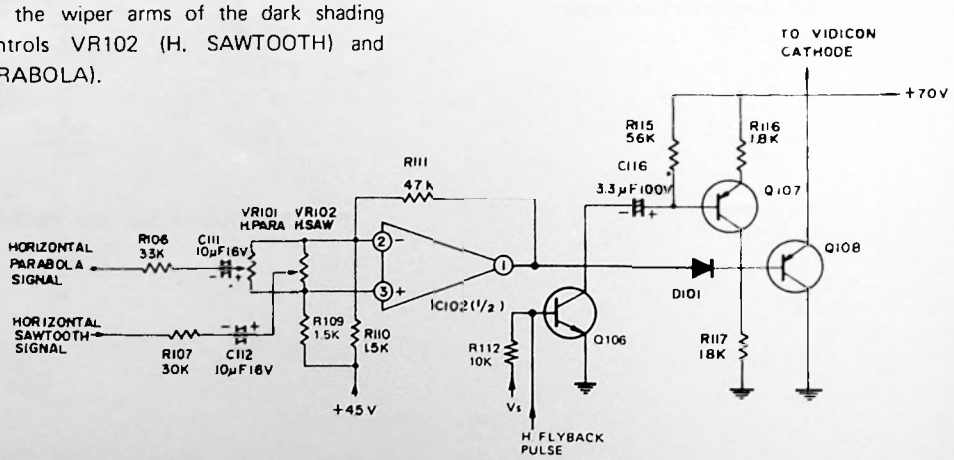


Fig. 3-8-2 Dark Shading Correction & Cathode Blanking Circuit

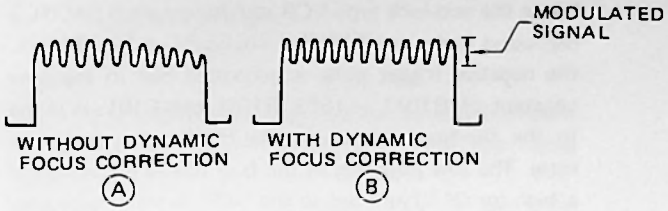


Fig. 3-9-1 Dynamic Focus Correction

Details

The horizontal sawtooth signal from pin 7 of sawtooth generator IC101(1/2), the horizontal parabola signal from pin 7 of parabola generator IC102(1/2), the vertical sawtooth signal from pin 1 of vertical sawtooth/parabola generator IC106, and vertical parabola signal from pin 7 of IC106 to the wiper arms of dynamic focus correction control VR132 (H. SAWTOOTH), VR131 (H. PARABOLA), VR134 (V. SAWTOOTH) and VR133 (V. PARABOLA) respectively.

These waveforms are applied to both the base and emitter of Q109, where they are amplified. The collector of Q109 produces an inverted or non-inverted signal depending on the position of these controls.

The dynamic focus correction waveform at the collector of Q109 is AC coupled via C118 into vidicon grid-4 (G4) electrode which normally receives the DC voltage adjusted by VR116 (FOCUS).

In this way, the electron beam is focused along the entire scanning area, and the unevenness of modulation is corrected.

Note: Dynamic focus should be adjusted when color non-uniformity is seen in the picture of a white card after dark shading is properly adjusted and after electrical focus and beam alignment are correctly set.

To judge whether the camera needs this adjustment, signal shading potentiometers VR209, 211, 213, 215 (R. Shading Correction) and VR208, 210, 212, 214 (B. Shading Correction) on the Process circuit board (YWV-3110PZK2) must be at their mechanical centers.

Be aware that proper beam alignment has greater contribution to color uniformity than dynamic focus even though it is more difficult to achieve in a hurry.

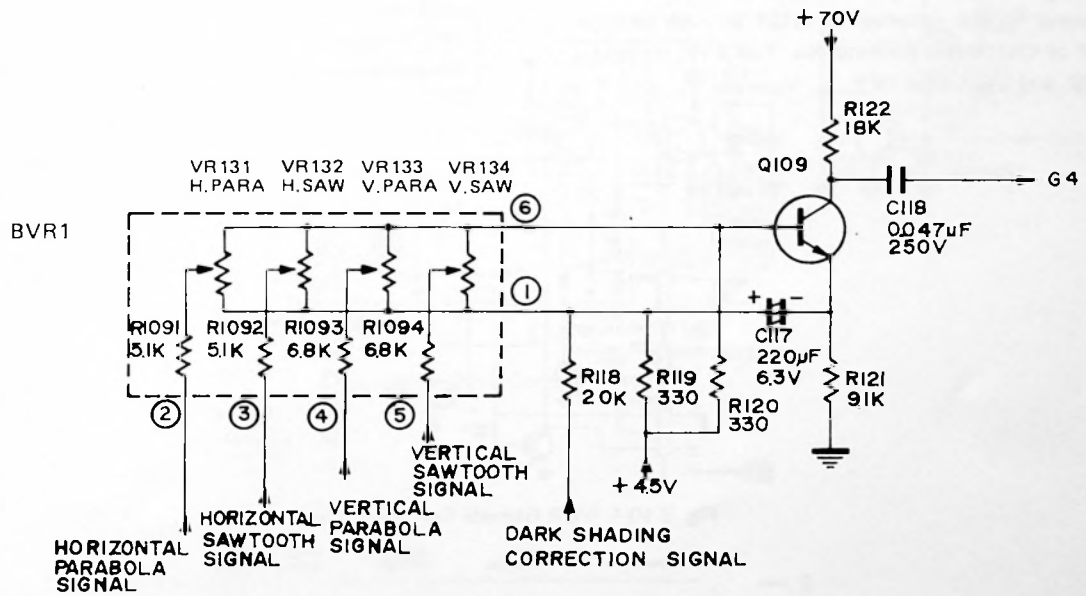


Fig. 3-9-2 Dynamic Focus Correction Circuit

3-10. VCR Remote Control Circuit

Outline

This circuit generates VCR start/stop (pause) control signal.

When the VCR is set to the recording mode, the VCR is started by a high potential from this circuit. If a low potential is sent to the VCR, it stops (pauses).

This circuit also has the VCR compatibility switch for other VCR which is started by a low potential and stopped by a high potential.

Details

When the power switch is turned ON, the potential at pin 6 and pin 7 of IC103 is set to high and low respectively by a flip-flop circuit inside IC103.

When the VCR is set to the recording mode and the VCR compatibility switch SW004 is set to the normal (+) position, the high potential at pin 6 is fed through CN115, VCR compatibility switch SW004 to Q110 where it is inverted. The inverted low potential is supplied through terminal No. 1 of CN106 and terminal No. 6 of VCR connector CN004 to the VCR to stop (pause) it.

At the same time, the low potential at pin 7 turns OFF inverter Q121. Therefore, no current flows to the VCR recording indicator D1002 in the electronic viewfinder connected to the collector of Q121 through terminal No. 4 of CN109 and terminal No. 7 of EVF connector CN802 and it is turned OFF.

When the non-lock type VCR start/stop switch SW701 is depressed (refer to "FIRST TRIGGER" in Fig. 3-10-2), the negative trigger pulse is generated due to the time constant of R1011 – 1013, R1016 and C101. It is fed to the flip-flop, and causes the flip-flop to change its state. The low potential at pin 6 of IC103 is inverted to a high by Q110 and fed to the VCR to start recording. At the same time, the high potential at pin 7 of IC 103 turns ON Q121 and the current flows to the VCR recording indicator D1002 lights.

When a subsequent trigger pulse is sent to the flip-flop by depressing SW701 again (refer to "SECOND TRIGGER" in Fig. 3-10-2), the flip-flop is inverted. As a result, the VCR is stopped and recording indicator goes OFF.

The VCR compatibility switch SW004 and inverter Q133 invert the potential of VCR start/stop control signal for other VCR which starts with a low potential and stops with high potential.

When the VCR is set into the playback mode, an inhibit signal (high level) from the VCR is supplied to the base of Q113 to turn it ON setting the potential at pin 3 of IC103 to low so that the potential at pin 6 and pin 7 are forced high and low respectively. In this state, even if another trigger pulse is sent to the flip-flop by depressing SW701 again, the flip-flop remains set. Therefore, no current flows to the VCR recording indicator and no VCR recording control signal is sent to VCR from Q110. This condition is maintained until the playback mode is released and set to the recording mode again.

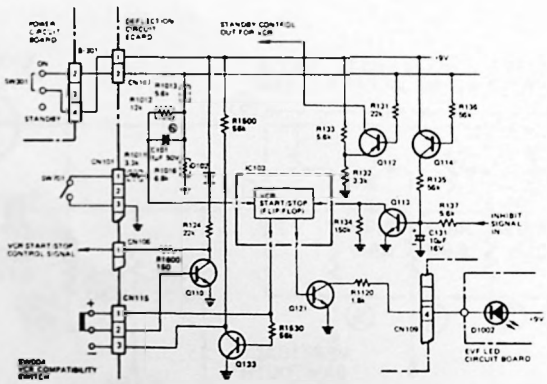


Fig. 3-10-1 VCR Remote Control Circuit

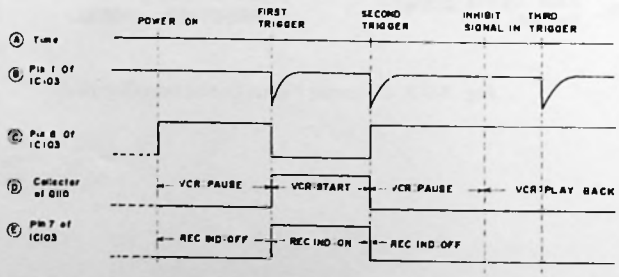


Fig. 3-10-2 Timing Chart

3-11. Fade Control Circuit

Outline

This circuit generates the fade control signal and sends it to the Process circuit board to control the video fade-in/out effects.

When the VCR is in recording mode, if the VCR start/stop switch is depressed after pressing the fade switch, the fade-out effect is obtained and the VCR pauses, then the picture reappears. If the VCR is in pause, depressing the VCR start/stop switch after pressing the fade switch, the video will fade out, the VCR starts recording and the video fade in again.

If the VCR start/stop switch is depressed without pressing the fade switch, no fade effect occurs and the VCR is remote-controlled as described in VCR remote control circuit.

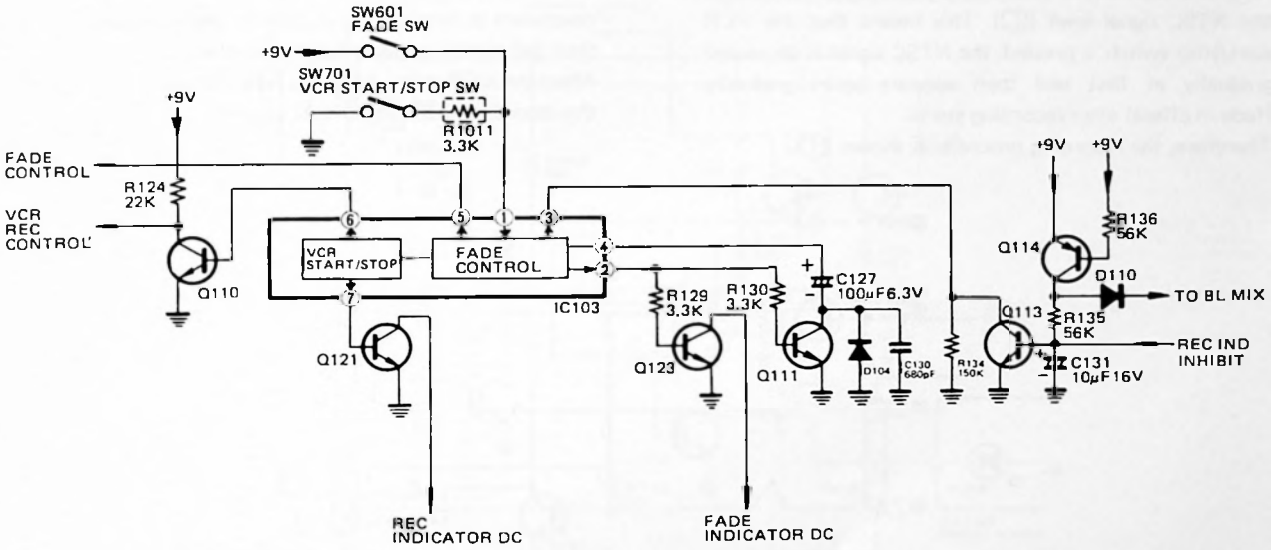


Fig. 3-11-1 Fade Control Circuit

Details

Fade-in effect

When the momentary fade switch SW601 is depressed (Ⓐ), the DC level at pin 1 of IC103 becomes higher (+9V) than DC voltage obtained by R1013, R1016 (about 5V). This high DC level initiates the fade control circuit in IC103.

This trigger signal changes pin 2 from low to high (Ⓕ) turning ON Q123 and the fade indicator (D1003) in the viewfinder lights. Then when the VCR start/stop switch SW701 is pressed (Ⓑ, 1st Trigger), pin 1 of IC103 goes low and the level at pin 5 starts increasing gradually (Ⓓ).

After about a second (determined by R126, C127), the potential at pin 6 of IC103 becomes low (Ⓖ) turning OFF Q110 and the VCR starts recording (Ⓗ).

Simultaneously, the potential at pin 2 of IC103 goes low (Ⓕ) and the DC level at pin 5 starts decreasing gradually (Ⓓ). This DC level (Ⓓ) at pin 5 of IC103 is sent to the Process circuit board as a fade control signal to control the NTSC signal level (Ⓔ). This means that the VCR start/stop switch is pressed, the NTSC signal is decreased gradually at first and then appears again gradually (fade-in effect) after recording starts.

Therefore, the recording proceeds as shown (Ⓘ).

When the VCR starts recording, the fade indicator D1003 goes OFF and recording indicator D1002 lights. If the VCR start/stop switch SW701 is depressed independently after the fade-in effect is accomplished (Ⓑ, 2nd and 3rd Trigger). The VCR can be remote-controlled as previously described in VCR remote control circuit.

Fade-out effect

As in the case of fade-in effect, if the VCR start/stop switch SW701 is depressed (Ⓑ, 4th Trigger) after pressing the fade switch SW601, the DC level at pin 5 of IC103 starts increasing gradually to fade-out the video. After few seconds, the potential at pin 2 of IC103 goes low to turn OFF D1003 and the potential at pin 6 of IC103 goes high and VCR stops (pauses). Now the DC level at pin 5 start decreaisng gradually. This DC level at pin 5 of IC103 is sent to the Process circuit board to control the NTSC signal level.

When the VCR start/stop switch is pressed, the picture disappears at first (fade-out effect), the VCR pauses and then the picture appears again gradually.

When the VCR stops, both the fade indicator D1003 and the recording indicator D1002 go OFF.

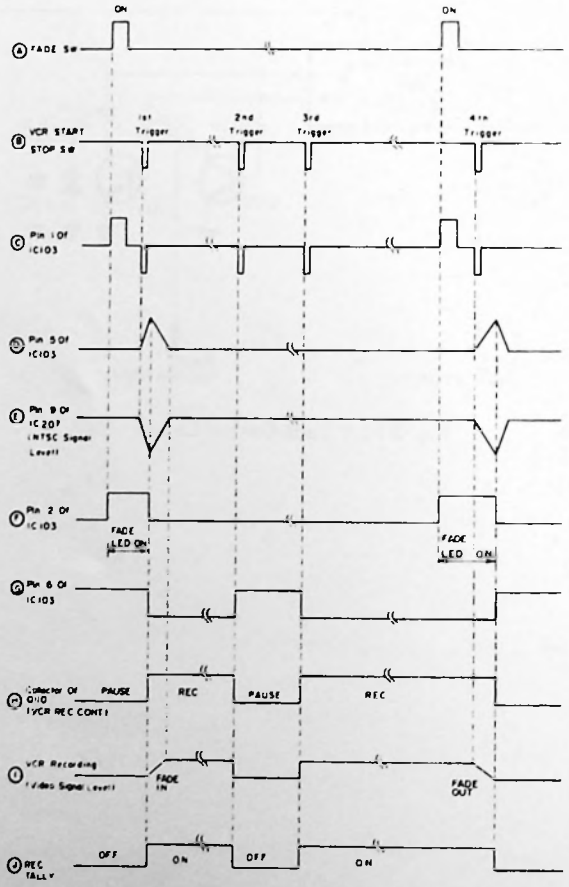


Fig. 3-11-2 Fade Timing Chart

3-12. Standby Circuit

Outline

When recording outdoors, using camera and VCR, the power reserve of the batteries must be conserved as much as possible, which is the exact function of the standby circuit.

Details

When the standby switch SW301 is set to the "ON" position, practically all circuits in the camera and the VCR are operational, that is, the power from +9V source is supplied to all electric circuits in the Process, Deflection and Viewfinder circuit boards in the camera and +12V is consumed in the VCR.

When the standby switch SW301 is set to the "STAND-BY" position, the power from +9V source goes only to the +6V DC regulator in order to preheat the heater of vidicon tube and cathode ray tube(CRT). At the same time, Q112 turns ON and the VCR receives a standby signal(+3V) from the collector of Q112 to stop (stand-by) the operation of itself.

Since the +9V DC regulator circuit and the VCR remote control circuit are located in the same IC, the VCR remote control circuit also receives the +9V power in the standby mode. Therefore, the state of flip-flop is controlled by the operation of VCR start/stop switch SW701 and the VCR recording indicator D1002 is turned ON/OFF in the standby mode. Q114 turns OFF D1002 in the standby mode.

When the standby switch SW301 is set to STANDBY mode, Q114 turns ON causing Q113 ON and the potential at pin 3 of IC103 low. As a result, the potential at pin 6 and pin 7 are forced high and low respectively, and D1002 goes OFF.

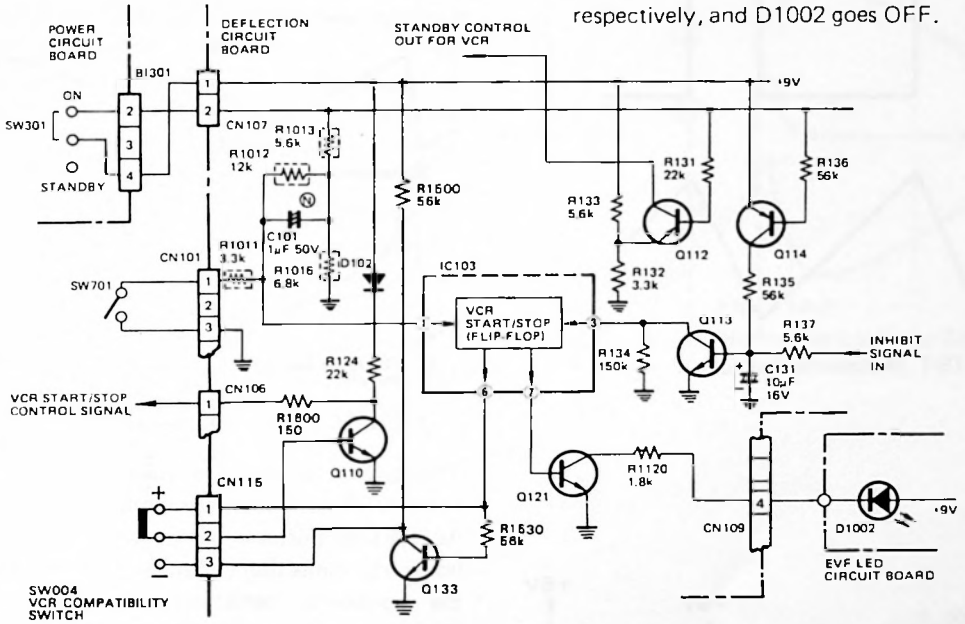


Fig. 3-12-1 Standby Circuit-1

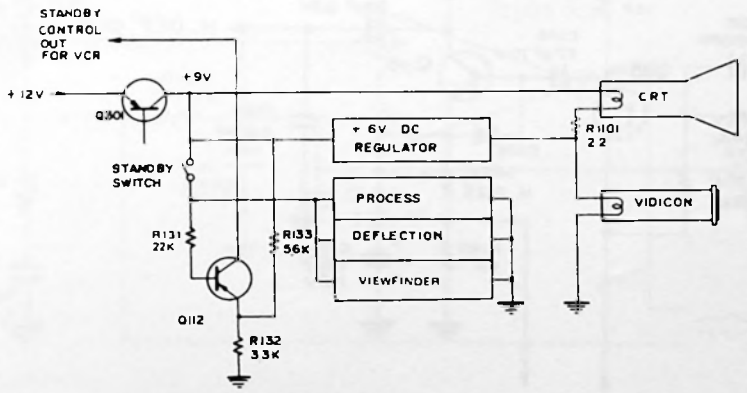


Fig. 3-12-2 Standby Circuit-2

3-13. Horizontal Deflection Circuit

Outline

This circuit generates the sawtooth current for the horizontal (H) beam deflection inside the vidicon, supplying it to the horizontal deflection coil.

Details

The horizontal scanning start (Hs) pulse supplied from the Process circuit board (YWV3110PZK2) goes via inverter Q115 to horizontal deflection output Q116. When Q116 is switched by the Hs pulse from Q115, the collector current pulse of Q116 resonates with L102 and C139, and the resultant horizontal sawtooth current is supplied to the horizontal deflection coil through pin 6 of CN111. VR105 (H. SIZE) is a control for adjusting the horizontal scanning size.

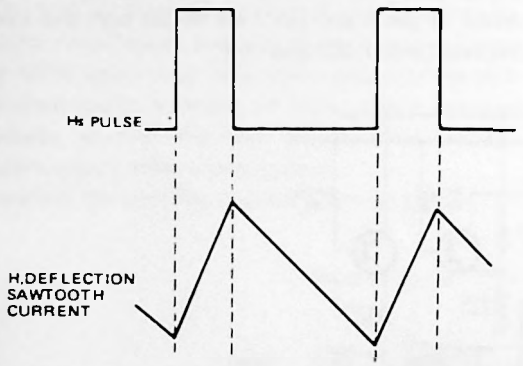


Fig. 3-13-1 Horizontal Deflection

3-14. Horizontal Linearity Correction Circuit

Outline

The horizontal (H) deflection circuit is of a switching type, so that the generated sawtooth current waveform has poor linearity. By feeding the sawtooth current to the deflection coil, the intensity of the magnetic field generated in the deflection coil is not linear as the vidicon's electron beam is deflected.

If a linear sawtooth current Ⓐ is sent to the deflection coil, however, the magnetic field in the scanning start portion is distorted Ⓑ due to the effect of the vidicon's electrodes, coil hysterisis, etc. As a result, the linearity of the scanning start portion deteriorates, and a shading (unevenness of amplitude) appears on the left edge of the picture.

Therefore, in order to generate a linear magnetic field intensity Ⓓ and to correct the linearity and shading of the scanning start portion, it is necessary to feed a nonlinear sawtooth signal Ⓒ to the deflection coil.

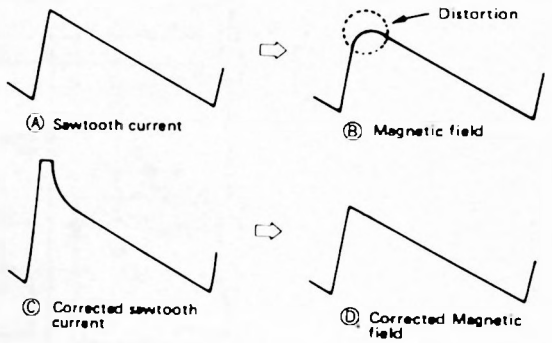


Fig. 3-14-1 Horizontal Linearity Correction-1

This circuit, generates a waveform to "correct" the linearity of horizontal sawtooth current waveform and its starting portion. As shown in Fig. 3-14-2, the horizontal deflection circuit is connected to one end of the horizontal deflection coil, and the horizontal linearity correction circuit to the other end.

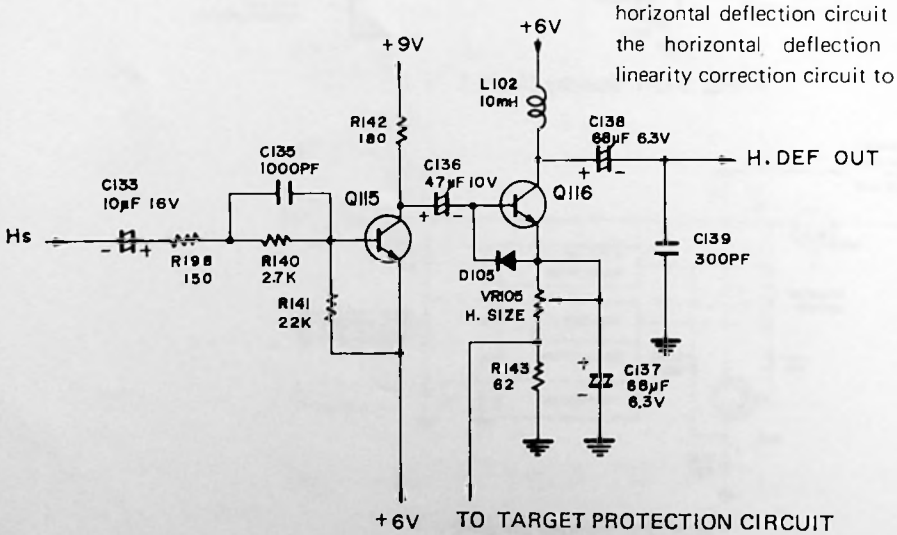


Fig. 3-13-2 Horizontal Deflection Circuit

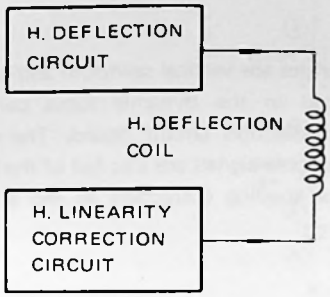


Fig. 3-14-2
Horizontal Linearity Correction-2

Details

The horizontal flyback pulse Ⓔ produced from the collector of Q116 in the horizontal (H) deflection circuit is integrated by L103 and R145 into a sawtooth signal Ⓕ.

This sawtooth signal is again integrated by L103, R149 and C142 into a parabola signal Ⓖ, which is applied through VR112 (H. LIN-1) to pin 6 of differential amplifier IC105 (1/2) as a horizontal linearity correction signal.

The horizontal flyback pulse Ⓔ from Q116 is integrated by R148 and C140 into a linearity correction signal Ⓗ for correcting the linearity of the starting portion of the horizontal sawtooth current waveform. The starting portion linearity correction signal Ⓗ is applied to pin 5 of IC105 where the linearity correction signal Ⓖ and the starting portion linearity correction signal Ⓗ are mixed and amplified.

The mixed signal Ⓘ of these linearity correction signals at pin 7 of IC105 is fed to the horizontal deflection coil to correct the linearity of the horizontal sawtooth current waveform.

VR112 (H. LIN-1) is a control for adjusting the overall linearity of sawtooth signal and VR106 (H. LIN-2) for adjusting the linearity of the starting portion. VR107 (H. CENTERING) is a centering control which controls the positive input potential of IC105 to change the direct current flowing to the deflection coil, and thus sets the horizontal scanning position on the vidicon.

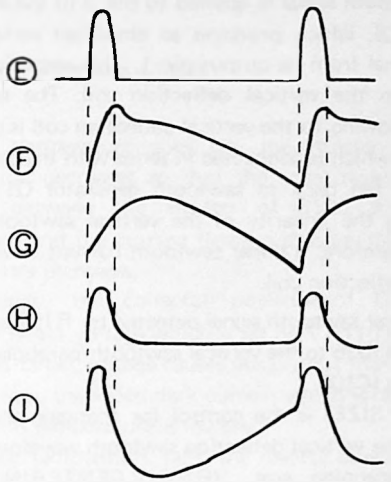


Fig. 3-14-3
Horizontal Linearity Correction-3

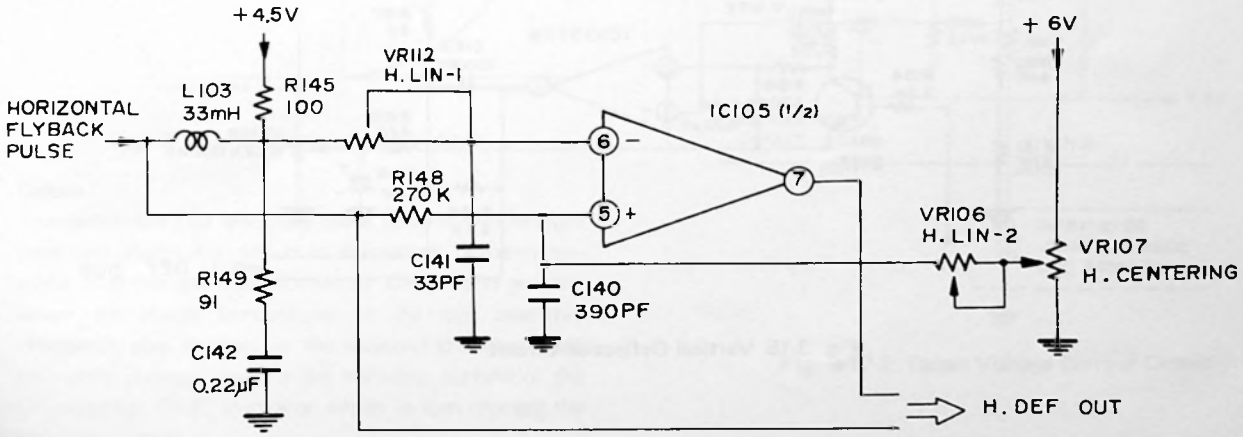


Fig. 3-14-4 Horizontal Linearity Correction Circuit

3-15. Vertical Deflection Circuit

Outline

This circuit generates a sawtooth current for the vertical(V) beam deflection inside the vidicon, feeding it to the vertical deflection coil.

Details

The vertical scanning start(Vs) pulse sent from the Process circuit board (YWV3110PZK2) is fed to sawtooth generator Q117 which converts it into a vertical rate sawtooth.

This sawtooth signal is applied to pin 2 of the amplifier IC105(1/2), which produces an amplified vertical sawtooth signal from its output pin 1. This amplified signal is sent to the vertical deflection coil. The sawtooth current flowing to the vertical deflection coil is detected by R157 which is connected in series with the deflection coil, and fed back to sawtooth generator Q117, thus correcting the linearity of the vertical sawtooth waveform. Therefore, a linear sawtooth current flows in the vertical deflection coil.

The vertical sawtooth signal detected by R157 is applied through R1035 to the vertical sawtooth/parabola generator circuit IC106.

VR108(V.SIZE) is the control for changing the amplitude of the vertical deflection sawtooth waveform to set vertical scanning size. VR109(V.CENTERING) is a centering control which controls the direct current flowing to the vertical deflection coil to set the vertical scanning position on the vidicon.

3-16. Vertical Sawtooth/Parabola Generator Circuit

Outline

This circuit generates the vertical sawtooth and parabola waveforms needed in the dynamic focus correction circuit on the Deflection circuit board. The vertical sawtooth and parabola signals are also fed to the Process circuit board for shading correction of red and blue signals.

Details

The vertical(V) deflection sawtooth signal generated in the vertical deflection circuit is fed to pin 3 of IC106 where it is amplified. The amplified V.sawtooth signal at pin 1 of IC106 is supplied to the miller integrator consisting of IC106 (1/2), R1031 in BR103, R165, C150 and C151, and converted into a V. parabola signal. The V. sawtooth signal and V. parabola signal at pin 1 and pin 7 of IC106 are applied respectively to the wiper arms of VR134 (V. SAWTOOTH) and VR133 (V. PARABOLA) in Variable Resistor Block BVR1 in the dynamic focus correction circuit, and the Process circuit board through terminal No. 4 and No. 5 of BI101 for the shading correction of red and blue signals.

The V. sawtooth signal is also supplied to the target protection circuit.

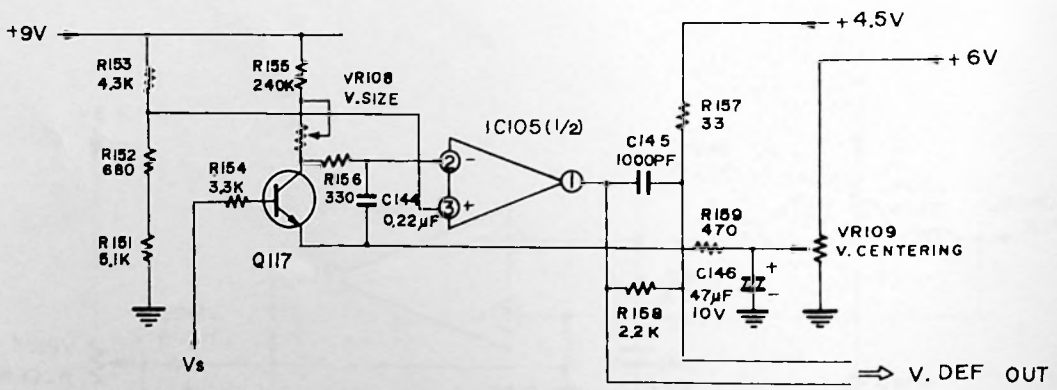


Fig. 3-15 Vertical Deflection Circuit

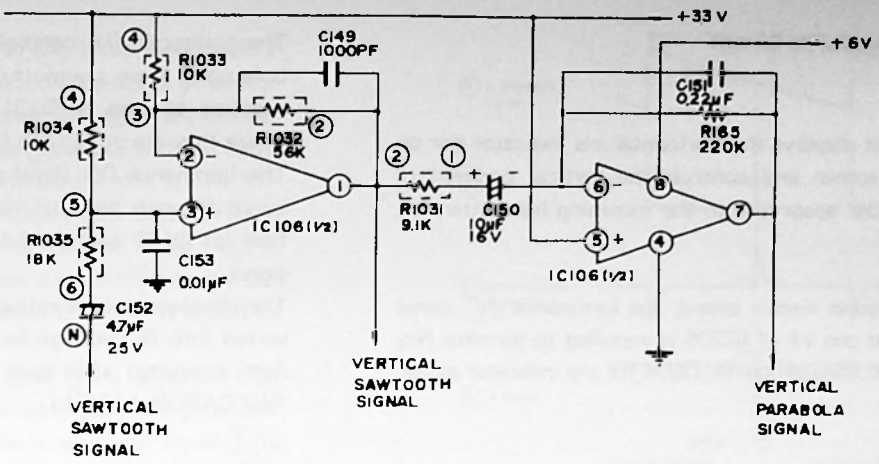


Fig. 3-16 Vertical Sawtooth/Parabola Generator Circuit

3-17. Target Voltage Control Circuit

Outline

The pick-up tube gives out an output signal which corresponds to the incoming light intensity. Even when no light reaches the tube, an output signal, called dark current is produced. The vidicon's dark current is relatively large and varies according to the vidicon temperature so that the black level of the output signal tends to drift causing color shift.

The target voltage control circuit detects the vidicon's temperature variation, and controls the target voltage according to the temperature drift, and thus reduces dark current variations.

This circuit, and the optical black clamp circuit minimize the black level variations.

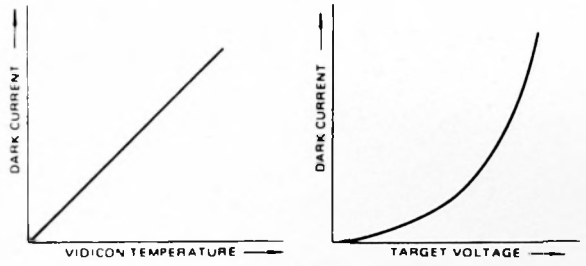


Fig. 3-17-1 Characteristic of Vidicon

Details

The deflection coil assembly has a built-in temperature detecting thermistor which is connected between terminal 1 of the multi-pin connector CN111 and ground. When the inside temperature of the coil assembly changes(it also changes in the vidicon) the thermistor resistance changes, causing the collector current of the DC amplifier Q120 to change which in turn changes the collector voltage.

The target voltage applied to the vidicon is set by VR110 (TARGET).

If the temperature goes up, the resistance of the thermistor decreases so that the total resistance connected between the emitter of Q120 and ground decreases, and the current flowing through the collector and emitter increases.

Accordingly, the collector potential of Q120 falls, and the target voltage which is set by VR110 is reduced. Reduced target voltage causes less output from the tube. In this way, the video dark current which is raised by an increase in temperature is lowered.

When the temperature falls, the reverse operation takes place.

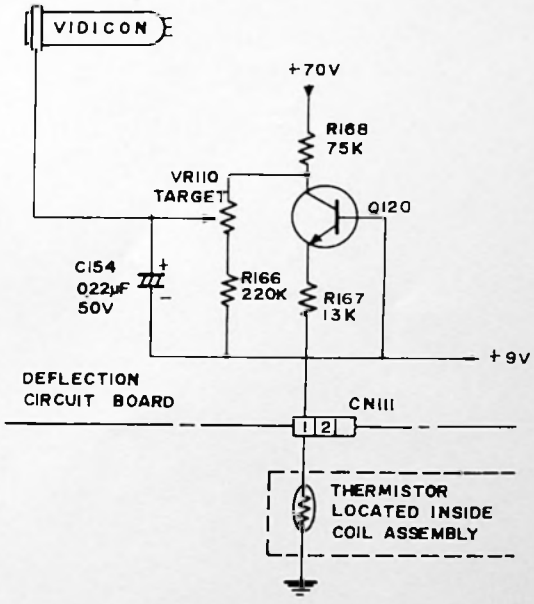


Fig. 3-17-2 Target Voltage Control Circuit

3-18 Iris Indicator Circuit

Outline

This circuit displays the horizontal iris indicator bar on the CRT screen and controls the vertical position of indicator bar according to the incoming light intensity.

Details

In the process circuit board, the luminance (Y) signal obtained at pin 14 of IC205 is supplied to terminal No. 6 of CN206 through buffer Q204 for iris indicator signal.

The horizontal (H) parabola signal and vertical (V) parabola signal from sawtooth/parabola generator circuit are supplied to base of Q131 through R1527 and R1528 where they are mixed and fed to Q132.

The luminance (Y) signal supplied from process circuit board through terminal No. 6 of BI101 is supplied to base of Q132 and modulated by the mixed parabola signal.

Then the modulated luminance signal is rectified and converted into DC voltage (corresponding to the incoming light intensity) after level controlled by VR121 (IRIS INDICATOR LEVEL).

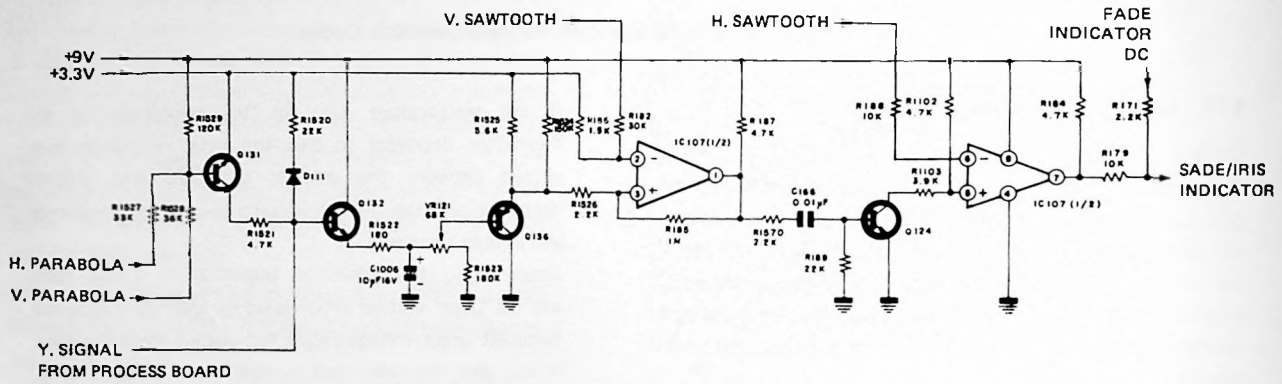


Fig. 3-18-1 Iris Indicator Circuit

The vertical (V) sawtooth signal (A) is supplied to pin 2 of IC107 from the vertical sawtooth/parabola generator circuit. The DC voltage and V. sawtooth signal are compared in IC107 (1/2) and V. pulse (B) whose width is controlled by the DC voltage is generated at pin 1. The V. pulse (B) is then supplied to switching amp Q124 through the differentiator consisting of C166 and R189 ((C)), and the V. pulse (D) whose phase is controlled by the DC voltage is obtained at the collector of Q124. It is sent to pin 5 of IC107.

The horizontal (H) sawtooth signal (E) is fed to pin 6 of IC107 from the horizontal sawtooth/parabola generator circuit. The V pulse (D') and the H. sawtooth signal (E) is compared in IC107 ((F)) and the iris indicator signal (G) is generated at pin 7 of IC107.

In this way, the indicator bar moves vertically on the CRT screen indicating the incoming light intensity when the incoming light intensity changes.

The indicator signal is then mixed with the fade indicator control DC through R179 and R171 and fed to the viewfinder circuit through terminal No. 3 of CN109 and terminal No. 3 of EVF connector CN802.

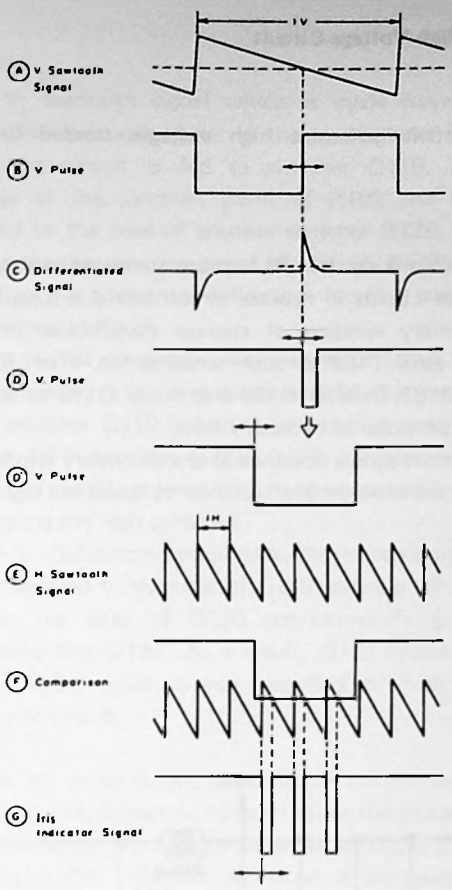


Fig. 3-18-2 Iris Indicator Signal

3-19. High Voltage Circuit

Outline

This circuit generates high voltages needed for the vidicon.

Details

The pre blanking (pre BL) pulse generated in the pulse generator circuit in Process circuit board is supplied to the primary winding of step-up transformer in high voltage pack T102 through terminal No. 1 of BI103, buffer Q127, inverter Q129 and driver Q118 to step up the pre BL pulse to necessary level.

The boosted pulses obtained at the secondary winding of step-up transformer are rectified to generate high voltages.

The high voltages are derived as follows.

The −60V obtained at pin 6 of T102 is fed to grid-1 (G1) through VR114 (BEAM). The +340V at pin 4 of T102 is applied to.grid-2 (G2) directly. +1.5KV obtained at pin 3 of T102 is supplied to grid-6 (G6) through R199. The voltages for grid-4 (G4) and grid-5 (G5) are obtained by dividing +1.5KV by block resistor BR104 and VR116 (FOCUS). +6V is fed to the heater.

Q128 prevents a beam spot appearing on the vidicon for a while after the Power switch is turned OFF.

In the operating condition. Q128 is energized and the proper voltage for grid-1 (G1) of vidicon is set between +9V and −60V by VR114. When the power switch is turned OFF, Q128 becomes OFF and VR114 is disconnected from the +9V line. Therefore, −60V charged into the capacitor inside T102 is not discharged and −60V is fed to G1 of vidicon. In this way, the electron beam is blocked preventing beam spot on the vidicon. The +70V obtained at pin 5 of T102 is fed to the cathode blanking circuit, dynamic focus correction circuit and target voltage control circuit.

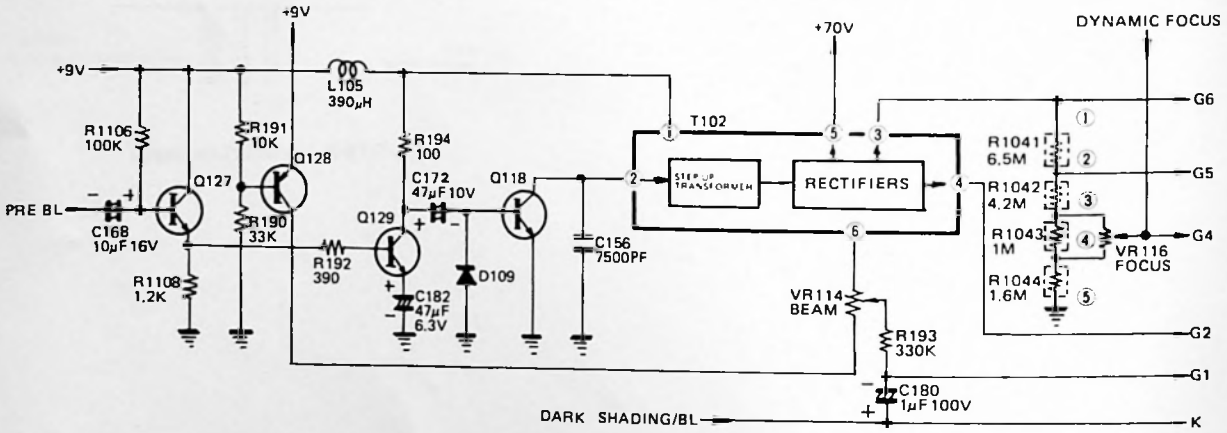


Fig. 3-19 High Voltage Circuit

3-20. Target Protection Circuit

Outline

If no deflection current flows to the vidicon deflection coil because of a horizontal(H) or vertical(V) deflection circuit failure, the scanning process would stop, and the vidicon electron beam would remain stationary.

Should this happen, the photoconductive layer of the vidicon would be burned in one spot, making the vidicon unusable.

The vidicon target protection circuit protects the photo-conductive layer from burn-out in the event of a deflection circuit failure by stopping the generation of high voltages supplied to the vidicon grids and thus cutting off the electron beam.

Details

The V. sawtooth signal which is made from the V. deflection sawtooth signal in the V. sawtooth/parabola generator circuit is fed to switcher Q119. The DC voltage at the junction point of R162 and R163 is applied to the base of another switcher Q126. The DC voltage at the junction point of VR105 (H. SIZE) and R143 in the horizontal deflection circuit is supplied to the emitter of Q126.

Under normal conditions, the emitter of Q126 is biased approximately 1.9V, and the base of Q126 approx. 1.5V since switcher Q119 is turned ON. In this case, Q126 is turned OFF and the buffer Q127 operates normally. Thus the pre BL pulse is sent to the high voltage circuit generating the high voltages.

If the V. Deflection circuit fails, the V. sawtooth signal is not applied to the base of Q119, turning OFF Q119, biasing the base of Q126 approximately 2.6V and switching ON Q126. As a result, Q127 becomes OFF and pre BL pulse is not supplied to high voltage generator circuit.

If the Hs pulse is not supplied to the H. deflection circuit, the H. deflection circuit fails or the coil assembly is disconnected, the emitter potential of Q126 is lowered turning it ON. The pre BL pulse is not supplied to generate the high voltages.

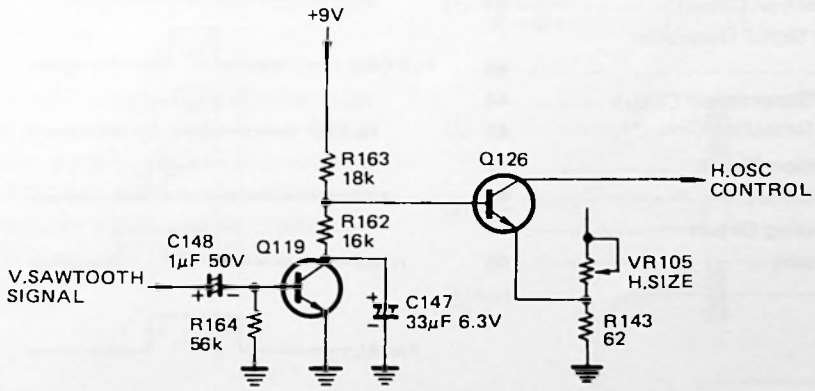


Fig. 3-20 Target Protection Circuit

4. Process Circuit Board (YWV3110PZK2)

The Process Circuit Board (YWV3110PZK2) contains following circuits.

4-1. Pulse Generator Circuit

Outline

This circuit generates all sync pulses used in the camera.

Details

The crystal oscillator which consists of crystal oscillator X201, VC202 (3.58MHz ADJ), C246 and C248, connected between pin 3 and pin 4 of sync generator IC211 oscillates 14.3MHz. The following pulses are generated from IC211.

Pin 5 :	SC0°	(0° phase subcarrier)
pin 6 :	SC90°	(90° phase subcarrier)
pin 7 :	Pre BL	(Preblanking pulse)
pin 8 :	CP	(Clamp pulse)
pin 9 :	Hs	(Horizontal scanning start pulse)
pin 10:	BFP	(Burst flag pulse)
pin 11:	Gsc	(Gated subcarrier)
pin 12:	Vs	(Vertical scanning start pulse)
pin 13:	BL	(Composite blanking pulse)
pin 15:	W.BL	(Wide blanking pulse)
pin 16:	Sync	(Composite sync pulse)

The relative timing information for each pulse is shown in Fig. 4-1-1.

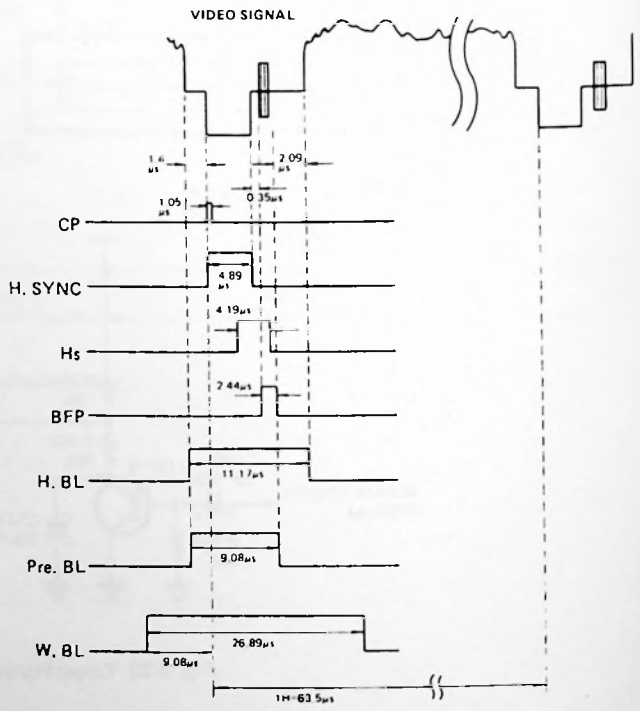


Fig. 4-1-1 Pulses

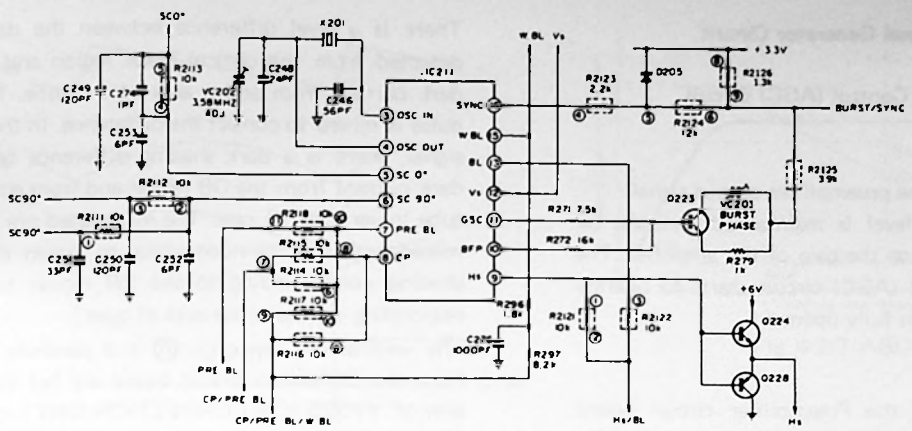


Fig. 4-1-2 Pulse Generator Circuit

VC202 (3.58MHz ADJ) is a control for setting the subcarrier frequency.

The SC0° and SC90° are respectively supplied to other circuit, through integrators consisting of R2113 and C249, R2111 and C251, and R2112 and C250.

The preblanking (Pre BL) pulses are fed to other circuit as follows. The Pre BL pulse is fed through R2118 to other circuit. The Pre BL pulse Ⓐ through R2114 is mixed with the clamp pulse (CP) Ⓑ through R2115. Also the Pre BL pulse through R2117 is mixed with the CP through R2116, and wideblanking (W. BL) pulse Ⓓ through R296/R297. Then the multiplexed signals Ⓒ and Ⓔ are supplied to other circuits.

The Hs pulse is fed to the Deflection circuit board through buffer Q224 and Q228.

The Vs pulse is also supplied to the Deflection circuit board.

The multiplexed signal Ⓗ which is made by mixing the Hs pulse Ⓕ and the BL pulse Ⓖ through R2121 and R2122 is fed to other circuits.

The Gsc signal Ⓘ and the BFP Ⓙ are mixed through R271 and R272 resulting in a burst signal Ⓚ. The burst signal thus generated is supplied to phase shifter Q223. The phase-shifted burst signal at the junction point of VC203 (BURST PHASE) and R279 is then mixed with the sync pulse Ⓛ through R2125 and R2123/R2124. The mixed signal Ⓜ is supplied to the burst/sync mix inside IC207 through pin 7.

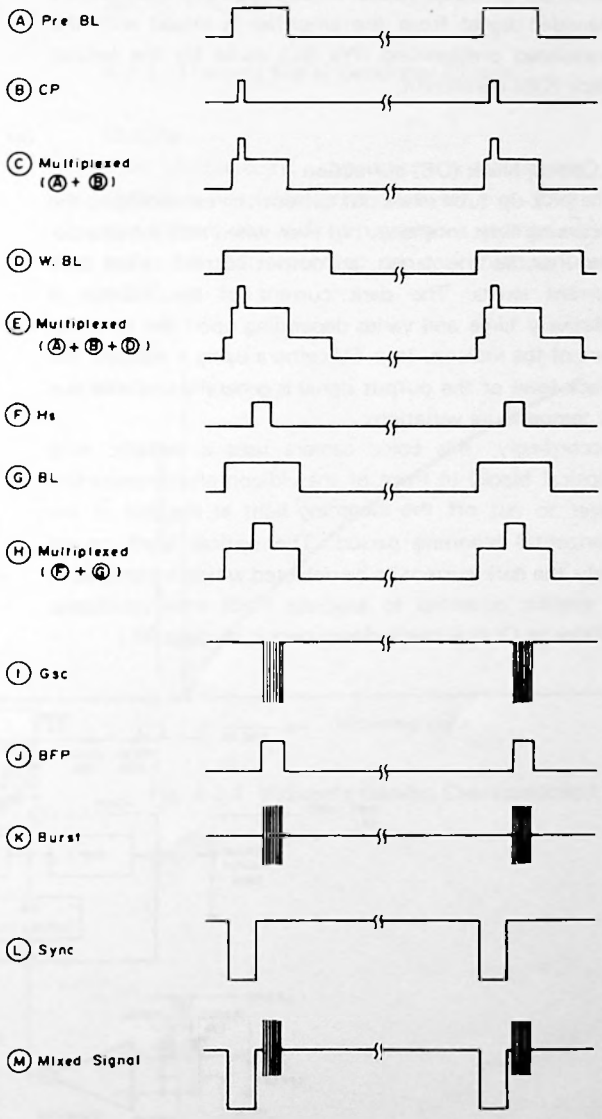


Fig. 4-1-3 Mixed Signals

4-2. AGC/Tracking Signal Generator Circuit

4-2-1. Automatic Gain Control (AGC) Circuit

Outline

This circuit amplifies the preamplifier output signal.
The amplified signal level is maintained constant by automatically controlling the gain of the amplifier. The automatic gain control (AGC) circuit starts to operate only when the lens iris is fully opened.

Details

The output signal of the Preamplifier circuit board (YWCC007ZK05) goes to terminal No. 4 of CN201. After its level is set by VR220 (INPUT GAIN), it goes to the amplifier inside IC205 through pin 2. The amplified pre-video signal from the amplifier is mixed with the modulated preblanking (Pre BL) pulse for the optical black (OB) correction.

• Optical black (OB) correction

The pick-up tube sends out current corresponding to the incoming light intensity, but even when no light whatsoever reaches the target, an output current called dark current exists. The dark current of the vidicon is relatively large and varies depending upon the temperature of the vidicon. In a TV camera using a vidicon, the black level of the output signal is generally unstable due to temperature variations.

Accordingly, this color camera uses a metallic strip (optical black) in front of the vidicon photoconductive layer to cut off the incoming light at the end of the horizontal scanning period. The optical black causes only the dark current to be detected which is clamped at a specific potential to suppress black level variations. (Refer to Optical black clamp circuit on page 30.)

There is a level difference between the dark current detected from the optical black region and the actual dark current from active area of the tube. The pre BL pulse is mixed to correct the difference. In the pre-video signal, there is a dark shading difference between the dark current from the OB region and from active area of tube in vertical (V) rate. The modulated pre BL pulse is mixed with the pre-video signal to match the V. dark shading corresponding to the OB region to that corresponding to the active area of tube.

The vertical (V) sawtooth Ⓐ and parabola Ⓑ signals from the Deflection circuit board are fed to the wiper arm of VR225 (OB CORRECTION-SAW.) and VR226 (OB CORRECTION-PARA.) respectively. These waveforms are applied to both the non-inverted (pin 3) and inverted (pin 2) inputs of IC206 (1/2), where they are amplified. The output of IC206 (1/2) at pin 1 produces a positive or negative mixed signal Ⓒ of V.sawtooth and parabola signals depending on the position of these controls. The signal Ⓒ is then fed to the OB correction circuit inside IC205 through pin 3.

VR227 (OB OFFSET) controls the positive input potential of IC206 to change the output DC level.

The multiplexed signal of the clamp pulse (CP) and pre BL pulse is fed from the pulse generator circuit to the CP/Pre BL separator inside IC205 through pin 7, where the CP and Pre BL pulse are separated. The separated pre BL pulse is fed to the OB correction circuit inside IC205. The amplified pre-video signal Ⓓ is then modulated by the mixed signal Ⓒ and pre BL signal for correcting the difference of dark current level and matching the dark current shading (Ⓔ & Ⓕ).

VR225 and VR226 are controls for matching the dark current shading and VR227 is for correcting the difference of dark current level.

The corrected pre-video signal is then fed to the automatic gain control (AGC) circuit inside IC205.

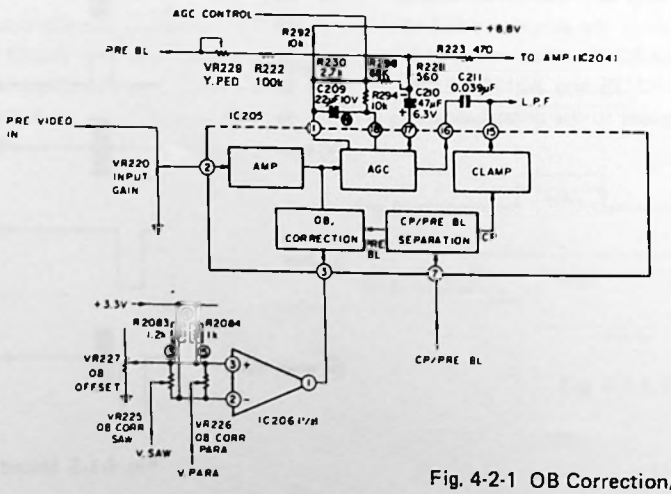


Fig. 4-2-1 OB Correction/AGC Circuit

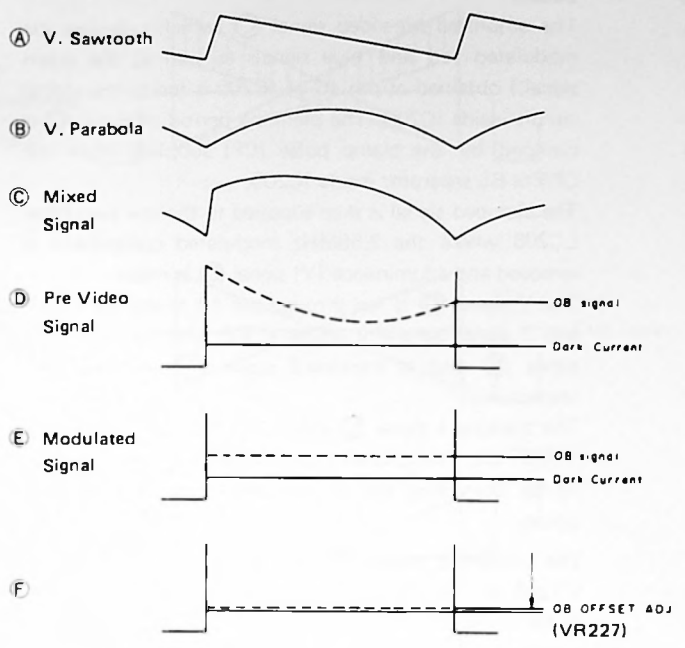


Fig. 4-2-2 OB Correction

• Automatic gain control (AGC) Circuit

The DC voltage which supplied from the AIC driver inside IC204 to automatic iris control (AIC) lens to control its iris opening is also supplied to the AGC amplifier inside IC205 through pin 18 of IC205 through CN208.

In order to open the iris, the iris control voltage must be increased.

When the AIC lens works properly, the relatively low DC voltage is supplied to the AGC amplifier from the AIC driver and AGC amplifier becomes fixed gain amplifier. The amplified signal is fed through pin 17 of IC205 and pin 18 of IC204 to the 14dB amplifier inside IC204.

When the camera is pointed at a weakly illuminated scene, the iris control voltage is increased to open the lens iris. However, the lens iris becomes fully open at a certain iris control voltage and cannot be opened any more even when the DC voltage is increased. When the lens iris is wide open by the increased DC voltage, the AGC amplifier assumes a differential amplifier configuration whose gain is automatically controlled by the DC voltage supplied through pin 18 to keep the signal level constant.

In this way, the signal level corresponding to normal and relatively high illumination is kept constant by the lens iris opening while the signal level corresponding to relatively low illumination is controlled by the AGC circuit.

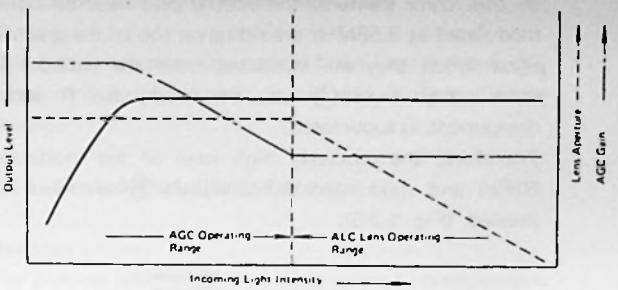


Fig. 4-2-3 AGC Operation

The amplified pre-video signal from the AGC amplifier is also fed to the tracking signal generator circuit through pin 16 of IC205.

4-2-2. Tracking Signal Generator Circuit

Outline

The photoelectric conversion characteristic of the vidicon is not linear. The relatively high level of video signal from the vidicon undergoes greater suppression than that corresponding to dark picture part. (Fig. 4-2-4).

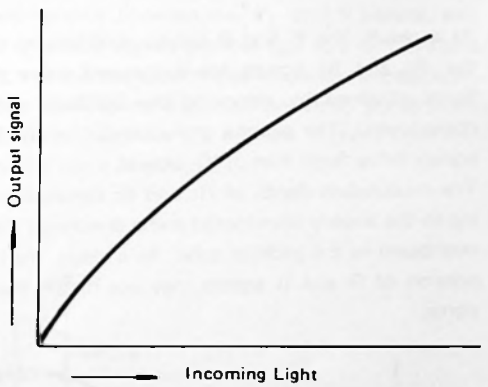


Fig. 4-2-4 Vidicon's Gamma Characteristic-1

In this color camera, the red(R) and blue(B) signals modulated at 3.58MHz are riding on top of the green(G) signal when they are extracted from the vidicon. So, signal's high level Ⓐ i.e., the modulated R and B component, is suppressed.
Therefore, the relatively high level of the modulated R(Rc) and modulated B(Bc) signals Ⓑ are also suppressed. (Fig. 4-2-5).

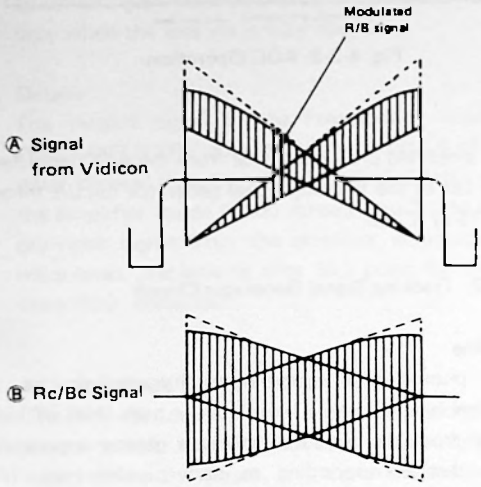


Fig. 4-2-5 Vidicon's Gamma Characteristic-2

As a result, the R and B signals obtained by detecting the Rc and Bc signals are suppressed more than Y_L signal obtained by removing the 3.58MHz modulated component. (The gamma characteristic of the R and B signals differ from that of Y_L signal).
The modulation depth of Rc and Bc signals corresponding to the weakly illuminated scene is reduced due to the over-beam in the pick-up tube. As a result, the low level portion of R and B signals may not match that of Y_L signal.

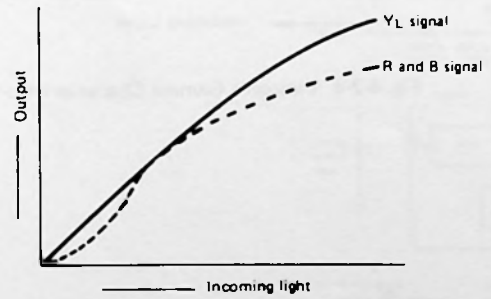


Fig. 4-2-6 Vidicon's Gamma Characteristic-3

The circuit generates the tracking signals for correcting the gamma characteristic of the R and B signals, and matching them with the Y_L signal.

Details

The amplified pre-video signal Ⓒ (which contains the modulated red and blue signals as well as the green signal.) obtained at pin 16 of IC205 is fed to the clamp circuit inside IC205. The blanking period of signal Ⓒ is clamped by the clamp pulse (CP) supplied from the CP/Pre BL separator inside IC205.
The clamped signal is then supplied to the low pass filter LC208 where the 3.58MHz modulated component is removed and a luminance (Y) signal Ⓓ is made.
The Y signal Ⓓ is fed through pin 14 to the tracking-1 and 2 signal generator inside IC205 where a tracking-1 signal Ⓔ and a tracking-2 signal Ⓕ are generated respectively.
The tracking-1 signal Ⓔ at pin 9 of IC205 is supplied to VR207 (R. TRACKING-1) and VR206 (B. TRACKING-1) for correcting the relatively low level of R and B signals.

The tracking-2 signal Ⓕ at pin 8 of IC205 is fed to VR205 (R. TRACKING-2) and VR204 (B. TRACKING-2) for correcting the relatively higher portion of R and B signals.

The Y signal Ⓓ is also applied to the tracking-3 signal generator inside IC205 through pin 13. The tracking-3 signal Ⓖ at pin 11 of IC205 is fed to VR203 (R. TRACKING-3) and VR202 (B. TRACKING-3) for the high level of R and B signals.

The tracking-3 signal is also fed to the high Y level chroma clip circuit inside IC208 through LC202 which delays the tracking-3 signal to match the chrominance signal in phase.
The DC voltage which is set by VR219 (TRACKING-3 SET) and supplied to the tracking-3 signal generator through pin 12 determines the clip level for the tracking-3 signal.

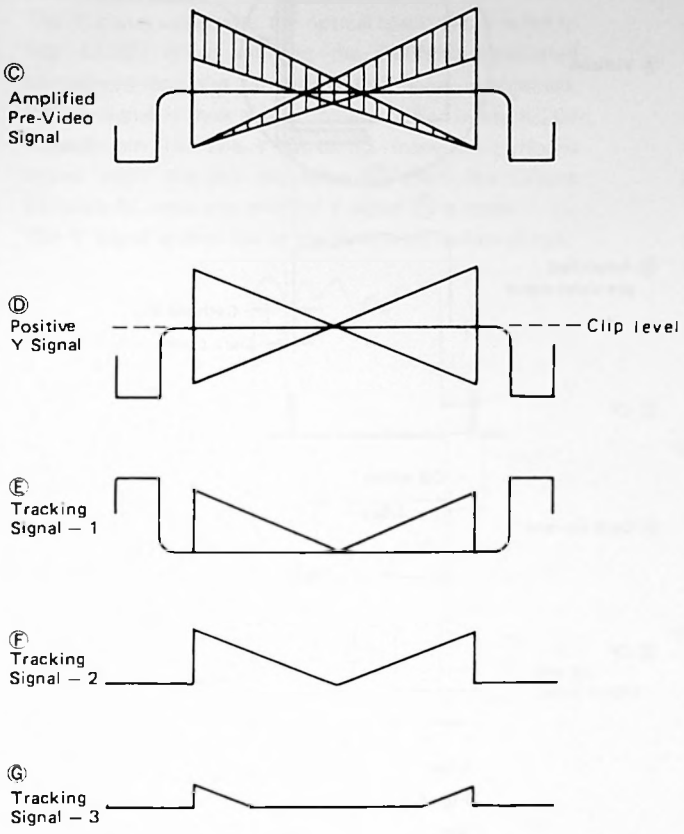


Fig. 4-2-7 Tracking Signals

4-3. Luminance Signal Processing Circuit

This circuit contains the optical black clamp circuit, Y_H signal circuit, Y_L signal circuit and Y (edge) signal circuit.

4-3-1. Optical Black Clamp Circuit

Outline

The pick-up tube sends an output current corresponding to the incoming light intensity, but even when no light reaches the target, an output current called dark current is obtained. The dark current of the vidicon is relatively large and varies with the temperature of the vidicon. In a TV camera using a vidicon, the dark level of the output signal is extremely unstable with respect to changing temperature.

In a color camera using the single carrier frequency multiplexing system, the red(R) and blue(B) signals modulated at 3.58MHz are riding on top of the green(G) signal. Thus the black level of the R and B signals are free from temperature variations because they are independent of vidicon dark current.

However, the black level of the Y signal which is obtained by removing the modulated R and B components from the vidicon output increases or decreases according to temperature variations. Therefore, the black level balance between the Y_L and R signals, and between Y_L and B signals are lost due to a temperature variations and this causes a change in color reproduction. This circuit receives the amplified pre-video signal from the AGC circuit and clamps its dark current level for correcting the black level variation.

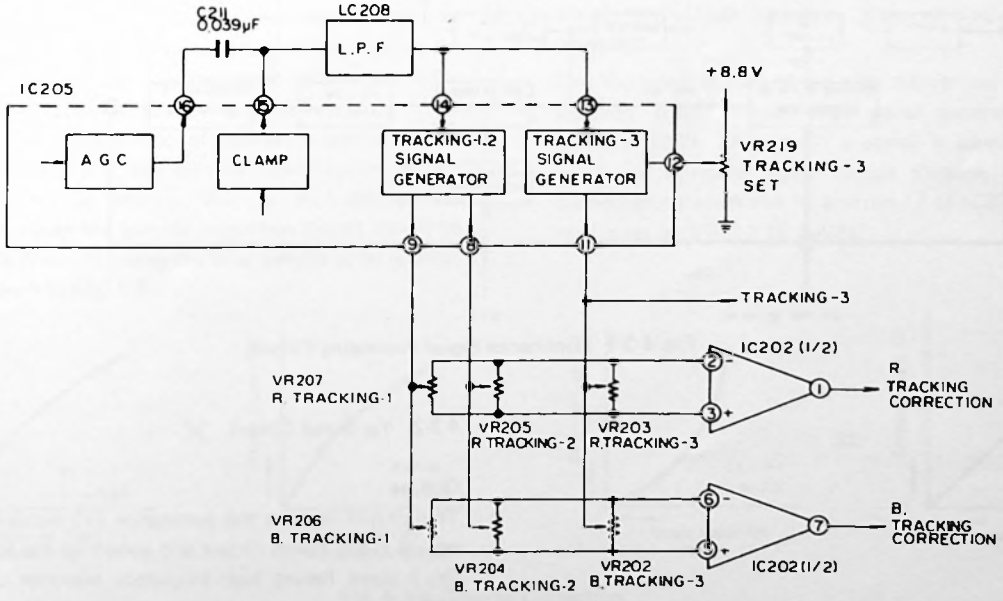


Fig. 4-2-8 Tracking Signal Generator Circuit

Details

The amplified pre-video signal which contains the modulated red/blue signals and green signal is fed from the AGC amplifier inside IC205 to the 14dB amplifier through pin 17 of IC205 and pin 18 of IC204. The amplified signal is fed through pin 17 of IC204 and C208 to optical black (OB) clamp circuit inside IC204. A metallic strip (optical black) for cutting the incoming light at the end of the horizontal scanning period is built into the vidicon faceplate.

When the beam scans the optical black portion Ⓐ, the dark current of the vidicon is produced and this signal portion Ⓑ is clamped to a fixed DC potential, so that the black level variation due to a change of dark current is sensed.

In other words, the dark current level Ⓐ' of the amplified pre-video signal Ⓑ supplied to the clamp circuit inside IC204 is clamped by the clamp pulse (CP) Ⓒ' separated from the multiplexed signal of CP, pre BL and wide BL pulses, inside IC204. (The multiplexed signal of CP, pre BL and wide BL pulses are generated in the pulse generator circuit and mixed, then fed to the CP/pre BL/wide BL separator where they are separated.) Therefore, even if the dark current level drift due to the temperature variations, the DC potential of the optical black (OB) level is held constant.

In this way, the black level variation is corrected.

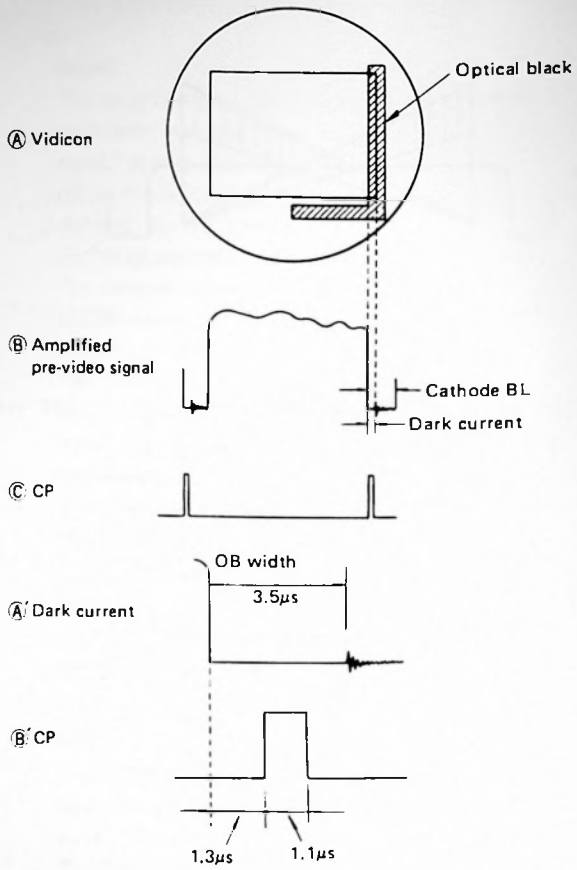


Fig. 4-3-2 OB Clamp

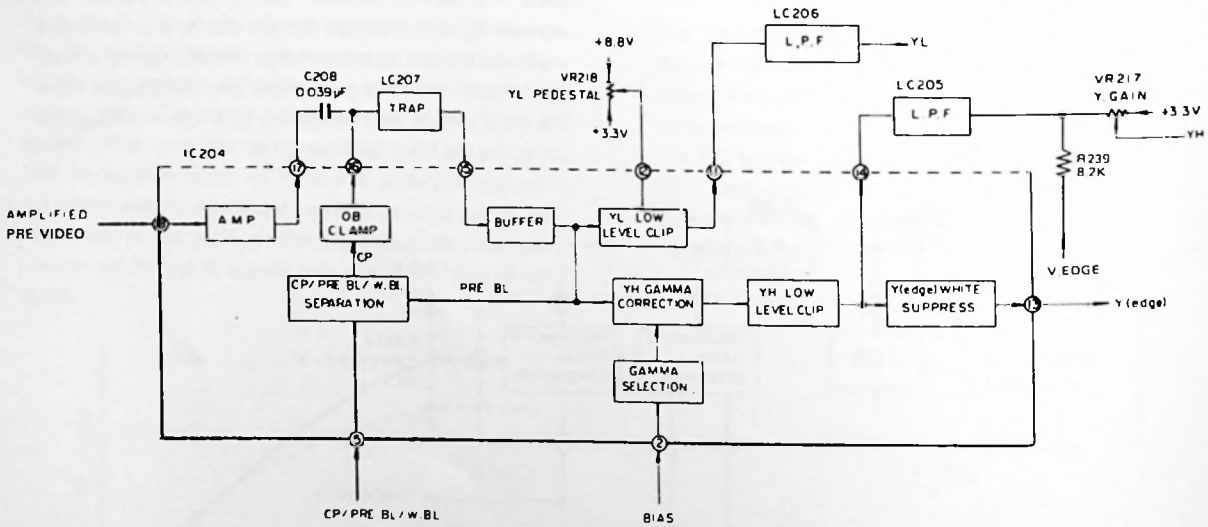


Fig. 4-3-1 Luminance Signal Processing Circuit

4-3-2. Y_H Signal Circuit

Outline

This circuit receives the luminance (Y) signal from the optical black clamp circuit and generates the luminance (Y_H) signal having high frequency response characteristic.

Details

The Y signal undergoes the optical black clamp is fed to trap LC207 which removes the 3.58MHz modulated component and the luminance (Y) signal is obtained. The Y signal is then applied to the buffer inside IC204 through pin 15. The Y signal Ⓓ from the buffer is mixed with the pre BL pulse Ⓔ from the CP/pre BL/wide BL separator and the Y signal Ⓕ is made.

The Y signal is then fed to the gamma correction circuit.

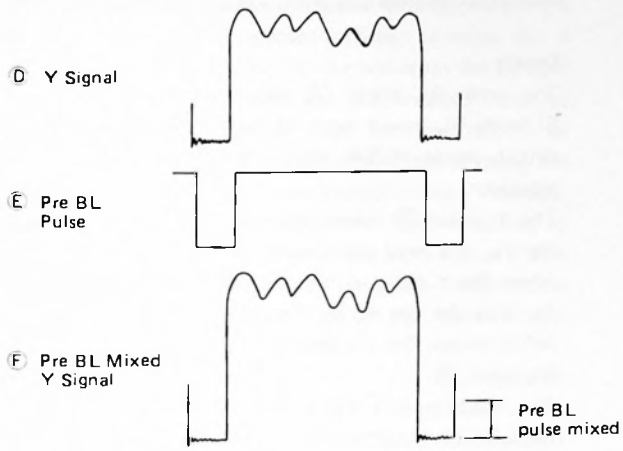


Fig. 4-3-3 Preblanking Mix

Details

The Y signal mixed with the pre BL pulse is fed to the gamma (γ) correction circuit and undergoes the gamma correction. The suppression level and the extent of suppression for the gamma correction are selected by the gamma select circuit inside IC204, which is controlled by the DC voltage at pin 2 of IC204.

The Y signal Ⓖ which undergoes the gamma correction is supplied to the low level clip circuit inside IC204, where the low level preblanking portion of the signal is clipped Ⓗ and its pedestal level is set.

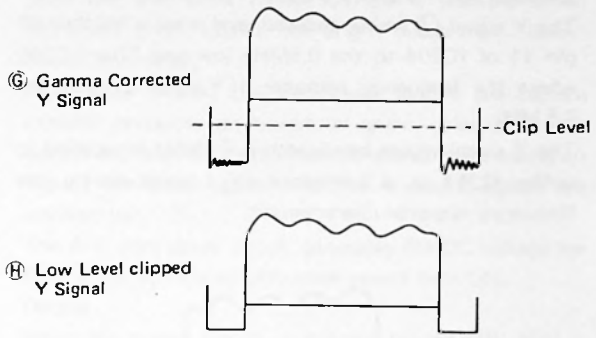


Fig. 4-3-5 Low Level Clip

• Gamma correction circuit

Outline

This circuit matches the non-linearity of vidicon's photoelectric conversion characteristic to that of cathode ray tube (CRT) and reproduces a linear picture of high fidelity on the monitor.

In order for a televised picture to have the same contrast gradation as the original scene, the system (including the pick-up tube, signal processing inside camera and monitor, and CRT) gamma must be equal to 1.

The gamma characteristic of vidicon is approximately (approx.) 0.65 and the gamma characteristic of the monitor CRT is approx. 2.2, so that the gamma characteristic of the gamma correction circuit should be approx. 0.7, which makes the total gamma to be approx. 1.0 as shown in Fig. 4-3-4.

The Y signal whose pedestal level is set is supplied to 2.8MHz low pass filter LC205, where the frequency response of Y signal is limited to 2.8MHz and its phase is delayed to match the chrominance signal, and the Y_H signal having high frequency response characteristic is generated.

The Y_H signal is then mixed with the vertical edge signal supplied from vertical edge signal generator circuit through R239. Then the Y_H signal is supplied to the horizontal aperture signal circuit through the buffer connected between pin 16 and pin 17 of IC207, after its level is set by VR217 (Y GAIN).

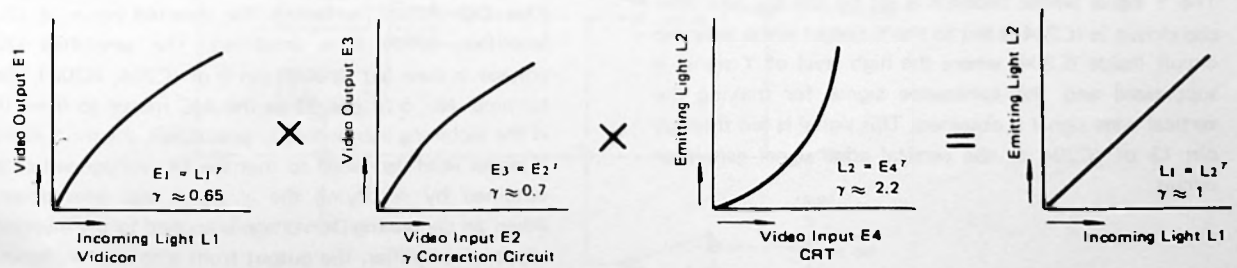


Fig. 4-3-4 Gamma Correction

4-3-3. Y_L Signal Circuit

Outline

This circuit receives the luminance (Y) signal from the Y signal circuit, and generates the luminance (Y_L) signal having low frequency response characteristic.

Details

The Y signal Ⓘ mixed with the preblanking (pre BL) pulse is fed to the low level clip circuit inside IC204, where the Y signal's low level preblanking portion is clipped and its pedestal level is set (Ⓙ). The clip level (pedestal level) is set by VR218 (Y_L PEDESTAL).

The Y signal Ⓙ whose pedestal level is set is fed through pin 11 of IC204 to the 0.5MHz low pass filter LC206 where the frequency response of Y signal is limited to 0.5 MHz.

The Y signal whose bandwidth is 0.5MHz is supplied to buffer Q214 as a luminance (Y_L) signal having low frequency response characteristic.

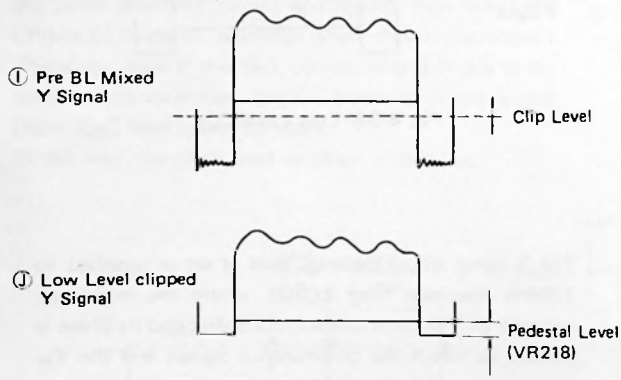


Fig. 4-3-6 Pedestal Level

4-3-4. Y(edge) Signal Circuit

Outline

This circuit generates the luminance [Y(edge)] signal for making the vertical edge signal.

Details

The Y signal whose pedestal is set by the Y_H low level clip circuit in IC204 is fed to the Y (edge) white suppress circuit inside IC204, where the high level of Y signal is suppressed and the luminance signal for making the vertical edge signal is obtained. This signal is fed through pin 13 of IC204 to the vertical edge signal generator circuit.

4-4. Automatic Iris Control(AIC) Circuit

Outline

This circuit controls the lens iris opening according to the incoming light intensity. This circuit generates the DC voltage corresponding to the light intensity and sends this DC voltage to the automatic iris control (AIC) lens to drive iris mechanism.

The lens iris is closed when the power is turned OFF for vidicon protection.

Details

The wide BL signal Ⓐ separated from the CP/pre BL/wide BL mixed signal is supplied to the modulator circuit inside IC204 from the CP/pre BL/wide BL separator.

The Y signal Ⓑ whose pedestal level is set is fed from the Y_H low level clip circuit to the modulator circuit, where the Y signal is modulated by the wide BL signal. To drive the lens iris by the signal corresponding to the center image, the Y signal Ⓑ is modulated by the wide BL signal Ⓐ.

The modulated Y signal Ⓒ is peak-rectified in the modulator and converted into DC voltage corresponding to the Y signal level i.e., the incoming light intensity.

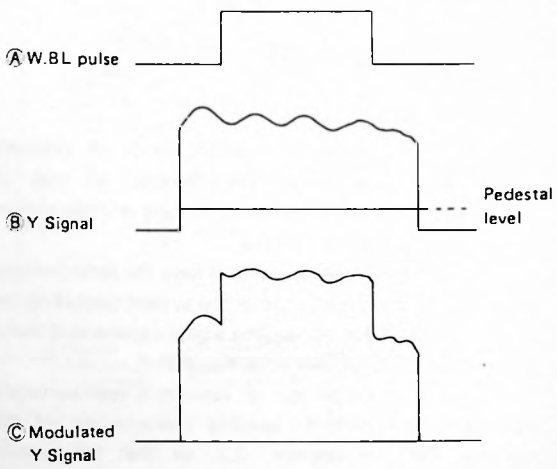


Fig. 4-4-1 Modulation Signal for AIC

This DC voltage is fed to the inverted input of DC amplifier, where it is amplified. The amplified DC voltage is then fed through pin 9 of IC204, R2001 and terminal No. 6 of CN202 to the AIC motor to drive it. If the incoming light intensity goes down, the modulated Y signal level decreased so that the DC voltage which is obtained by rectifying the Y signal also goes down. When an decreasing DC voltage is applied to the inverted input of amplifier, the output from amplifier increases. This output is applied to motor to open the lens iris.

When the incoming light intensity increases, reverse operation takes place.

In this way, the incoming light to the pick-up tube and preamplifier output level are maintained constant.

When the incoming light intensity is extremely low, and the lens iris becomes wide open, the automatic gain control (AGC) circuit in IC205 starts to operate. (Refer to AGC circuit on page 27).

When the light intensity changes and the Iris control motor is operated, the electromotive force appears in the motor damper coil connected between terminal No. 4 and No. 7 of CN202. The DC current from the damper coil is negatively fed back to the inverted input of amplifier inside IC204 through terminal No. 7 of CN202, amplifier IC206 and pin 8 of IC204 to damp the unwanted iris hunting due to changes in light intensity.

The DC voltage set by VR224 (AIC SET) is applied to the inverted input of amplifier IC206 and pin 8 of IC204 for adjusting the amplitude of amplifier inside IC204 and setting the normal iris stop at the standard light intensity.

When the power switch is turned OFF, the regulated +3.3V which is generated in IC204 and supplied to the motor through terminal No. 4 of CN202 falls to zero and the lens iris is closed mechanically.

The regulated +3.3V is fed to other circuits in the Process circuit board as a sub-power source.

The circuit which consists of Q220 and D204 is connected to the non-inverted input of amplifier IC206 is the AIC start delay circuit.

4-5. AIC Start Delay Circuit

Outline

The automatic iris control (AIC) circuit generates the DC voltage corresponding to the Y signal and controls the iris opening of the lens with the DC voltage.

However, it takes some time for the cathode of the vidicon to be heated sufficiently in order to emit electrons at full force after turning ON the power switch. Therefore, the output signal of the vidicon is gradually resolved from its low signal level.

When the power switch is turned ON, the output signal of the vidicon is very low and the iris of AIC lens is wide open. At this time, if the camera is pointed at an extremely bright object, the bright image may "burn" the vidicon target.

Also, after turning ON the power switch, the camera initially produces an unnatural green color since the red(R) and blue(B) modulated components are riding on top of the green signal, and the R and B signals are resolved last.

The AIC start delay circuit generates the DC voltage for closing the lens iris initially after power turn ON.

Details

When the power switch is initially turned ON, +6V is applied to the emitter of Q220 and Q220 is switched ON due to the surge current flowing into C241. When Q220 is switched ON, +6V at its collector is fed to the non-inverted input pin 5 of IC206.

The amplified output from IC206 is supplied to the automatic iris control (AIC) driver inside IC204 through pin 8 to close the lens iris. This state lasts approximately 15 seconds until C241 is fully charged and Q220 is switched OFF. When Q220 is switched OFF, the lens iris is controlled by the DC voltage corresponding to the incoming light intensity.

In this way, the lens iris is closed during the initial period after the power switch is turned ON in order to prevent the vidicon from burning and avoid unnatural green color in the highlights.

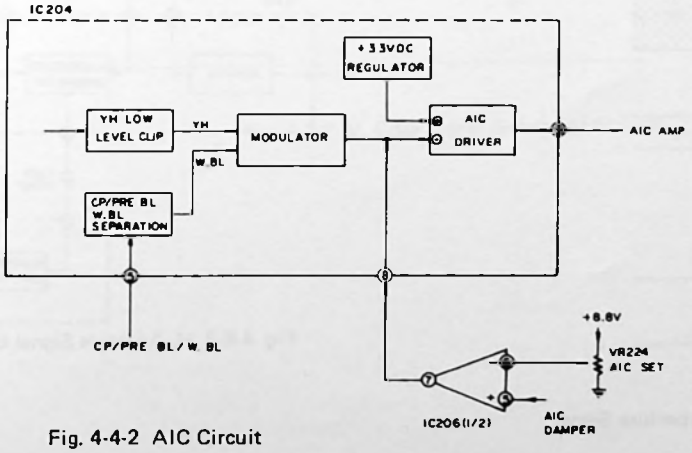


Fig. 4-4-2 AIC Circuit

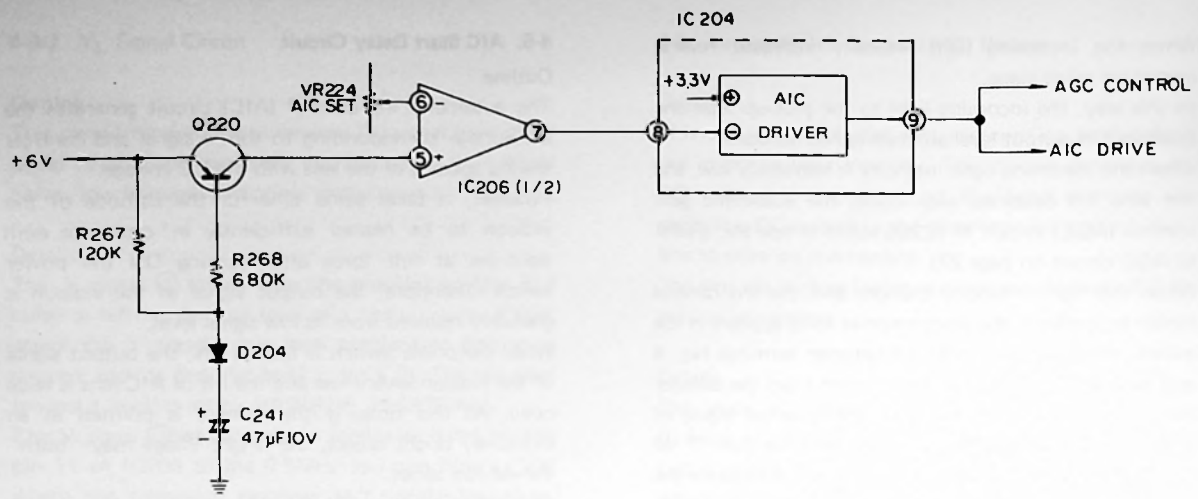


Fig. 4-5 AIC Start Delay Circuit

4-6. Horizontal Aperture Signal Generator Circuit

Outline

This circuit generates the horizontal edge (aperture) signal to enhance the horizontal resolution.

Details

The luminance (Y_H) signal having high frequency response is fed from the Y_H signal circuit inside IC207 to buffer inside IC207 through pin 16.

When the camera is aimed at an object Ⓐ for example, signal Ⓑ passed through pin 18 of IC207, signal Ⓒ delayed 0.2μsec. by delay line LC209 and amplified in the H. aperture generator circuit and signal Ⓓ which results from the delayed Y_H signal being reflected back through LC209 and delayed again (0.4μsec.) appear at the output of the aperture generator where they are mixed in fixed proportions to make up the horizontal (H) aperture signal Ⓔ (Fig. 4-6-1).

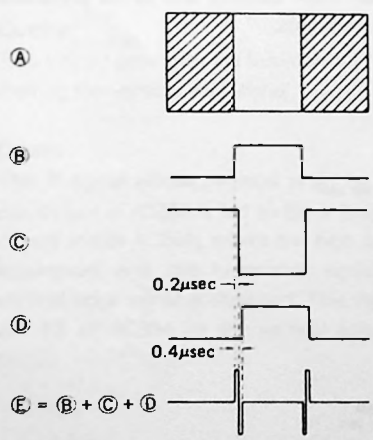


Fig. 4-6-1 Horizontal Aperture Signal

The H. aperture signal obtained in this way is applied through pin 3 of IC207 and pin 7 of IC208 to the H. aperture noise coring/suppress circuit, where the noise mixed in the H. aperture signal Ⓕ is removed Ⓖ.

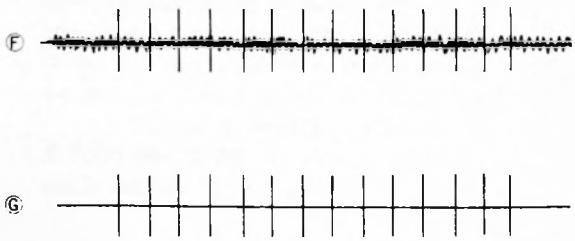


Fig. 4-6-2 H. Aperture Noise Corning

The H. aperture signal which undergoes the noise coring/suppress circuit is then supplied through pin 8 of IC208 to mixing amplifier Q211, where it is mixed with the chrominance signal.

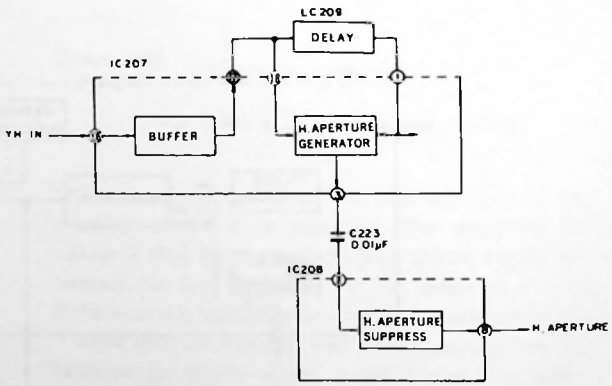


Fig. 4-6-3 H. Aperture Signal Generator Circuit

4-7. Vertical Edge Signal Generator Circuit

Outline

This circuit generates a vertical edge signal for increasing the vertical resolution by enhancing vertical edge contrast.

Details

The luminance [Y(edge)] signal for making the vertical (V) edge signal supplied from the Y(edge) signal circuit through pin 13 of IC204 is fed to pin 1 of IC201 through VR201 (V. EDGE BALANCE). This Y(edge) signal modulates the subcarrier signal which is applied from the pulse generator circuit to pin 3 of IC201.

The modulated signal from pin 7 of IC201 is sent to the glass delay line DL201(1/2) which delays the input signal by 1H line.

The 1H-delayed modulated signal is detected by the full-wave detector circuit consisting of T201, Q201 and Q202. The delayed Y(edge) signal Ⓑ from the emitters of Q201 and Q202 is fed to the base of Q203, where it is mixed with the undelayed Y(edge) signal Ⓐ applied to the emitter of Q203 to form a vertical edge signal Ⓒ at the collector.

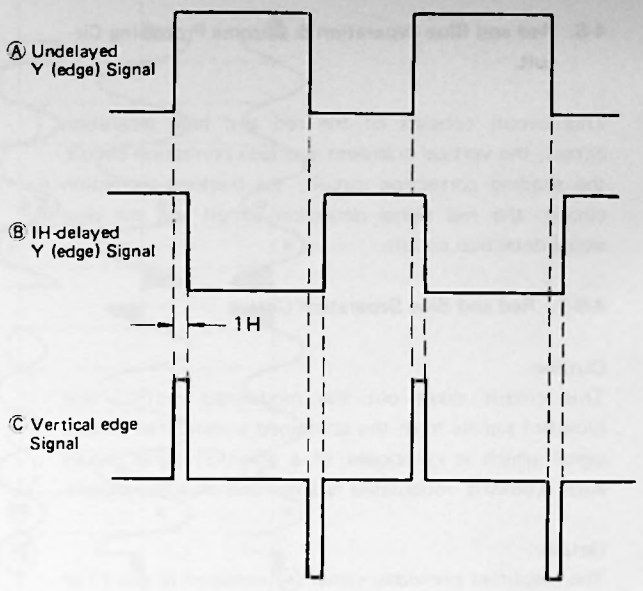


Fig. 4-7-1 Vertical Edge Signal

The vertical edge signal is sent to the low pass filter LC201 where the 3.58MHz and its harmonics are removed. The vertical edge signal from the low pass filter is sent via the output amplifier, consisting of Q206–Q209, to the vertical transient spurious correction circuit inside IC203, and to the Y_H signal circuit where it is mixed with the Y_H signal.

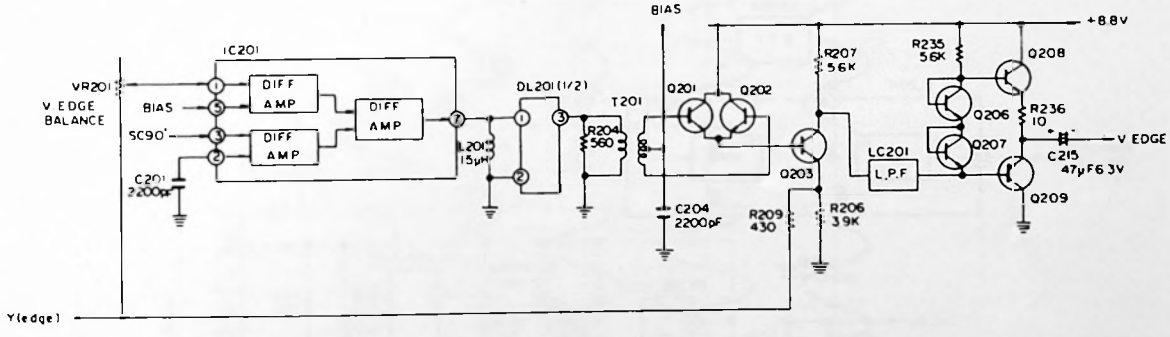


Fig. 4-7-2 V. Edge Signal Generator Circuit

4-8. Red and Blue Separation & Chroma Processing Circuit.

This circuit consists of the red and blue separation circuit, the vertical transient spurious correction circuit, the shading correction circuit, the tracking correction circuit, the red signal detection circuit and the blue signal detection circuit.

4-8-1. Red and Blue Separation Circuit

Outline

This circuit takes out the modulated red(Rc) and blue(Bc) signals from the combined preamplifier output signal which is composed of a green(G) signal mixed with 3.58MHz modulated red(Rc) and blue(Bc) signals.

Details

The amplified pre-video signal Ⓐ obtained at pin 17 of IC204 is fed to 3.58MHz band pass filter (BPF) LC204 where the Rc/Bc signal Ⓑ is detected.

The detected Rc/Bc signal is then supplied to the 90° phase shifter Q215 through VR216 (Rc/Bc GAIN), the Rc/Bc amplifier inside IC204, C231 and VR223 (Rc/Bc SEPARATION-2). The 90° phase-shifted Rc/Bc signal Ⓒ obtained at the junction point of VC201 (Rc/Bc SEPARATION-1) and R295 is then applied to the Rc/Bc separation circuit inside IC203 through pin 18. VC201 is a control for shifting the phase of Rc/Bc signal by 90°.

The Rc/Bc signal Ⓑ at pin 3 of IC204 is also supplied to 1/2H delay line DL202(1/2) where it is delayed a half horizontal line (31.75μsec). The 1/2H-delayed signal is then fed to another 1/2H delay line DL202(1/2) through amplifier Q227. (Q227 is used for matching the impedance between two 1/2H delay lines.)

The inverted 1H-delayed Rc/Bc signal Ⓓ obtained at the junction point of C271 and R291 is supplied to the vertical transient spurious correction circuit inside IC203 via pin 17. (The vertical transient spurious correction will be described later.) The Rc/Bc signal undergoes the vertical transient spurious correcton is supplied to the Rc/Bc separation circuit.

In the Rc/Bc separation circuit, the 90° phase-shifted Rc/Bc signal Ⓒ and the inverted 1H-delayed Rc/Bc signal Ⓓ are added forming the Rc signal Ⓔ, and the Rc/Bc signal Ⓒ and the Rc/Bc signal Ⓓ are subtracted each other forming the Bc signal Ⓕ.

The Rc and Bc signals are fed to the respective shading/tracking correction circuits.

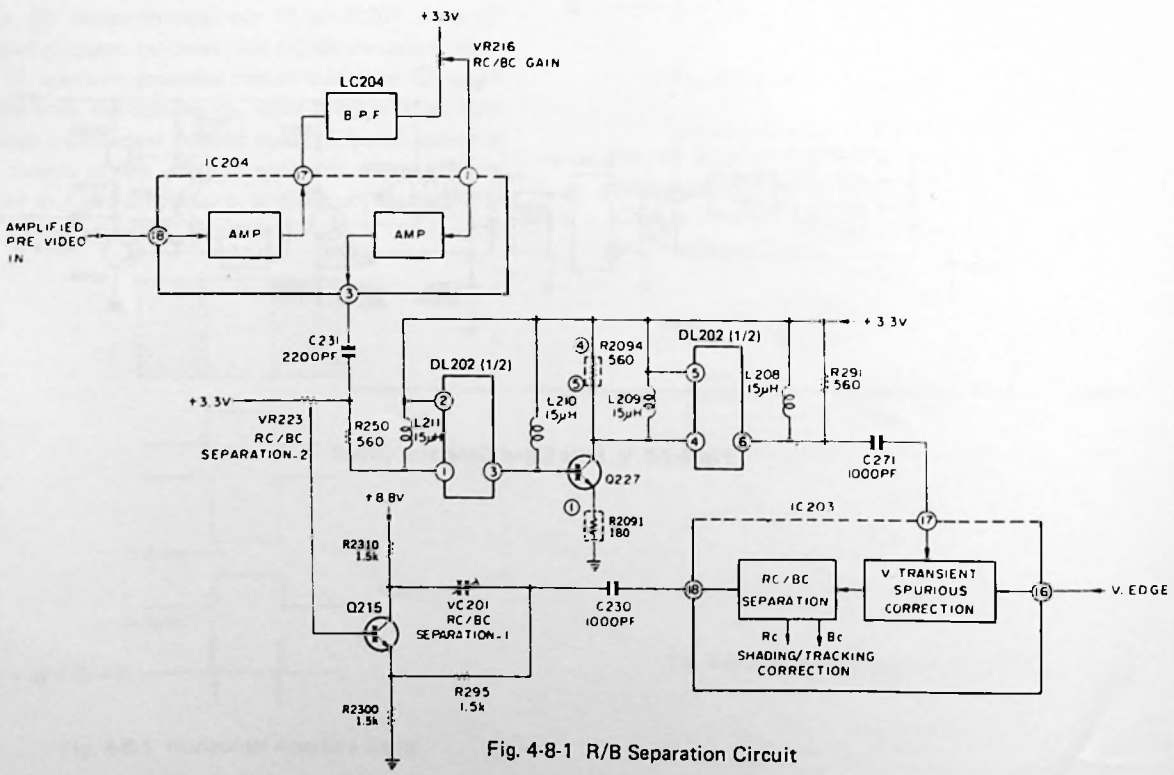


Fig. 4-8-1 R/B Separation Circuit

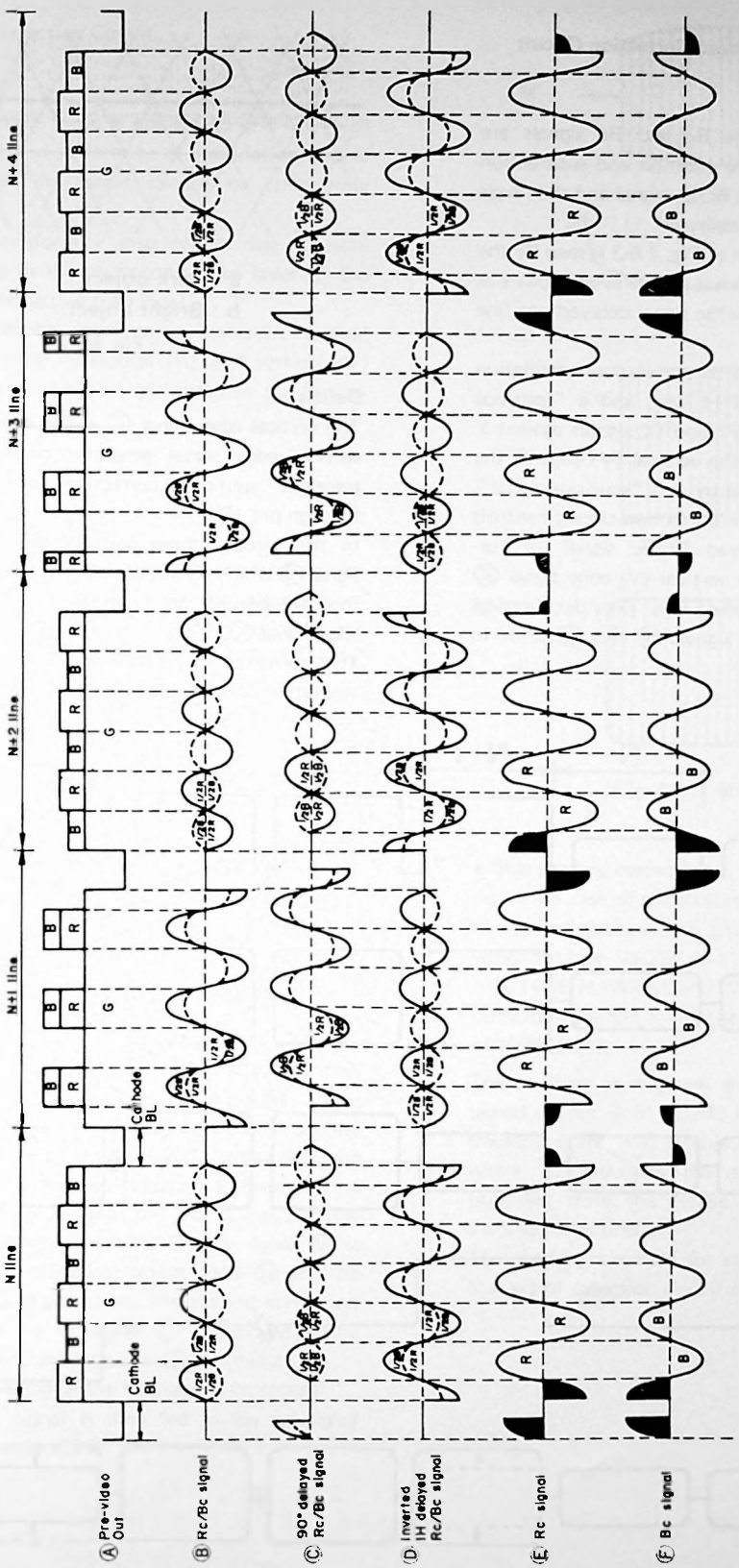


Fig. 4-8-2 Rc/Bc Signal Separation

4-8-2. Vertical Transient Spurious Correction Circuit

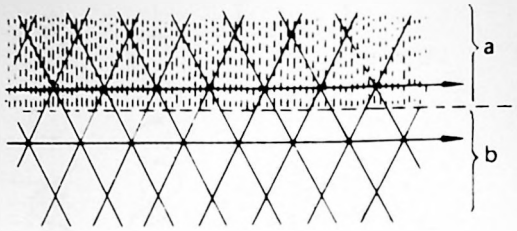
Outline

As described previously, the Rc and Bc signals are separated from each other by addition and subtraction of the one line (1H) delayed Rc/Bc signal and the phase shifted Rc/Bc signals but not delayed.

When a pattern such as shown in Fig. 4-8-3 is seen by the camera, the Rc/Bc signal which is not delayed appears as in Ⓘ in Fig. 4-8-4, and the Rc/Bc signal delayed one line (1H) becomes as in Ⓙ.

Therefore, it is impossible to secure vertical correlation between Rc/Bc signals of N+1 line, and a "spurious signal" differing in level of Rc and Bc signals against Y signal Ⓗ is generated, and the vertical (V) edge of the object is unnaturally colored by this "spurious signal".

The vertical transient spurious correction circuit controls the amplitude of 1H-delayed Rc/Bc signal Ⓙ corresponding to N+1 line with vertical (V) edge signal Ⓚ and the signal Ⓛ is made. This provides vertical correlation between Rc/Bc signals Ⓘ and Ⓛ prior to color separation.



a : Dark object
b : Bright object

Fig. 4-8-3

Details

The vertical edge signal Ⓚ in Fig. 4-8-4 is sent from the vertical edge signal generator circuit to the vertical transient spurious correction circuit inside IC203 through pin 16.

In this circuit, those parts of the 1H-delayed Rc/Bc signal Ⓙ which do not correlate with the Rc/Bc signal Ⓘ (not 1H-delayed) are controlled in level by the vertical edge signal Ⓚ.

The corrected Rc/Bc signal Ⓛ is fed to the Rc/Bc separation circuit inside IC203.

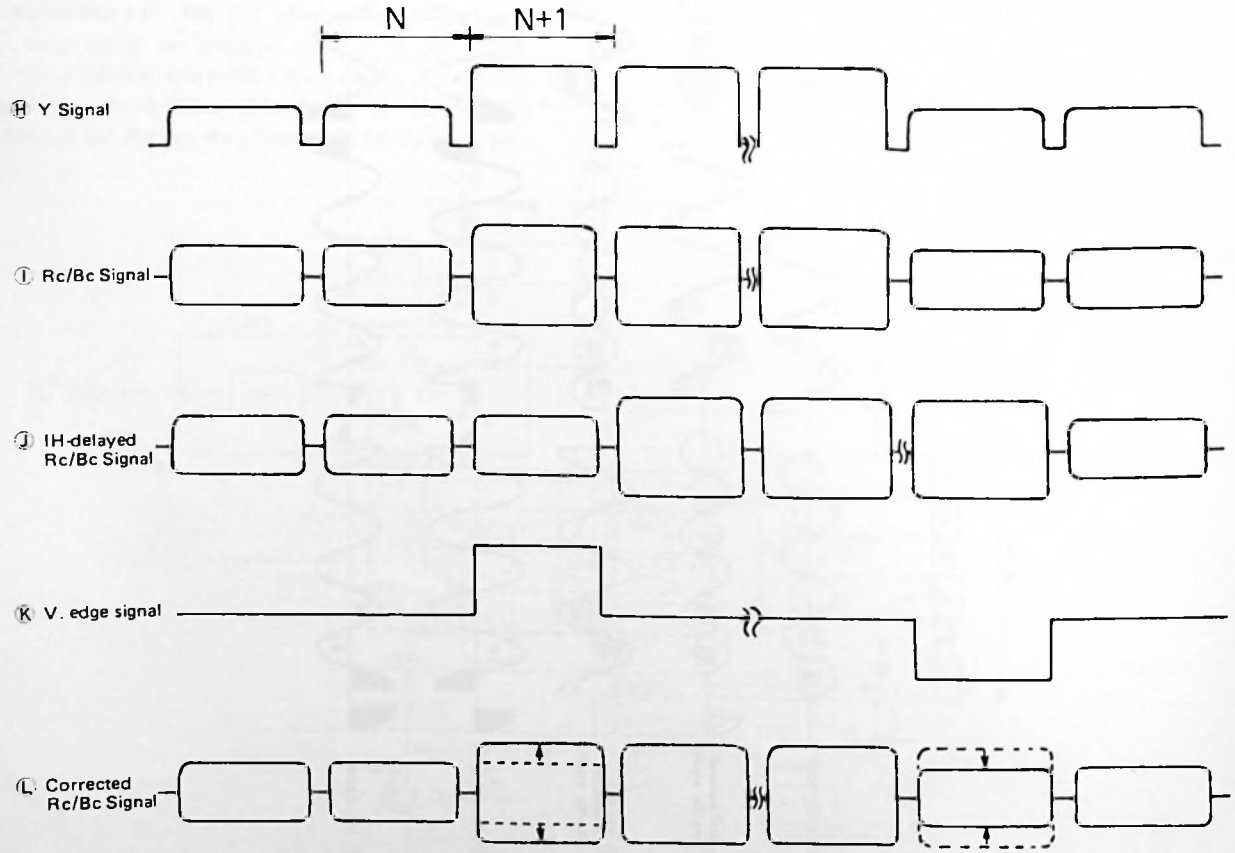


Fig. 4-8-4 Vertical Transient Spurious Correction

4-8-3. Shading Correction Circuit

Outline

Even when dynamic focus is applied to grid-4(G4) of pick-up tube, the non-uniformity of modulation due to uneven focus on the target cannot be completely eliminated.

Modulation non-uniformity also occurs due to non-uniform structure in the photoconductive layer of the pick-up tube (manufacture tolerance).

The shading correction circuit compensates for residual picture shading using horizontal (H) and vertical (V) sawtooth and parabola signals generated in the Deflection circuit board.

Details

- Red shading correction

The vertical parabola and sawtooth, and horizontal parabola and sawtooth signals which are applied from the Deflection circuit board are supplied to the wiper arms of VR209 (R-V.SAW), VR211 (R-V.PARA), VR215 (R-H.PARA) and VR213 (R-H.SAW).

These signals are fed to both the inverted (pin 2) and non-inverted input (pin 3) of amplifier IC202(1/2), where they are mixed and amplified. The output of IC202 at pin 1 produces a positive or negative shading correction signal depending on the position of these controls.

The shading correction signal adjusted by VR209, VR211, VR213 and VR215 is forwarded to the shading/tracking correction circuit inside IC203 through pin 3, where it modulates the modulated red (Rc) signal for correcting the signal shading.

Suppose a uniformly illuminated white object is seen by the camera and the Rc signal has a shading (unevenness of amplitude) such as that shown in Fig. 4-8-5 Ⓜ. This is sent to the shading/tracking correction circuit from the Rc/Bc separation circuit inside IC203. In this case, the four red shading controls are adjusted to generate the shading correction signal Ⓝ at pin 1 of IC202, and it is applied to the correction circuit. The Rc signal Ⓜ is modulated by the shading correction signal Ⓝ and the corrected signal Ⓞ is produced. The shading correction signal mixed with the Rc signal Ⓞ is removed in the correction circuit and the Rc signal Ⓟ is obtained.

In this way, the shading of the Rc signal is corrected.

The corrected Rc signal is then fed to the red signal detection circuit inside IC203.

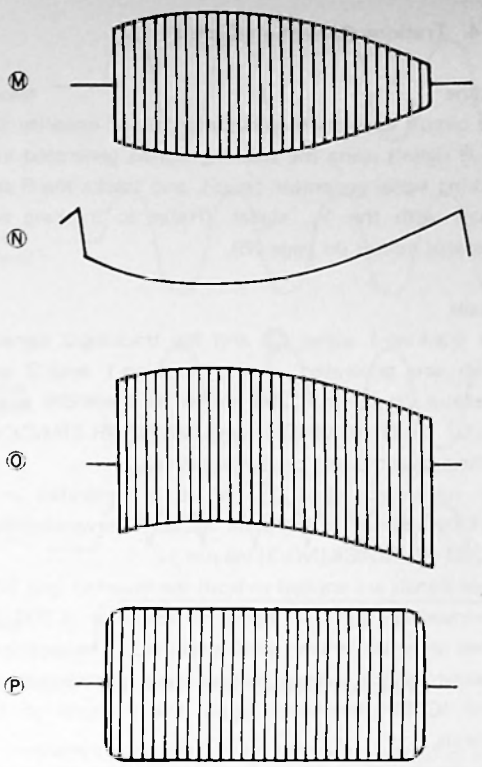


Fig. 4-8-5 Shading Correction

- Blue shading correction

As in the case of red shading correction, the vertical and horizontal parabola and sawtooth signals supplied to the wiper arms of VR208 (B-V.SAW), VR210 (B-V.PARA), VR214 (B-H.PARA) and VR212 (B-H.SAW) are fed to both the inverted (pin 6) and non-inverted (pin 5) input of IC202(1/2).

The positive or negative shading correction signal obtained at pin 7 of IC202 is fed to the blue shading/tracking correction circuit through pin 15 of IC203, where it modulates the modulated blue (Bc) signal (supplied from the Rc/Bc separation circuit) for the shading correction.

The shading-corrected Bc signal is then applied to the blue signal detection circuit inside IC203.

4-8-4. Tracking Correction Circuit

Outline

This circuit corrects the characteristic of linearity for R and B signals using the tracking signals generated in the tracking signal generator circuit, and tracks the R and B signals with the Y_L signal. (Refer to tracking signal generator circuit on page 28).

Details

The tracking-1 signal Ⓠ and the tracking-2 signal Ⓡ which are generated in the tracking-1 and 2 signal generator circuit in IC205 are fed to the wiper arms of VR207 (R.TRACKING-1) and VR205 (R.TRACKING-2) through pin 9 and pin 8 respectively.

The tracking-3 signal Ⓢ which is generated in the tracking-3 signal generator in IC205 is forwarded to the VR203 (R.TRACKING-3) via pin 11.

These signals are applied to both the inverted (pin 2) and non-inverted (pin 3) input of amplifier IC202(1/2), where they are mixed and amplified. The positive or negative red tracking correction signal is produced at pin 1 of IC202 depending upon the position of these controls.

The correction signal is then fed to the red shading/tracking correction circuit through pin 3 of IC203, where it modulates the Rc signal Ⓣ comes from the Rc/Bc separation circuit for correcting the linearity of Rc signal Ⓤ. In this way, the R signal matches the Y_L signal.

VR207 corrects the relatively low level of R signal, VR205 for the relatively high level, and VR203 for the highest level (Fig. 4-8-7).

The tracking correction for the B signal is similarly done with VR206 (B.TRACKING-1), VR204 (B.TRACKING-2), VR202 (B.TRACKING-3), IC202(1/2) and the blue tracking correction circuit inside IC203.

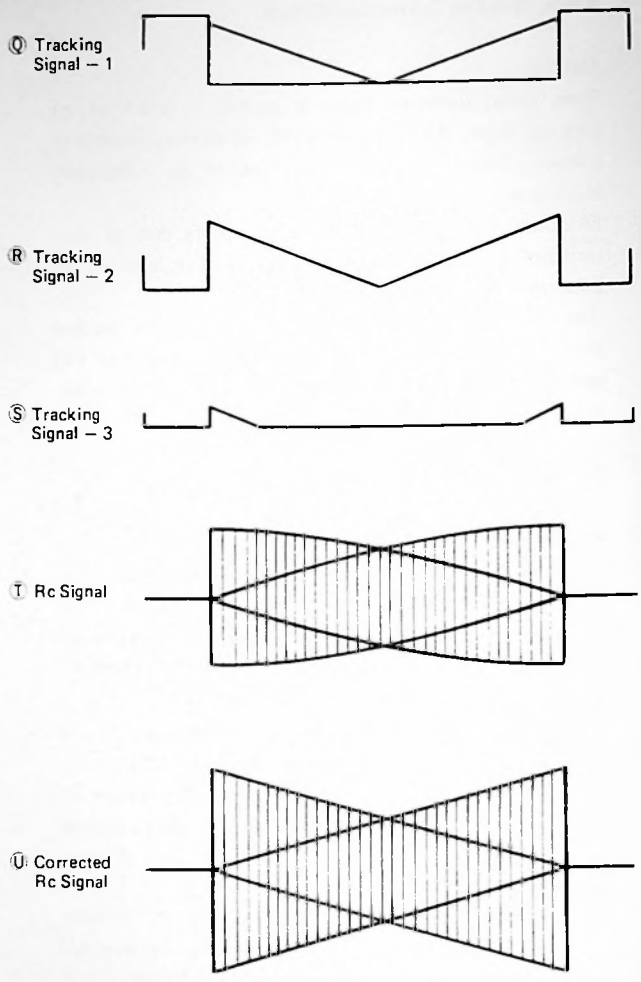


Fig. 4-8-6 Tracking Correction-1

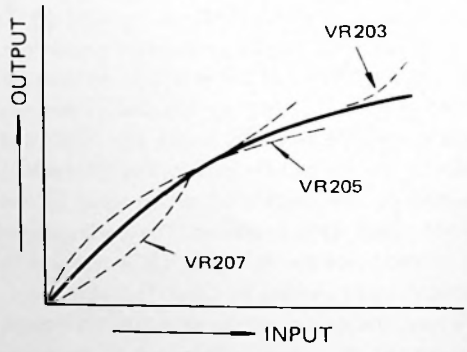


Fig. 4-8-7 Tracking Correction-2

4-8-5. Red Signal Detection Circuit

Outline

This circuit receives the modulated red(Rc) signal from the red shading/tracking correction circuit, removes the modulation and detects the red video signal.
The red video signal is then supplied to the chrominance encoding circuit.

Details

The Rc signal Ⓥ from the red shading/tracking correction circuit is fed through the gain control circuit to the amplifier where it is amplified. The amplified positive Rc signal Ⓦ and negative Rc signal Ⓧ obtained at the output of amplifier are forwarded to the detector.
The detected Rc signal Ⓨ is then fed to the low pass filter (LPF) LC210. The detector which extracts the red signal produces a unwanted 7.16MHz ripple signal Ⓨ. The 7.16MHz component is removed by the LPF leaving only the red signal Ⓩ.
The resultant red signal is fed to the chrominance encoding circuit through buffer Q213.
VR001 (COLOR ADJUSTMENT) which is located on the side of the camera is a control for fine adjustment of the color balance. VR228 (R. GAIN) is a red signal level presetting control.
VR222 (R. PEDESTAL) is a control for setting the red pedestal.

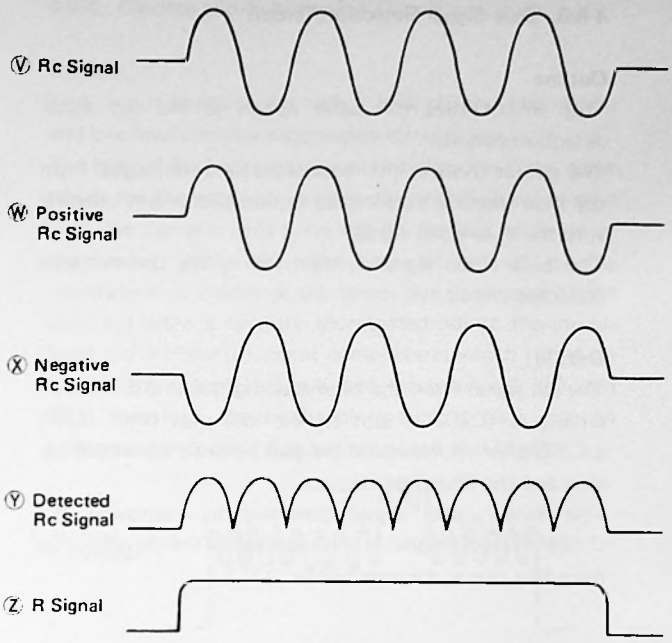


Fig. 4-8-8 Red Signal Detection

The preblanking (pre BL) pulse fed to the amplifier from the pulse generator circuit removes the noise during the blanking period.

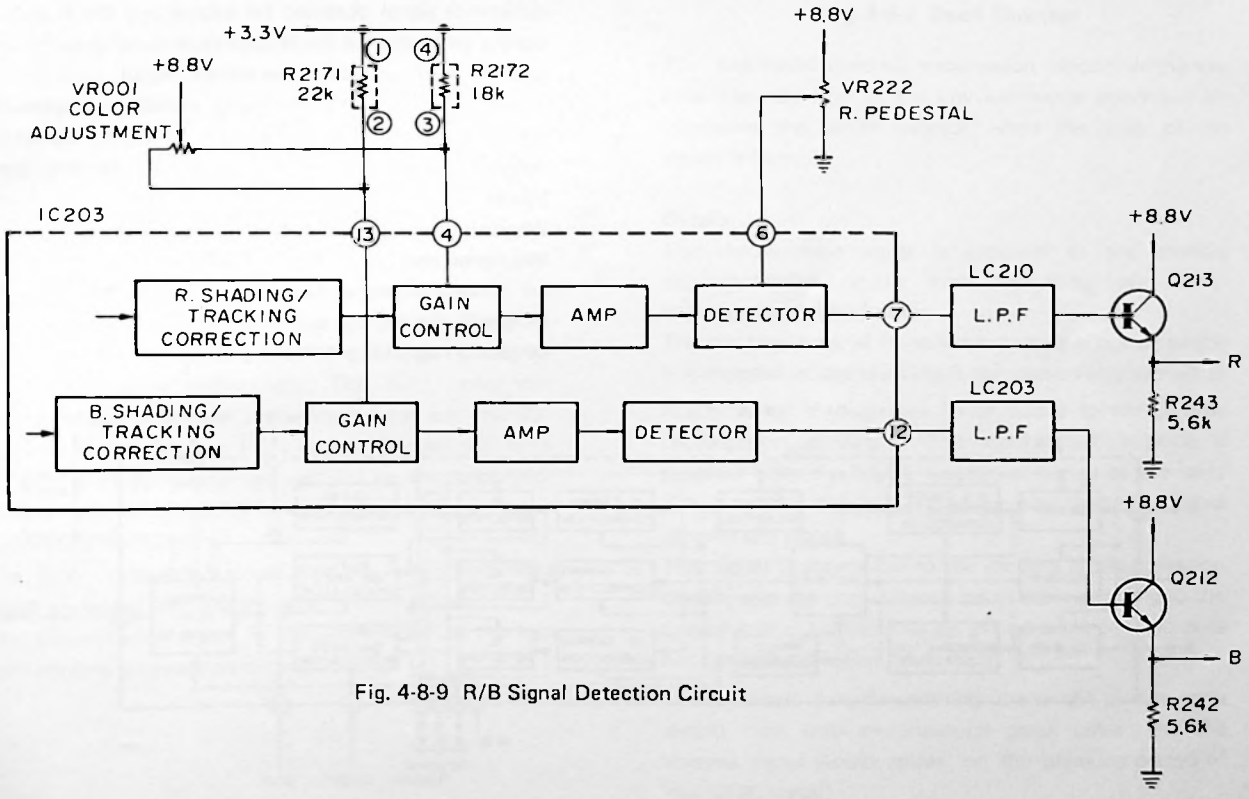


Fig. 4-8-9 R/B Signal Detection Circuit

4-8-6. Blue Signal Detection Circuit

Outline

This circuit uses the same design as the red signal detection circuit.

The circuit receives the modulated blue (Bc) signal from the blue shading/tracking correction circuit and converts it to the blue video signal.

The blue video signal is then fed to the chrominance encoding circuit.

Details

The Bc signal from the blue shading/tracking correction circuit in IC203 is sent to the low pass filter (LPF) LC203 after it undergoes the gain control, the amplification and the detection circuits.

The blue video signal obtained by removing the 7.16MHz ripple signal is then applied to the chrominance encoding circuit through buffer Q212.

4-9. Chrominance Encoding Circuit

This circuit contains the color reproduction correction circuit, the gamma correction circuit, the chrominance signal generator circuit and the chroma clip/suppression circuit.

4-9-1. Color Reproduction Correction Circuit

Outline

This circuit receives the luminance (Y_L) signal having low frequency response characteristic, the red signal and the blue signal, and corrects colorimetry imperfection (particularly red and green) resulting from the spectral characteristic of the stripe filter which affects mostly the red and green signals.

Details

The red(R), blue(B) and Y_L signals obtained at the emitter of buffer Q213, Q212 and Q214 respectively are applied to clamp circuit inside IC208 through pin 3, pin 4 and pin 2. In the clamp circuit, the blanking level of these signals are clamped by the horizontal scanning start (Hs) pulse applied from the Hs/BL separation circuit inside IC208 respectively.

The clamped R, B and Y_L signals are forwarded to the matrix circuit. The R and Y_L signals are also applied to the R.color reproduction correction circuit and they are subtracted each other.

The R-Y_L color difference signal made by the subtraction is supplied to the matrix circuit. The B-Y_L color difference signal obtained by subtracting the B and Y_L signals each other in the B.color reproduction correction circuit is also supplied to the matrix circuit.

The R, B, Y_L, R-Y_L and B-Y_L signals undergoes the matrix to generate the corrected R, B and Y_L signals for correcting the color reproduction of red and green image.

When the camera is pointed at a black and white object, the signal level of R, B and Y_L is the same. Therefore, no correction signal is applied to the matrix circuit. However, the camera is pointed at a colored object, the correction signal is generated.

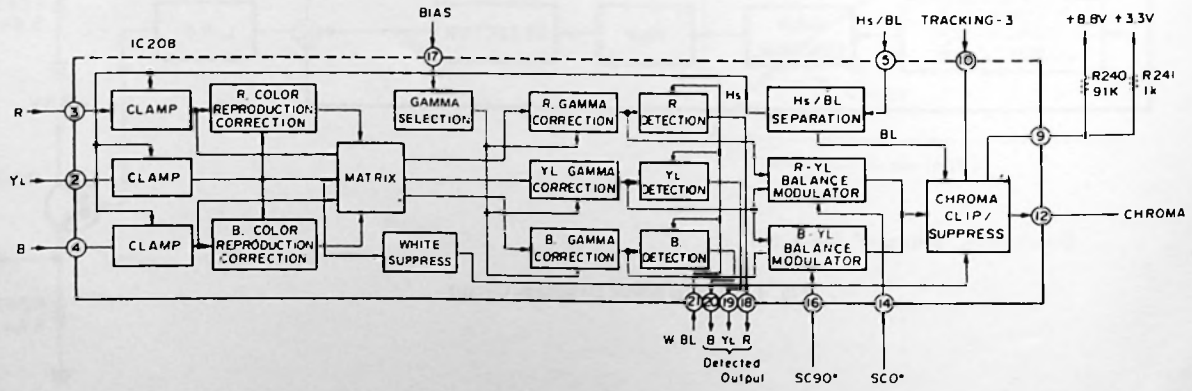


Fig. 4-9-1 Chrominance Encoding Circuit

4-9-2. Gamma Correction Circuit

Outline

This circuit receives the red(R), blue(B), and Y_L signals from the color reproduction correction circuit.

These signals undergoes the gamma correction and goes to the chrominance signal generator circuit.

Details

The R, B and Y_L signals from the matrix circuit are supplied to the gamma(γ) correction circuits respectively and undergoes the gamma correction. (Refer to the gamma correction circuit on page 32.) The suppression level and the extent of suppression are set by the gamma(γ) select circuit which is controlled by the DC voltage at pin 17 of IC208.

The gamma-corrected R, B and Y_L signals are forwarded to the chrominance signal generator circuit.

4-9-3. Chrominance Signal Generator Circuit

Outline

This circuit matrixes the red(R), blue(B) and Y_L signals to generates the R-Y_L and B-Y_L color difference signals, and modulates these base band color difference signals on two subcarrier differing in phase by 90° to generate a chrominance signal.

Details

The R signal from the R gamma correction circuit is fed to the R-Y_L balance modulator circuit. The Y_L signal from the Y_L gamma correction circuit is also supplied to the R-Y_L balance modulator circuit where the R-Y_L color difference signal is made up inside the modulator. The R-Y_L signal modulates the 0° phase subcarrier (SC 0°) applied to the modulator from the sync generator IC211 through pin 14 of IC208. The modulator produces an AM modulated (suppressed carrier) signal.

Similarly, the B signal and Y_L signal from the B and Y_L gamma correction circuits are fed to the B-Y_L balance modulator circuit respectively. The B-Y_L color difference signal made up in the modulator and the 90° phase shifted subcarrier (its phase is delayed 90° with respect to R-Y_L subcarrier) applied to the modulator through pin 16 of IC208 undergoes suppressed carrier quadrature modulation.

The R-Y_L modulated signal and the B-Y_L modulated signal are added forming the chrominance signal.

The chrominance signal is then forwarded to the low level chroma suppression circuit.

4-9-4. Chroma clip/Suppression Circuit

Outline

This circuit contains the high Y level chroma clip circuit and low level chroma suppression circuit.

The high Y level chroma clip circuit clips the green color which results when an excessively bright object is shot with the camera. This is caused by the lack of beam in the pick-up tube. When the beam of pick-up tube is insufficient to discharge the target due to excessive light reflected from a brightly illuminated object, the modulated red(R)/blue(B) signal components which riding on top of the green(G) signal become satulated (Ⓐ and Ⓑ). Therefore, the bright picture parts turn into an unnatural green color due to lack of red and blue.

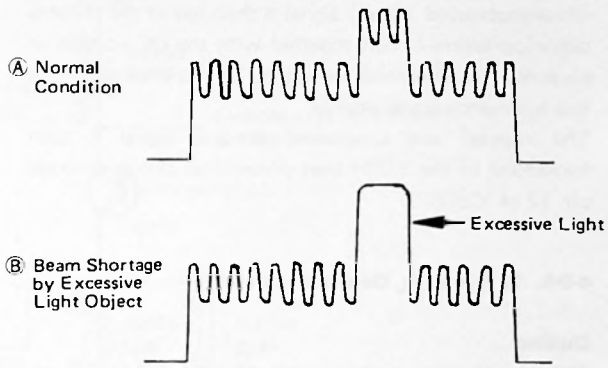


Fig. 4-9-2 Beam Shortage

The low level chroma suppression circuit enchances color reproduction in the low luminance condition by improving the white balance, when the color of the object is faint.

Details

The chrominance signal is supplied to the chroma clip/suppression circuit from the R-Y_L and B-Y_L balance modulator circuits.

The tracking-3 signal (high luminance level signal) which is generated in the tracking-3 signal generator circuit in IC205 is fed through pin 10 of IC208 to the chroma clip/suppression circuit. The blanking (BL) pulse is supplied from the Hs/BL separation circuit to the same circuit, where they are mixed forming the high Y level chroma clip signal.

This signal is forwarded to the chroma clip/suppression circuit, and the chrominance signal corresponding to the excessive bright object and BL period is clipped and does not reach the NTSC output.

If this circuit is malfunctioning, the bright picture parts would turn into an unnatural green color, and the chroma signal would appear on the blanking period of the NTSC signal.

The DC voltage, obtained by dividing the voltage between +8.8V and +3.3V with R240 and R241 and fed to the chroma clip/suppression circuit via pin 9, determines the suppression level of chroma signal.
This DC Voltage is applied to the chroma clip/suppression circuit and clips the low chrominance level.

Fig. 4-9-3 Low Level Chroma Suppression

The Y_L signal from the Y_L clamp circuit inside IC208 is applied to the Y(sup) white suppression circuit. The white-suppressed Y(sup) signal is then fed to the chroma clip/suppression circuit together with the DC voltage to suppress the chrominance signal corresponding to the low luminance signal mainly.
The clipped and suppressed chroma signal is then forwarded to the 1/2fH beat prevention circuit through pin 12 of IC208.

4-9-5. R, B and Y_L Detection Circuit

Outline
This circuit receives the red(R), blue(B) and Y_L signals from the gamma correction circuit and converts them to the DC voltages.
The detected DC voltages are sent to the white balance setting circuit.

Details
The R, B and Y_L signals from the gamma correction circuits are respectively fed to the detection circuits and their center portions are detected by the wide blanking (W. BL) pulse supplied through pin 21 of IC208 in order to set the white balance with the signal corresponding to the center image.
The R, B and Y_L detected signals are converted to the DC voltage in the detection circuit and fed to the white balance setting circuit through pins 18, 20 and 19 of IC208.

4-10. 1/2 fH Beat Prevention Circuit

Outline
In this color camera, the red(R) and blue(B) signals are obtained from the modulated R and B signals of odd-number scanning lines and the modulated R and B signals of even-number scanning lines either by adding or subtracting them.
It should also be noted that the levels of the R and B signals on odd-numbered and even-numbered scanning lines are not equal due to the non-linear vertical scanning and decoding process necessary for separation. (Fig. 4-10-1 Ⓐ and Ⓑ)
Therefore, the chroma signal level obtained after NTSC modulation of R-Y_L and B-Y_L signals differs between the even-numbered lines and the odd-numbered lines, causing a level difference Ⓒ.

Thus, this level difference appears on the monitor as an 1/2fH beat. (i.e. seen as line pairing of chroma)
To remove this beat, the chroma signal level of each horizontal line is averaged by adding a 1H delayed chroma signal Ⓓ and an un-delayed chroma signal Ⓒ to make a chroma signal Ⓔ without beat or differences.

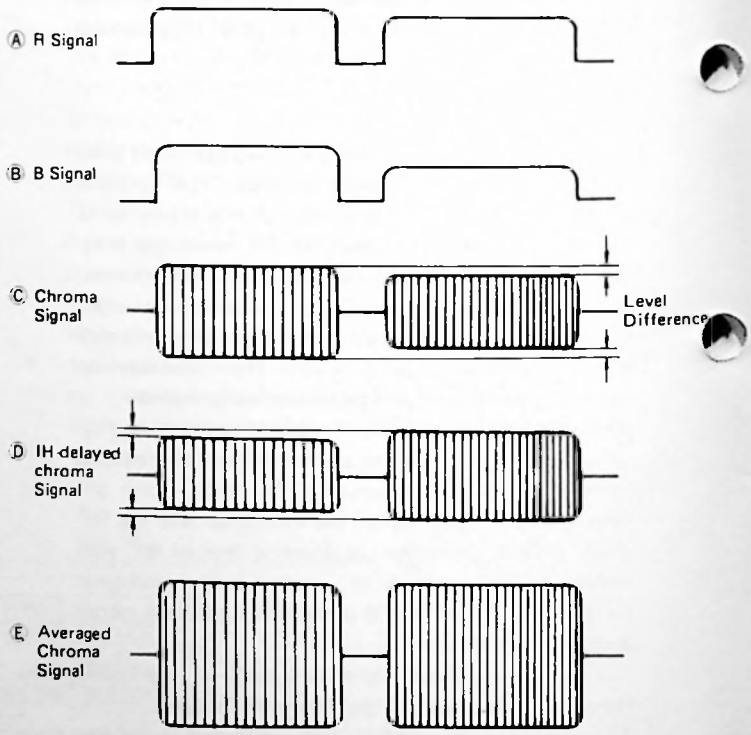


Fig. 4-10-1 1/2 fH Beat Prevertion

Details

The chroma signal Ⓒ from pin 12 of IC208 is supplied to 1H delay line DL201(1/2) through C221, R2164 in BR216 and L203. The 1H-delayed chroma signal Ⓓ runs through R2162 in BR216, and is mixed with the un-delayed chroma signal Ⓒ which is fed through R2163 in BR216.

After its level is set by VR221 (CHROMA GAIN), the mixed chroma signal Ⓔ is multiplexed with the horizontal (H) aperture signal comes from pin 8 of IC208 through C222 and R2153 in BR215.

The mixed signal is applied to the NTSC signal processing circuit through amplifier Q211.

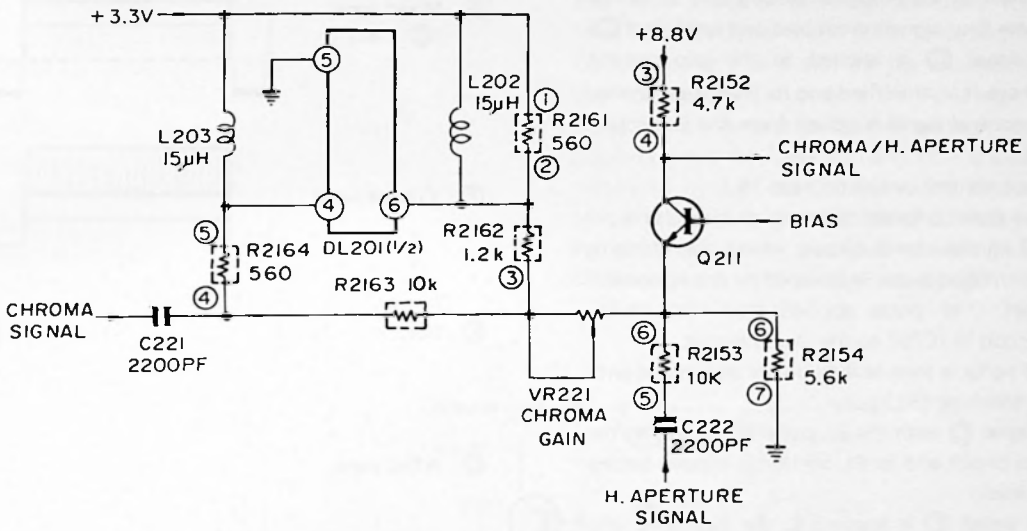


Fig. 4-10-2 1/2 fH Beat Prevention Circuit

4-11. White Balance Set Circuit

This circuit and the circuit in the White set circuit board set the white balance of the picture automatically. Refer to 5. White Set Circuit Board on page 49 for circuit description.

4-12. NTSC Signal Processing Circuit

Outline

In this circuit, the chrominance signal, the luminance signal, the burst signal and the sync signal are mixed to produce a composite NTSC signal. The NTSC signal is applied to the portable VCR, or a table model type VCR through the power supply.

Details

The mixed signal Ⓐ of the luminance (Y_H) signal and the vertical (V) edge signal is fed to amplifier inside IC207 through pin 1. The mixed signal Ⓑ of the chrominance signal and the horizontal (H) aperture signal is supplied to the amplifier through pin 2. In the amplifier, these four signals are mixed and amplified(Ⓒ). The mixed signal Ⓒ is applied to the gain control amplifier, where it is amplified and its level is controlled by the fade control signal supplied from the Deflection circuit board.

(Refer to Fade control circuit on page 14.)

The amplified signal is forwarded through pin 13 and pin 12 of IC207 to the clamp circuit, where the blanking level of the amplified signal is clamped by the horizontal scanning start (Hs) pulse applied from the Hs/BL separation circuit in IC207 to the clamp circuit.

The clamped signal is then sent to buffer and mixed with the positive blanking (BL) pulse.

The mixed signal Ⓓ with the BL pulse is supplied to the low level clip circuit and its BL portion is clipped setting the pedestal level.

The clipped signal Ⓔ is applied to the high level clip circuit where the signal exceeds 125IRE unit (0.9V) is clipped.

The mixed signal of chrominance and luminance signal is mixed with the mixing signal Ⓕ of sync pulse and burst signal forming a composite NTSC signal Ⓖ.

The NTSC signal at pin 9 of IC207 is supplied to the VCR through C239 and R264.

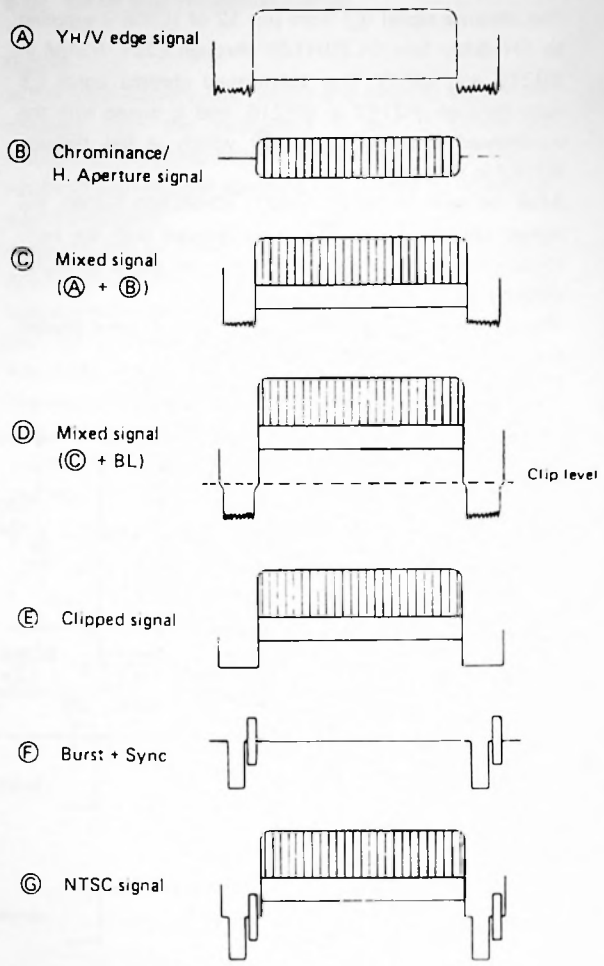


Fig. 4-12-1 NTSC Signal

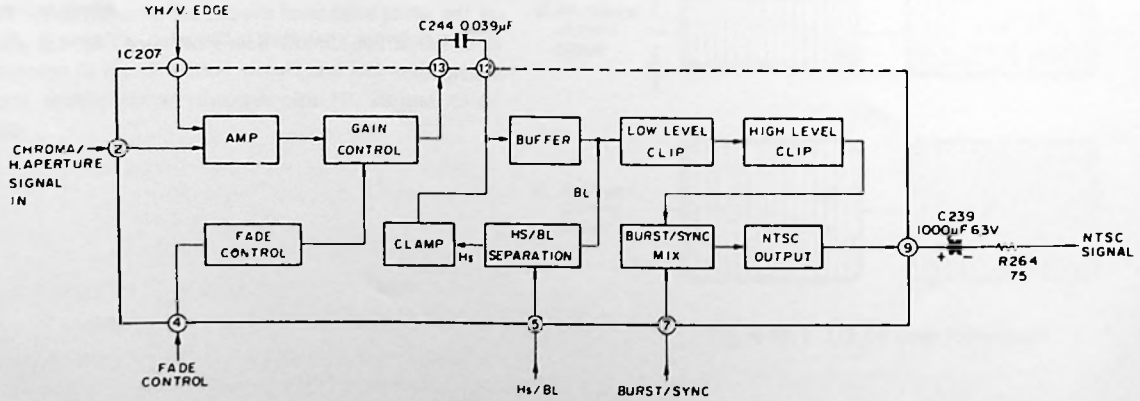


Fig. 4-12-2 NTSC Signal Processing Circuit

4-13. Playback Sense Circuit

Outline

This circuit senses the recording or playback mode of the portable VCR.

When the portable VCR is set into the recording mode, this circuit sets the camera to supply the NTSC output signal to the viewfinder, and the portable VCR for recording.

When the portable VCR is set into the playback mode, this circuit shuts off the camera function and supplies the playback signal from VCR to the viewfinder.

Details

When the portable VCR is set into the recording mode, no DC bias is applied to the base of Q216 and Q216 remains OFF, and 6.2V zener diode D203 connected between +9V and ground through R2131 and R2135 in BR213 turns ON to switch Q218 ON. Therefore, +8.8V at the collector of Q218 is supplied to the Process circuit board. At the same time, the NTSC output signal at pin 9 of IC207 is fed to the viewfinder through the Deflection circuit board, and the portable VCR for recording.

When the portable VCR is set into the playback mode, the playback signal which rides on top of +6V DC is supplied from the VCR to the base of Q216. Q216 is turned on by the +6V and the potential of its emitter and D203 anode become approximately +5.3V. Therefore, the 6.2V zener diode D203 is turned OFF causing Q218 to be OFF and shut off the Process circuit board and Preamplifier circuit board. In this way, the NTSC signal is not generated in the camera and only the playback signal from the portable VCR is supplied to the viewfinder through the Deflection circuit board.

In the playback mode, Q217 and Q219 are turned ON and pin 8 of IC207 is grounded for setting the output of NTSC output at pin 9 to high impedance.

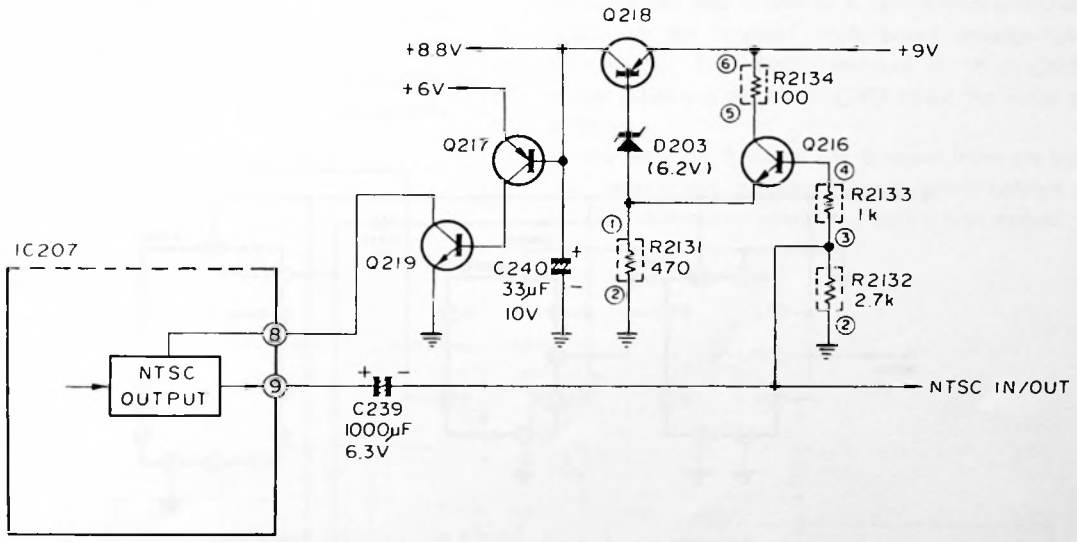


Fig. 4-13 Playback Sense Circuit

5. White Set Circuit Board (YWCC007ZK04)

The White Set Circuit Board (YWCC007ZK04) contains following circuits.

This circuit in conjunction with the white setting circuitry in the Process circuit board set the white balance of picture automatically. (Proper white balance or color balance means the camera will reproduce a white object in the picture as white.)

This section also explains the portion of the circuit on the Process circuit board.

Since the scene illumination contributes to color in balance, a diffusion filter is placed between the lens and the pick-up tube when the White Balance Switch is placed in the SET position.

Therefore white balance uses the same light as will be used later. When the SET position is chosen, the gain of the RED(R) and BLUE(B) signals prior to the chrominance encoding circuit is reduced to 0 (zero) level, which results in a greenish raster.

The automatic cycle in the camera increases R and B signals in steps and stops when each of these levels is equal to the green (Y_L) level. At this point, the R-Y_L and B-Y_L signals are both 0 (zero), the picture is white, and white balance has been achieved.

This is indicated by the INDOOR indicator in the viewfinder since it is also used as a White Balance indicator. It will flash after the power switch is turned ON and while the R and B signals are increasing, and it stops flashing when the auto white balance process is finished.

This circuit contains the clock pulse generator circuit, white balance preset circuit, automatic white balance setting circuit and white balance indicator circuit.

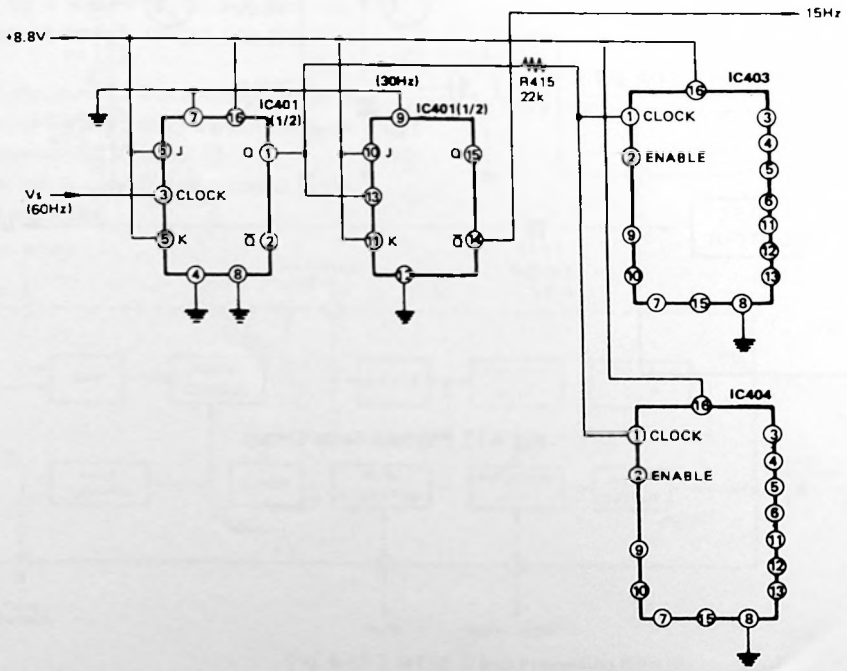


Fig. 5-1 Clock Pulse Generator Circuit

5-1. Clock Pulse Generator Circuit

The vertical scanning start (Vs) pulse (60Hz) is supplied from the Process circuit board to pin 3 of J-K flip-flop IC401. A 30Hz pulse obtained at pin 1 of IC401 is fed to pin 1 of 7-bit binary up counters IC403 and IC404 as a clock pulse. The 30Hz pulse at pin 1 of IC401 is also sent to another J-K flip-flop in IC401 through pin 13. A 15Hz pulse obtained at pin 14 is supplied to the white balance indicator circuit to drive the indicator.

5-2. White Balance Preset Circuit

When the power switch is turned ON, the base potential of Q406 is low momentarily due to C405. Therefore, Q406 is ON which turns Q407 ON. Q406 and Q407 form a latch circuit which stays ON until the white balance switch is placed in the SET position, and a high through D410 resets the latch.

When Q406 and Q407 are ON, Q405 is ON and pin 12 and 9 of the two flip-flops (latch) formed by IC402 are held low.

The high level at their output (pins 11 and 10) lift the INHIBIT inputs on pin 2 of 7-bit binary up counter IC403 and IC404. (IC403 is used to control the RED channel and IC404 is used for the BLUE channel). However, the counters do not count up, since the clock pulse fed to pin 1 of both up counters from IC401 is grounded through D404 and Q405.

The latch circuit Q406/Q407 also turns ON Q408 and Q409/Q410. Approximately +4V (set by R4042, D411 and the +3.3V supply) is fed to R. gain control amplifier in IC203 of the Process circuit board through Q409, terminal No. 1 of BI401, terminal No. 7 of CN204, buffer Q225 and pin 4 of IC203 to set the initial gain of R signal.

Similarly, the +4V is sent to B. gain control amplifier in IC203 of the Process circuit board through Q410, terminal No. 7 of BI401, terminal No. 6 of CN204, buffer Q226 and pin 13 of IC203 to set the initial gain of B signal.

In this way, the R. signal and B. signal levels are set so the camera will produce average white balance for 3200°K illumination when the power is first applied.

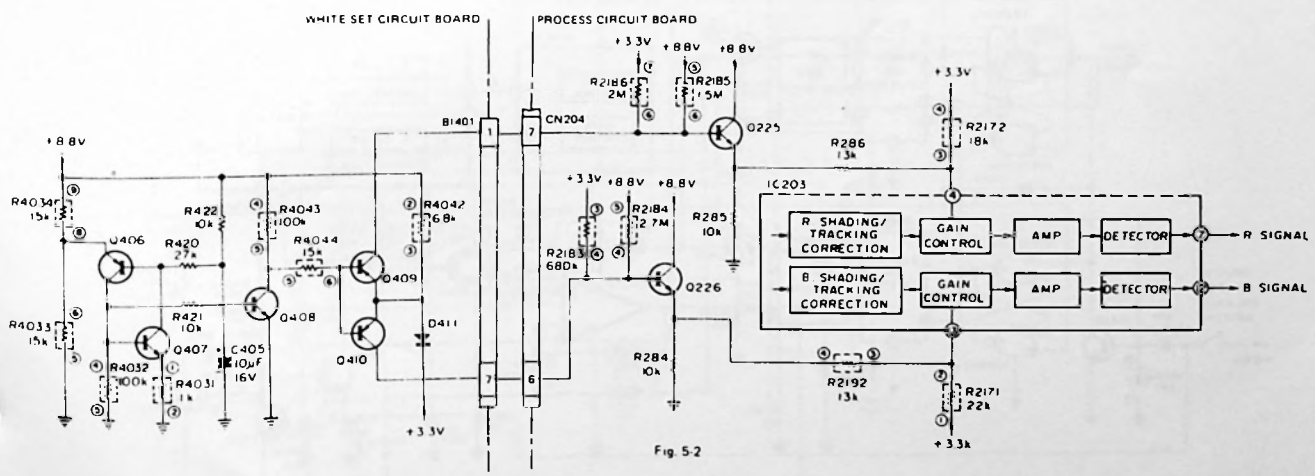


Fig. 5-2 White Balance Preset Circuit

5-3. Automatic White Balance Setting Circuit

When the white balance switch SW003 is placed to the SET position, +8.8V is applied to the base of Q406 through D410 to turn OFF the latch circuit Q406/Q407, Q405, Q408 and Q409/Q410. Therefore, the white balance preset circuit (previously described) turns OFF and the +4V to the RED and BLUE channel is removed. When the SW003 is placed to the SET position, Q402 turns ON as C401 charges and the low level at its collector acts as a SET command to both IC402 flip-flop (latch) sections just as Q405 did for preset. The high level on these flip-flop outputs at pins 11 and 10 lifts the INHIBIT input on pin 2 of 7-bit binary up counters (IC403 and IC404). At the same time, the high level at the base of Q402 is fed to pins 7 and 15 of both counters to reset them to 0. When Q402 turns OFF approximately 700 msec (determined by C401 and R4013), the 30Hz clock pulse appears at pin 1 and the counters start counting up. Pin 1 of both counters were grounded through D404 while Q402 was ON.

As the counters count up from 0→1→2→3 – the resistive digital/analog (D/A) network produces a staircase signal, starting from zero, by combining the binary outputs through a resistor ladder. The voltage level of this D/A converter will set the chroma (R or B) channel gain.

These signals buffered by Q225/Q226 and fed to the gain control amplifier in IC203 on the Process circuit board. This controls the RED and BLUE signal gain which was initially reduced to zero. Since RED and BLUE gain starts at zero, the white set process initially produces the other remaining color, GREEN. As the increasing voltage made by the stairstep raises the gain in the RED and BLUE channels in the Process circuit, the levels of RED and BLUE signal increase at IC203 pins 7 and 12. White balance will be attained when these levels match the Y_L signal (IC208 pin 2).

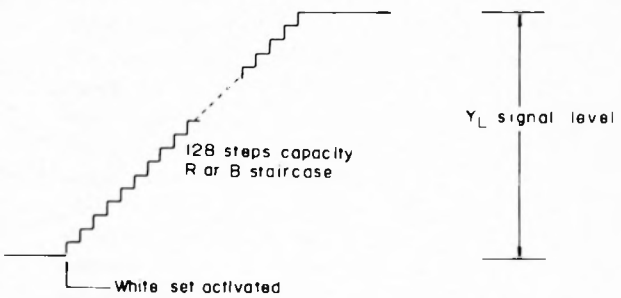


Fig. 5-3-2 Automatic White Balance Set

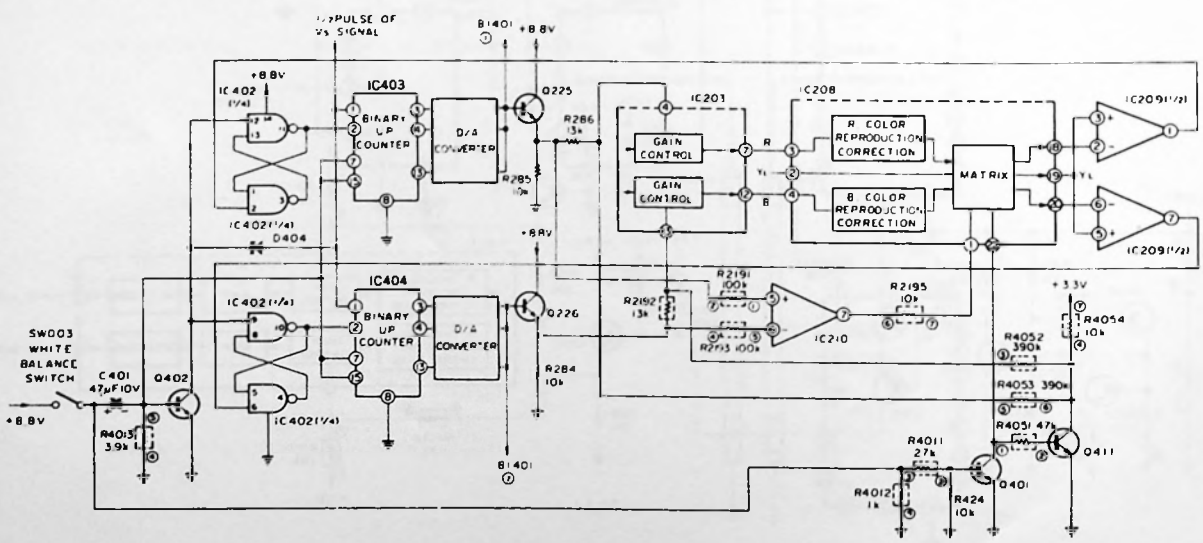


Fig. 5-3-1 Automatic White Balance Setting Circuit – 1

To determine when the occurs on Op-amp for each channel (IC209 pins 1, 2, 3 RED, pins 5, 6, 7 BLUE) compares the detected chroma levels (D.C.) which appear at IC208 (Pin 18-RED det. D.C., 19-Y_L det. D.C., 20-BLUE det. D.C.).

The outputs of comparison at pin 1 and 7 of IC209 are sent to pins 2 and 6 of flip-flop (latch) IC402. The outputs of comparator IC209 are high when the R and B signal levels are below the Y_L signal level. When either the R or B signal just exceeds the Y_L signal, the corresponding comparator switches its output to low, resets the appropriate flip-flop (IC402) output to low, and inhibits the coutner for that channel (RED or BLUE). The other channel counter stops counting in a similar fashion, at its appropriate time, determined by its comparator IC209.

Since by definition this means Y_L-R and Y_L-B are both zero, white balance has been achieved.

When the white balance indicator stops flashing, it indicates the camera is ready to use.

Since the diffusion filter has itself an inherent color filtering effect, the white balance shifts slightly when the white balance setting is accomplished and the diffusion filter is removed.

When in the white SET mode, Q401 generates a white balance low signal and Q411 enables R4052, R4053 and R4054, which go back to the Process circuit board.

When the DC level added by R4052, R4053 and R4054 is removed by Q411 being ON, the gains in latch channel should be reduced slightly for an almost exact match. This resistor matrix compensates for the white balance shift due to the diffusion filter.

Additionally, the camera has an optical color conversion filter which is inserted in the OUTDOOR position. However, when in the INDOOR mode, some color difference can occur in the light source. Q225 and Q226 are emitter follower buffers for the white balance circuit "stairstep" gain control, which when white balance is attained, becomes a fixed D.C. voltage. The main output of these transistor is to the gain control stages of IC203. However, a portion of the output from the white balance circuit is fed back to the matrix circuit to compensate for large differences in gain caused by light source difference (Such as fluorescent light.).

The white set low from Q401 inhibits any output from IC210 through D207. When the diffusion filter is removed, Q401 is OFF and the output of IC210 pin 7 is fed to the color matrix. At the same time, the matrix inhibit signal, which also comes from Q401 to D206 is removed for correcting the colorimetry imperfection resulting from the spectral characteristic of the stripe filter (refer to 4-9-1. Color Reproduction Correction Circuit on page 43). VR001 (COLOR ADJUSTMENT) is a control for fine adjustment of the red and blue signal gain.

VR228 (R. GAIN) is a red signal gain control.

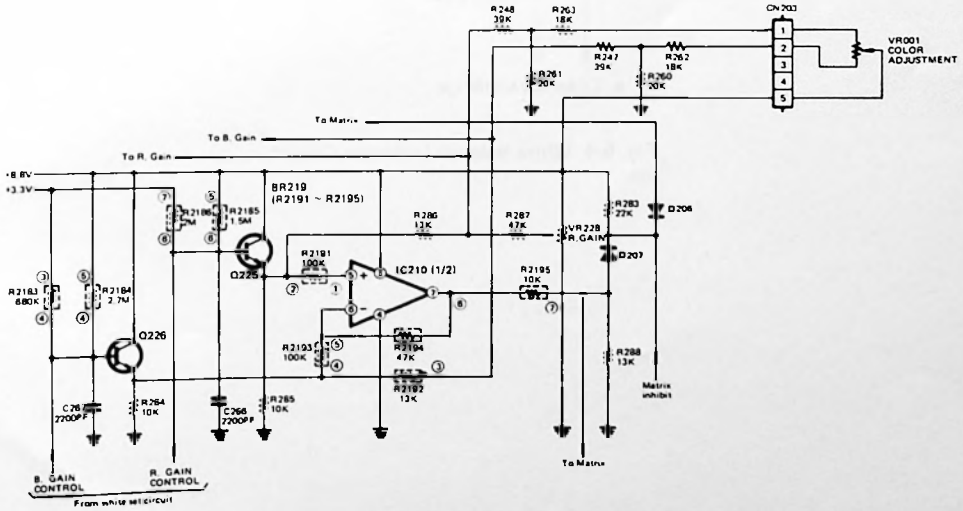


Fig. 5-3-3 Automatic White Balance Setting Circuit — 2

5-4. White Balance Indicator Circuit

When the power switch is turned ON and the white balance is not attemped, the potential at anodes of D406 and D407 is high. (Refer to 5-2. White Balance Preset Circuit on page 50).

Therefore, Q404 is turned ON and OFF by the 15Hz pulse supplied from IC401 pin 14, and the INDOOR indicator D1001 (used here as a White Balance Indicator) in the viewfinder flashes to indicate the white balance setting is required.

If the INDOOR/OUTDOOR switch is set to the INDOOR position, +8.8V is fed to D408, D1001 is kept flashing since Q403 is held ON by the high supplied through D406 and D407.

When the white balance switch is moved to the SET position, and white balance is accomplished, the flip-flop outputs which drive D406 and D407 become low, and Q404 is turned OFF, D1001 stops flashing since the 15Hz pulse is divided by R4023–R4025 and its level becomes smaller than 6V.

If the INDOOR/OUTDOOR switch is set to the INDOOR position at this time, +8.8V is fed to anode of D408, and D404 and D1001 are turned ON.

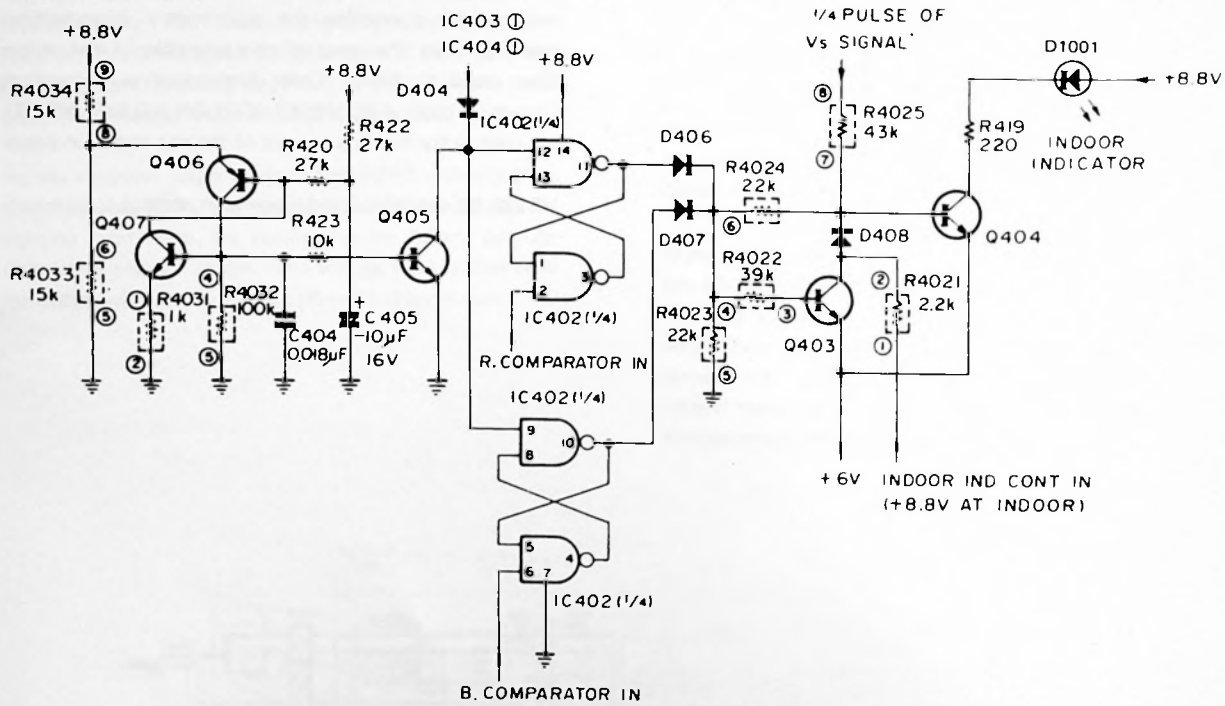


Fig. 5-4 White Balance Indicator Circuit

6. Electronic Viewfinder Circuit Boards

Electronic Viewfinder Circuit Board (YWV3100PZK6, ZK7, ZK8) consists of following circuits.

6-1. Video Amplifier Circuit

Outline

This circuit amplifies the video signal supplied from the Process circuit board and fed it to the cathode ray tube (CRT) together with the blanking pulse which is used to block retrace line on the CRT screen.

Details

The NTSC signal from the Process circuit board is supplied to buffer Q801 through terminal No. 1 of CN802. LC301, which is located on the power circuit board, is a trap for removing the chrominance component in the NTSC signal. The signal at the emitter of Q801 is fed to amplifier Q810 through VR801 (CONTRAST). The amplified signal is then applied to a mixing amplifier Q811.

The horizontal pulse from the secondary winding of flyback transformer (FBT) T801 and vertical (V) sawtooth signal from IC802 are supplied to base of Q812.

The composite blanking (BL) pulse obtained at the collector of Q812 by mixing the H. pulse and V. sawtooth signal is supplied to the emitter of Q811 and is mixed with the video signal supplied to its base. The video signal at the collector of Q811 is then supplied to grid-1 (G1) of the CRT together with the DC voltage set by VR803 (BRIGHTNESS). The iris indicator signal supplied from Q901 is also mixed with the video signal through R8108.

6-2. Sync Separation Circuit

Outline

This circuit generates the sync pulses from the composite video signal supplied from the Process circuit board and sends the horizontal sync pulses to the horizontal deflection circuit and vertical sync pulses to the vertical deflection circuit.

Details

The NTSC signal from the Process circuit board is supplied to a sync separator Q802 through the 3.58 MHz trap LC301 in the power circuit board, terminal No. 1 of CN802 and buffer Q801. Q802 detects only sync pulses of video signal which appear on its collector.

These separated sync pulses which contain horizontal (H) and vertical (V) sync pulses are applied to the differentiator consisting of C806 and R8006, where only the H. sync pulse passes. The H sync pulse is then supplied to Q804 in the H. automatic frequency control (AFC) circuit in the H. deflection circuit. The sync pulse at the collector of Q802 is sent via inverter Q803 to the integrator consisting of R824 and C826, where only V. sync pulse is passed. The V sync pulse is applied to Q809 in the V. deflection circuit.

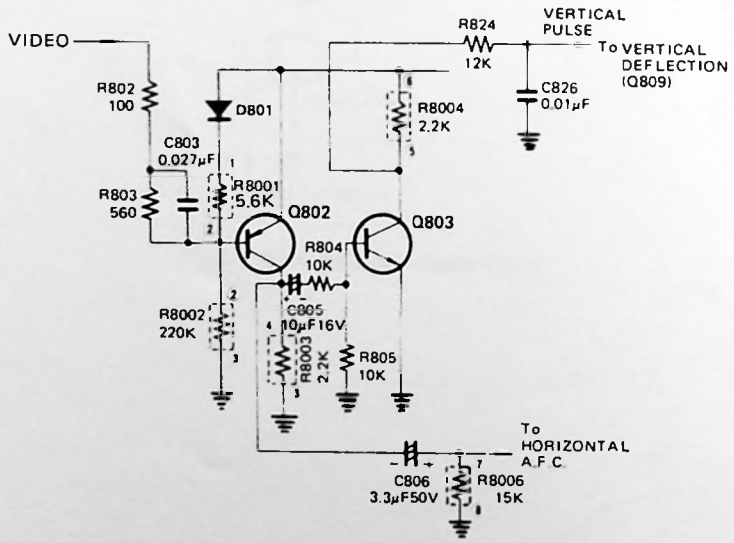


Fig. 6-2 Sync Separation Circuit

6-3. Vertical Deflection Circuit

Outline

This circuit generates vertical deflection sawtooth current for vertical scanning of the beam inside the cathode ray tube (CRT).

Details

The negative composite sync pulse from the collector of Q803 is supplied to the integrator circuit consisting of R824 and C826, where the H. sync pulse is removed and only the V. sync pulse is passed. The V. sync pulse is then fed to V. oscillator Q809 as a trigger pulse. Q809 is a free-running sawtooth generator using a thyristor whose frequency is approximately 50Hz determined by the time constant of C827, R8051 and R8052. When the trigger pulse is supplied to Q809, Q809 generates a 60Hz sawtooth signal. The sawtooth signal at the junction point of R8051 and R8052 is then supplied to pin No. 2 of differential amplifier IC802. The amplified sawtooth signal at pin No. 5 of IC802 is fed to the V. deflection coil through terminal No. 1 of CN801.

VR805 (V. SIZE) is control for vertical scanning size.

6-4. Horizontal Deflection Circuit

Outline

This circuit generates the horizontal deflection sawtooth current for horizontal scanning of the beam inside the CRT. This circuit contains the automatic frequency control (AFC) circuit which controls the frequency (phase) of the horizontal sawtooth current to correspond to that of horizontal sync pulse separated from the video signal.

Details

The H. sync pulse from the sync separation circuit is applied to phase comparator consisting of Q804, D802 and D803. The positive and negative H. sync pulses are obtained at the emitter and collector of Q804.

The flyback pulse obtained at the collector of Q808 is applied to the integrator consisting of R810, L802 and C810, and converted into a H. sawtooth signal. The H. sawtooth signal is supplied through C809 to the junction point of D802 and D803, and compared with the H. sync pulses in phase. The DC voltage corresponding to the phase difference is supplied to the voltage controlled oscillator (VCO) IC801 through low pass filter consisting of C811, C812, R809 and Q805 to control the oscillation frequency.

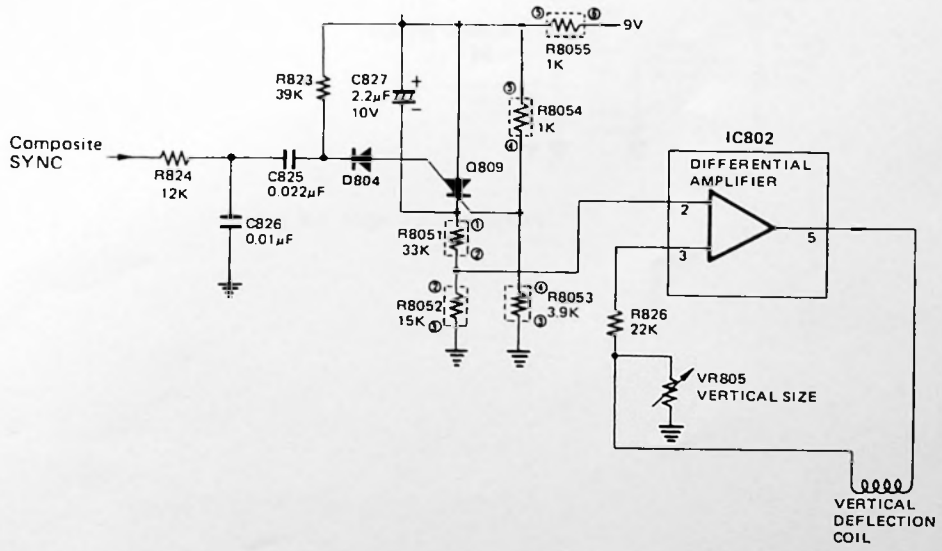


Fig. 6-3 Vertical Deflection Circuit

In this way, the H. OSC is automatically controlled to match its oscillation frequency with that of the sync pulse.

VR802 (H. HOLD) is a control for setting the oscillation frequency in a steady state.

The frequency controlled H. pulse from pin No. 3 of IC801 is supplied to H. deflection output Q808 through drivers Q806 and Q807. The H. deflection sawtooth current is supplied to the H. deflection coil from the collector of Q808 through C818, L805 (H. SIZE) and terminal No. 3 of CN801. L805 controls the H. scanning size on the CRT. Flyback pulse obtained at the collector of Q808 is fed to the high voltage circuit.

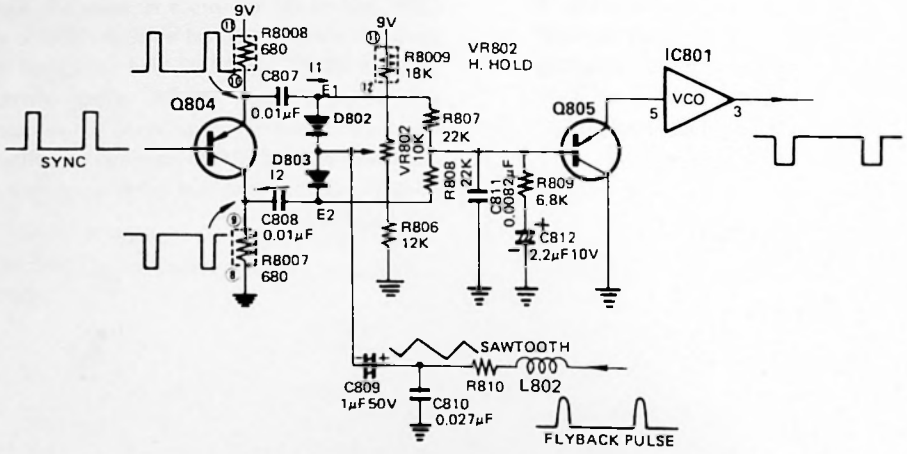


Fig. 6-4 AFC Circuit

6-5. High Voltage Circuit

Outline

This circuit generates high voltages for CRT electrodes.

Details

The flyback pulse generated in the horizontal (H) deflection circuit is supplied to the primary winding of flyback transformer (FBT) T8001 in high voltage pack T801 to step up the flyback pulse to necessary level. The boosted pulses obtained at the secondary winding of T8001 are rectified to generate high voltages.

4.5kV obtained by rectifying the boosted pulse with multiplier D8001 in T801 is supplied to the CRT anode. +600V obtained by rectifying the boosted pulse with D8002 and C821 is supplied to grid-3 (G3) of the CRT through VR804 (FOCUS). The voltage of grid-2 (G2) is derived by dividing +600V by means of resistors. The voltage of grid-1 (G1) is derived by rectifying the negative pulse from the FBT by D8003 and C820. Then the rectified −55V is divided by R817, R818 and VR803 (BRIGHTNESS) and supplied to G1 through VR803 together with the video signal supplied from the video amplifier circuit. The heater voltage for CRT is supplied from Deflection circuit board through terminal No. 8 of CN802.

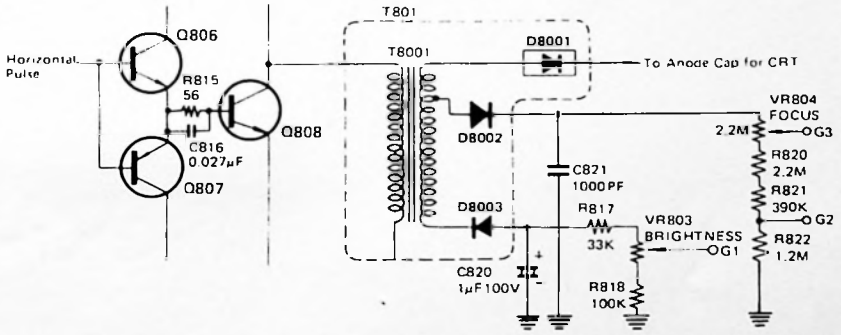


Fig. 6-5 High Voltage Circuit

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